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Analytical Model for the Piecewise Linearly Graded Doping Drift Region in LDMOS*

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Abstract: A novel 2D analytical model for the doping profile of the bulk silicon RESURF LDMOS drift region is proposed. According to the proposed model, to obtain good performance, the doping profile in the total drift region of a RESURF LDMOS with a field plate should be piecewise linearly graded. The breakdown voltage of the proposed RESURF LDMOS with a piecewise linearly graded doping drift region is improved by 58.8%, and the specific on-resistance is reduced by 87.4% compared with conventional LDMOS. These results are verified by the two-dimensional process simulator Tsuprem-4 and the device simulator Medici.

Key words: breakdown voltage; specific on-resistance; piecewise linearly graded doping drift region
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1 Introduction

Reduced surface field (RESURF) technology[1] has been widely applied in high-voltage integrated circuit (HVIC) devices and smart power integrated circuits (SPICs) devices[2~4]. The main advantages of high-voltage devices with RESURF technology are the lowering of on-resistance and the reduction of chip size under high drain voltages. Lateral double-diffused MOS (LDMOS) is one of the most popular high voltage devices due to its easy integration with standard low-voltage CMOS. The breakdown voltage and the on-resis-tance are the two most important performance factors for LDMOS, but these two electrical parameters often conflict with each other in processing technology. In recent years, much research on how to improve the breakdown voltage and reduce the specific on-resistance has been reported[5~12]. Linearly graded doping in the drift region of LDMOS was found to be one effective way to improve LDMOS performance[8~12]. References [8,9] predicted that a linear lateral doping profile in the drift region in SOI could yield the maximum breakdown voltage and the minimum specific on-resistance for SOI RESURF LDMOS. A computer program was developed to help realize a linear lateral doping profile, and experimental verifications were also performed[10]. However, References [8~10] apply only to SOI RESURF LDMOS. References [11,12] show that a linear lateral doping profile in the drift region in bulk-silicon also could improve the performance, but the model and simulated results are too simple ——the thickness of the oxide above the drift region was assumed to be uniform, and the influence of the field plate on the performance of the BS RESURF LDMOS was not considered.

The purpose of this work is to develop a 2D analytical model for the doping profile of the drift region in LDMOS with a field plate in terms of Poisson's solution. According to the proposed model, the doping profile in the total drift region of a RESURF LDMOS with a field plate must be piecewise linearly graded in order to obtain the best performance. A RESURF LDMOS with a piecewise linearly graded doping drift region was simulated by the 2D semiconductor device simulators Tsuprem-4 and Medici. The simulation results show that the novel LDMOS has an improved trade-off

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between the breakdown voltage and the specific on-resistance compared to conventional LDMOS. We think the model and the method will help designers improve the performance of high-voltage BS RESURF devices in practical LDMOS design.

2 Analytical models

A schematic cross section of the BS RESURF LDMOS structure with a step oxide layer in the drift region is shown in Fig. 1, where x is the horizontal position relative to the left edge of the drift region and y is the vertical position relative to the surface of the drift region. The drift region is divid-

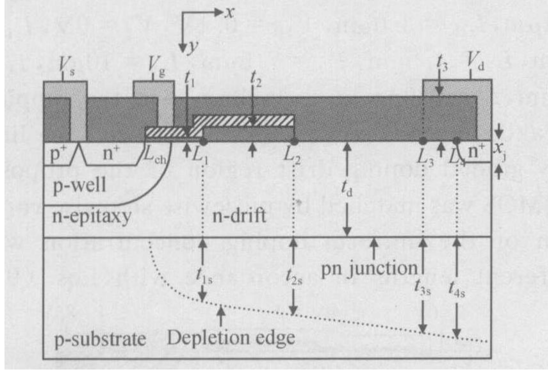

Fig. 1 Cross section of the BS RESURF LEDMOS structure

ed into four regions, the boundaries of which are denoted by L_1, L_2, L_3, and L_4. The p-substrate, whose doping concentration is N_{sub}, is assumed to be thick enough to deplete the substrate charge, and the width of the substrate depletion layers under L_i (i = 1, 2, 3, and 4) are t_{1s}, t_{2s}, t_{3s} and t_{4s}, respectively. Here, t_1 is the thickness of the gate oxide layer, t_2 and t_3 are the thicknesses of the field oxide layer under the poly gate-field-plate and the aluminum drain-field-plate, respectively. The relative dielectric constants of the oxide and the semiconductor are ε_{ox} and ε_{si}, respectively. The gate voltage is V_g, and the substrate and the source are grounded, while the drain is supplied with a positive voltage V_d. The n-epitaxy layer thickness is t_d with a doping concentration profile of $N_d(x)$. The potential function $\phi(x, y)$ in silicon film must be satisfied by Poisson's equation, yielding

$$\frac{d^2\phi(x,y)}{dx^2} + \frac{d^2\phi(x,y)}{dy^2} = -\frac{qN_d(x)}{\varepsilon_0\varepsilon_{si}} \quad (1)$$

Based on the theory in Ref. [13] we integrate Poisson's equation over the y-direction in the n-drift region, and obtain the following equation for $0 \le x \le L_1$.

$$\int_0^{t_d} \frac{d^2\phi_1(x,y)}{dx^2} dy + E_{1y}(x,0) - E_{1y}(x,t_d) = -\frac{qN_d(x)}{\varepsilon_0\varepsilon_{si}} t_d, \quad 0 \le x \le L_1 \quad (2)$$

Assuming that the electrical flux along the Si/SiO$_2$ interface is continuous, the following equation can be obtained by neglecting the influence of the fixed charge in the SiO$_2$ material.

$$E_{1y}(x,0) = -\frac{\varepsilon_{ox}[\phi_1(x,0) - V'_g]}{\varepsilon_{si} t_1} \quad (3)$$

Here, $V'_g = V_g - V_{FB}$ is the applied voltage, and V_{FB} is the flat-band voltage. Assuming that the n-drift region is fully depleted, we get

$$E_{1y}(x,t_d) = \frac{2[\phi_1(x,0) - \phi_1(x,t_d)]}{t_d} = \frac{2[\phi_1(x,t_d) - 0]}{t_{s1}} = \frac{2[\phi_1(x,0)]}{t_d + t_{s1}} \quad (4)$$

Here t_{s1} can be defined as $\frac{t_{1s}}{2}$ according to the assumption in Ref. [14]. According to the RESURF principle, the depletion approximation is suitable for the n-drift region. We can assume $\frac{d^2\phi_1(x,y)}{dx^2} \approx \frac{d^2\phi_1(x,0)}{dx^2}$ in the first-order approximation[15]. From Eqs. (2～4), we obtain

$$\frac{d^2\phi_1(x,0)}{dx^2} - \alpha_1\phi_1(x,0) = \beta_1 \quad (5)$$

where $\alpha_1 = \frac{\varepsilon_{ox}}{\varepsilon_{si} t_1 t_d} + \frac{2}{t_d(t_d + t_{s1})}$, and $\beta_1 = -[\frac{qN_d(x)}{\varepsilon_0\varepsilon_{si}} + \frac{\varepsilon_{ox}}{\varepsilon_{si} t_1 t_d} V'_g]$.

In the same way, we can obtain three similar equations under the conditions of $L_1 \le x \le L_2$, $L_2 \le x \le L_3$, and $L_3 \le x \le L_4$. The only difference is that $E_{3y}(x,0) = 0$ for $L_2 \le x \le L_3$ according to Ref. [16]. Then, we obtain the general expression

$$\frac{d^2\phi_i(x,0)}{dx^2} - \alpha_i\phi_i(x,0) = \beta_i \quad (6)$$

where

$$\alpha_2 = \frac{\varepsilon_{ox}}{\varepsilon_{si} t_2 t_d} + \frac{2}{t_d(t_d + t_{s2})}$$

$$\beta_2 = -[\frac{qN_d(x)}{\varepsilon_0\varepsilon_{si}} + \frac{\varepsilon_{ox}}{\varepsilon_{si} t_2 t_d} V'_g]$$

$$\alpha_3 = \frac{2}{t_d(t_d + t_{s3})}, \quad \beta_3 = -\frac{qN_d(x)}{\varepsilon_0\varepsilon_{si}}$$

$$\alpha_4 = \frac{\varepsilon_{ox}}{\varepsilon_{si} t_3 t_d} + \frac{2}{t_d(t_d + t_{s4})}$$

$$\beta_4 = -\left[\frac{qN_d(x)}{\varepsilon_0\varepsilon_{si}} + \frac{\varepsilon_{ox}}{\varepsilon_{si} t_3 t_d} V'_d\right]$$

$$V'_d = V_d - V_{FB}$$

Neglecting the influence of the junction depth of the drain region, according to Ref. [15], t_{4s} can be defined by the following equation, which follows from the 1D Poisson's equation.

$$t_{4s} = \frac{t_d}{2} \times \left(\sqrt{1 + \frac{8\varepsilon_{si}\varepsilon_0}{qN_{sub} t_d^2}} - 1\right) \qquad (7)$$

According to the RESURF principle, if the n-drift region is fully depleted and the concentration of the p-substrate is uniform, then t_{is} can be approximately defined as $t_{is} = \frac{L_i}{L_4} t_d$ ($i = 1, 2$, and 3). Based on the assumption in Ref. [14], t_{si} can be defined as $t_{si} = \frac{t_{is} + t_{(i-1)s}}{2}$, where $i = 2, 3$, and 4.

According to Ref. [12], in order to attain the maximum breakdown voltage, the surface potential distribution should follow the equation

$$\phi(x, 0) = \frac{V_d}{L_4} x \qquad (8)$$

Substituting Eqs. (8) and (7) into Eq. (6), we obtain the following equations:

$$N_{d1}(x) = M\alpha_{f1} x - \frac{\varepsilon_0\varepsilon_{ox}}{qt_1 t_d} V'_g, \quad 0 \le x \le L_1 \qquad (9)$$

$$N_{d2}(x) = M\alpha_{f2} x - \frac{\varepsilon_0\varepsilon_{ox}}{qt_2 t_d} V'_g, \quad L_1 \le x \le L_2 \qquad (10)$$

$$N_{d3}(x) = M\alpha_{f3} x, \quad L_2 \le x \le L_3 \qquad (11)$$

$$N_{d4}(x) = M\alpha_{f4} x - \frac{\varepsilon_0\varepsilon_{ox}}{qt_3 t_d} V'_d, \quad L_3 \le x \le L_4 \qquad (12)$$

where $M = \frac{\varepsilon_0\varepsilon_{si}}{qL_4} V_d$.

From Eqs. (9～12), we can draw a very useful conclusion. To obtain the maximum breakdown voltage, an improved trade-off between the breakdown and the specific on-resistance, the doping profile in the total drift region in an LDMOS with a field plate must be piecewise linearly graded. The following sections provide some results from Tsuprem-4 and Medici to show that the piecewise linearly graded doping drift region is very effective for improving the performance of BS RESURF LDMOS.

3 Simulation and discussion

The cross sections of the proposed and the conventional BS RESURF LDMOS structures are uniform, as can be seen in Fig. 1. Figure 2 shows the equipotential contour lines of the conventional (a) and the proposed (b) BS RESURF LDMOS at their breakdown voltages. The simulation results of the conventional LDMOS are obtained with $N_{sub} = 1 \times 10^{15} cm^{-3}$, $N_d = 3 \times 10^{14} cm^{-3}$, $t_d = 3.1\mu m$, $L_{ch} = 3.0\mu m$, $V_{FB} = 0.1V$, $V_g = 0V$, $L_1 = 1\mu m$, $L_2 = 4.5\mu m$, $L_3 = 7.5\mu m$, $L_4 = 10\mu m$, $t_1 = 30nm$, $t_2 = 630nm$, $t_3 = 1630nm$, and the supplied breakdown voltage $V_d = 85V$. The piecewise linearly graded doping drift region of the proposed LDMOS was matched by piecewise stepwise variation of the uniform doping concentration with different lengths in

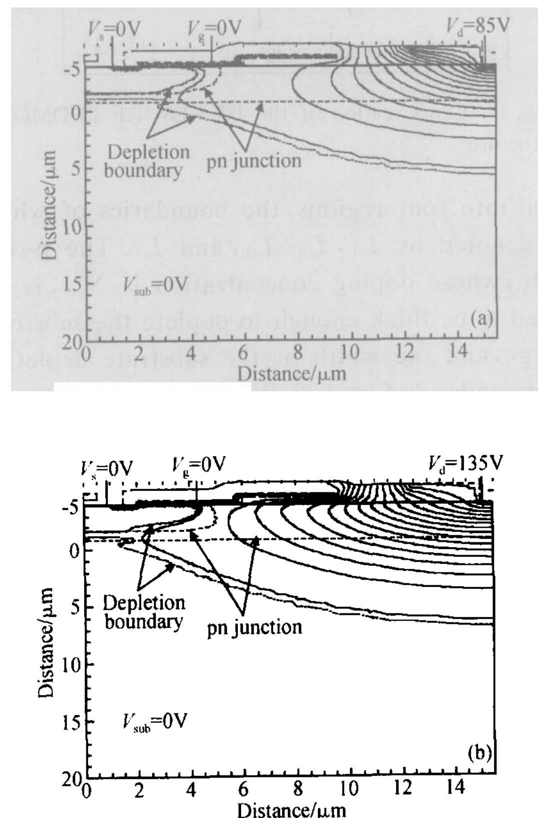

Fig. 2 Equipotential contour lines of the conventional (a) and the proposed (b) BS RESURF LDMOS at their breakdown voltages

accordance with Eqs. (9 ~ 12). In the practical process, the piecewise linearly graded drift region doping profile can be fabricated using a single phosphorus implant through a mask with a series of openings of different sizes[17]. The other parameters of the proposed LDMOS are the same as the conventional structure except for the applied breakdown voltage in the simulations. The contour lines along the drift region of the conventional LDMOS is not symmetrical, and the contour lines crowd at the drain region, which results in an avalanche breakdown, as can been seen in Fig. 2(a). However, from Fig. 2(b) we find that the contour lines along the drift region of the proposed RESURF LDMOS with a piecewise linearly graded doping drift region are very symmetrical, which improves the breakdown voltage. If the ionization integral is equal to 1, an avalanche breakdown will occur. In this way, the breakdown voltage of the conventional LDMOS is limited to 85V, but the breakdown voltage of the proposed RESURF LDMOS with piecewise linearly graded doping drift region can reach 135V, which can be seen in Fig. 3. The breakdown voltage of the proposed RESURF LDMOS is improved by 58.8% compared with that of conventional LDMOS.

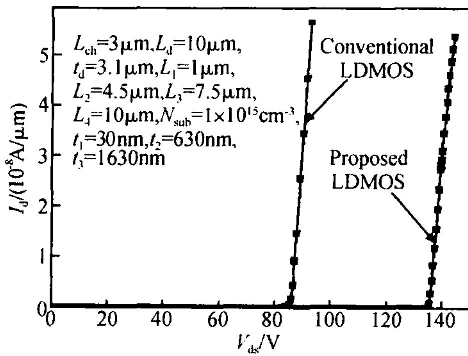

Fig. 3 Breakdown characteristic curves of the proposed and the conventional LDMOSs

Figure 4 shows the surface electrical field distribution along the drift region of the proposed and the conventional LDMOS at their breakdown voltages. There are five electrical field peaks in the surface electrical field distribution of the proposed LDMOS with the piecewise linearly graded doping drift region, and each electrical field peak value is less than that of the critical electrical field. This kind of surface electrical field distribution can greatly reduce the maximum peak electrical field so as to obtain the maximum breakdown voltage, which agrees with the theoretical analysis we introduced earlier in Ref. [18]. In contrast, there are only two electrical field peaks in the surface electrical field distribution of the conventional LDMOS, and the maximum electrical field peak reaches a magnitude of 2.5×10^5 V/cm at the drain edge. The nonuniform electrical field will greatly reduce the breakdown voltage.

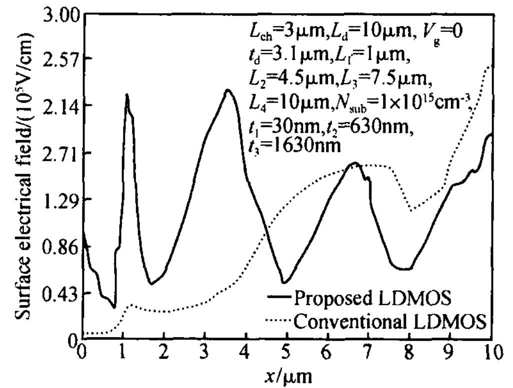

Fig. 4 Surface electrical field distribution along the drift region of the proposed and the conventional LDMOSs at their breakdown voltages

Figure 5 shows the surface potential distribution along the drift region of the proposed and the conventional LDMOS at their breakdown voltages. One can see from Fig. 5 that the potential distribution of the proposed LDMOS with the piecewise linearly graded doping drift region is approximatively linear, which is in agreement with Eq. (8) and thus can attain the maximum breakdown voltage. The linear distribution of the surface potential also leads to the optimal electrical field distribution

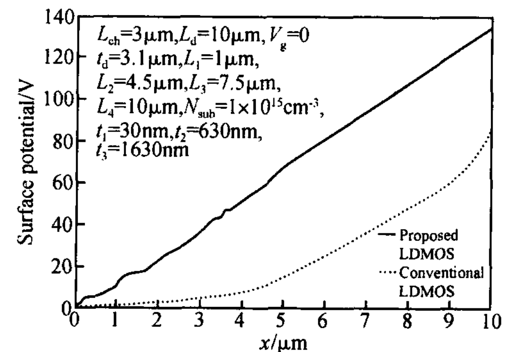

Fig. 5 Surface potential distribution along the drift region of the proposed and the conventional LDMOSs at their breakdown voltages

in the drift region of the piecewise linearly graded doping drift region LDMOS (seen in Fig.4). In contrast, the potential distribution of the conventional LDMOS shows a large curvature in the whole drift region, which leads to a non-uniform electrical field profile (seen in Fig.4). Consequently, the breakdown voltage suffers a considerable degradation.

Figure 6 shows the I-V curves of the conventional (a) and the proposed (b) BS RESURF LDMOS. One can see that the saturation characteristic of the proposed LDMOS with the piecewise linearly graded doping drift region is better than that of the conventional LDMOS. The specific on-resistance R_{on} can be extracted from the simulated I-V curves in the linear region and the channel length of the LDMOS. The numerically calculated values of R_{on} are 27.7 and 3.5m$\Omega \cdot cm^2$ at $V_g = 5V$ for the conventional and the proposed RESURF LDMOS, respectively, yielding a reduction of 87.4%. Here, we think the concentration of the proposed LDMOS with piecewise linearly graded doping drift region is higher than that of the conventional LDMOS, so the proposed LDMOS allows a significant reduction of the specific on-resistance compared with the conventional LDMOS.

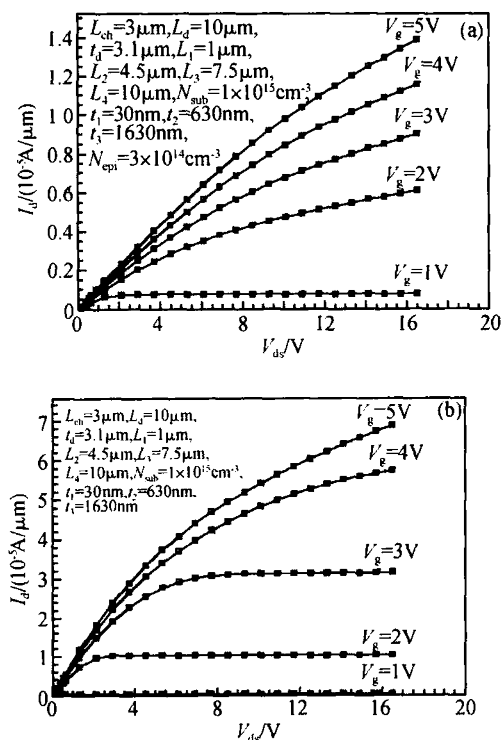

Fig.6 I-V curves of the conventional (a) and the proposed (b) BS RESURF LDMOS

4 Conclusion

A novel 2D analytical model for the doping profile of the bulk silicon RESURF LDMOS drift region has been proposed. The influence of the field plate and the variation of oxide layer thickness on the breakdown voltage and the specific on-resistance is taken into account in the model. According to the presented model, in order to obtain the maximum breakdown and the minimum specific on-resistance, the drift region doping profile of a RESURF LDMOS with a field plate must be piecewise linearly graded. In this way, a novel RESURF LDMOS with a piecewise linearly graded doping drift region is proposed, for which the breakdown voltage is improved by 58.8%, and the specific on-resistance is reduced by 87.4% compared to those of conventional LDMOS.

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体硅 LDMOS 漂移区杂质分段线性注入模型研究*

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摘要: 提出了体硅 LDMOS 漂移区杂质浓度分布的一种二维理论模型,根据该模型,如果要使带有场极板的 LDMOS 得到最佳的性能,那么 LDMOS 漂移区的杂质浓度必须呈分段线性分布. 用半导体专业软件 Tsuprem-4 和 Medici 模拟证明了该模型十分有效,根据该模型优化得到的新型 LDMOS 的击穿电压和导通电阻分别比常规 LDMOS 增加 58.8 %和降低 87.4 %.

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