Total Dose Radiation-Hard 0.8μm SOI CMOS Transistors and ASIC

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Abstract: This paper presents the total dose radiation performance of 0.8μm SOI CMOS devices fabricated with full dose SIMOX technology. The radiation performance is characterized by threshold voltage shifts and leakage currents of transistors and standby currents of ASIC as functions of the total dose up to 500krad(Si). The experimental results show that the worst case threshold voltage shifts of front channels are less than 320mV for pMOS transistors under off-gate radiation bias at 1Mrad(Si) and less than 120mV for nMOS transistors under on-gate radiation bias. No significant radiation-induced leakage current is observed in transistors to 1Mrad(Si). The standby currents of ASIC are less than the specification of 5μA over the total dose range of 500krad(Si).

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1 Introduction

Silicon-on-insulator(SOI) technology has attracted great interest lately because of its major advantages over bulk substrates, including total device isolation, speed, and density[1].

For hardened applications, SOI technologies present several advantages over their bulk counterparts. They are immune to latch-up, thanks to the complete dielectric isolation of their transistors. Moreover, their small sensitive volume limited by the buried oxide ensures a low sensitivity to single event effects[2,3]. A very high total dose hardening level can also be achieved with partially-depleted SOI technologies[4~15].

In order to improve the total dose radiation hardness of ASIC, we develop a total dose radiation-hard 0.8μm SOI CMOS process. In this paper, key radiation sensitive parameters such as the threshold voltages of individual transistors and leakage currents as a function of total dose will be investigated and discussed. Specifically, the radiation-induced threshold voltage shifts of front and back channel transistors are used to assess the radiation hardness of the gate oxide and the buried oxide, and the radiation-induced leakage currents of transistors and standby currents of ASIC will be presented to assess the isolation oxide.

2 Experiment

Our 0.8μm SOI CMOS transistors and ASIC were fabricated on full dose SIMOX wafers. We found that SIMOX materials meeting these requirements yield ASIC reasonably well. The buried oxide thickness is approximately 375nm, and the top silicon thickness is approximately 235nm. In our 0.8μm SOI CMOS technology, n and p wells are implanted to create partially depleted surface channel nMOS transistors and buried channel pMOS transistors, so that a neutral region always exists between the front and back gates. A single n^+ polysilicon gate technology was used. We used LOCOS isolation and two layers of metal.

To improve the front channel capabilities of nMOS and to ensure enough back channel threshold voltage, research has been done to optimize the channel doping process of nMOS, and the device structure used in the circuit design has been hardened as well. Then at a high dose of 1Mrad (Si) of radiation, the back channel threshold voltage can exceed 23V.

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The individual transistors in the process monitor, used for testing, are totally oxide-isolated. The gate length is 0.8μm, and the gate oxide thickness is 17.5nm. We have used lightly doped drain (LDD) technology for both nMOSFETs and pMOSFETs.

We used an HP 4145A parametric analyzer for characterizing the input and output characteristics of the individual transistors before radiation testing. We used an ARACOR model 4100 X-ray source for the total ionizing radiation testing. The total dose radiation effects for individual transistors were characterized by radiation-induced threshold voltage shifts and leakage currents as functions of the total dose up to 1 Mrad(Si). The dose rate used for testing individual transistors is 15krad (Si)/min. Worst-case radiation effects (largest shift under a specific irradiation bias) are emphasized and presented. In this paper we will adopt worst-case bias conditions with respect to MOSFETs; that is, the pMOS transistors were at off-gate bias and the nMOS transistors were at on-gate bias. The worst-case bias will be given in the inset of each figure showing the respective radiation test. A voltage of 5V is used in the radiation bias.

3 Results and discussion

3.1 Pre-radiation results

Figure 1 shows typical output current-voltage characteristics of an 8.0/0.8 surface channel nMOS transistor. The negative conductance effect is very small for the 0.8μm SOI nMOS transistors at V_{ds} = 5V. Figure 2 shows typical output current-voltage characteristics of an 8.0/0.8 surface channel pMOS transistor. The sloped saturation region is typical of the buried channel pMOS transistors.

From Figs. 1 and 2, it can be seen that when V_{gs} = ±5V, the saturation current is 1.8mA for nMOS and 1.29mA for pMOS. For nMOS, because of the SCBE (substrate current body effect) and the self-heating effect, I_{ds} increases distinctly with a large V_{ds}, and negative resistance can be observed for a large I_{ds}. For pMOS, an unsaturated current effect can be observed obviously for the same reason.

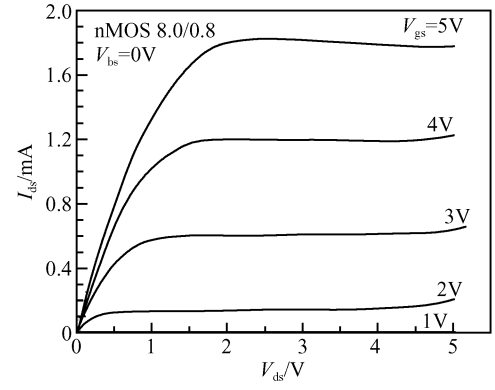

Fig. 1　Output characteristics of an 8.0/0.8 nMOSFET

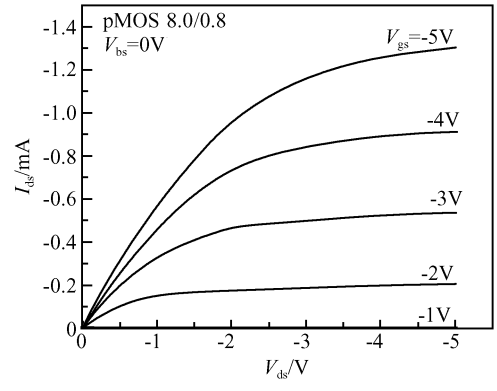

Fig. 2　Output characteristics of an 8.0/0.8 pMOSFET

The input current-voltage characteristics of an n-channel transistor are shown in Fig. 3 at V_{ds} = 0.1V, and that of a p-channel transistor are shown in Fig. 4 at V_{ds} = −0.1V. Very low leakage currents (~0.25pA/μm) were observed for these 0.8μm n-channel transistors, and ~0.02pA/μm for 0.8μm p-channel transistors. For SOI MOS devices, since there is no large area of pn junctions compared to the bulk MOS, the leakage current is much smaller.

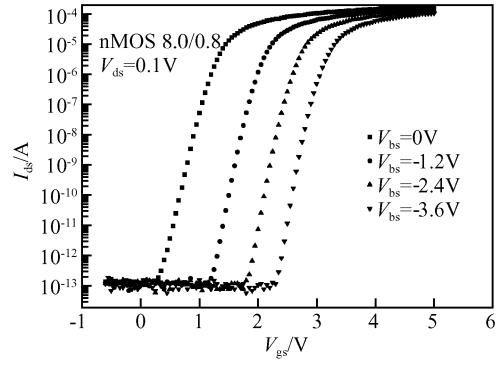

Fig. 3　Input characteristics of an 8.0/0.8 nMOSFET

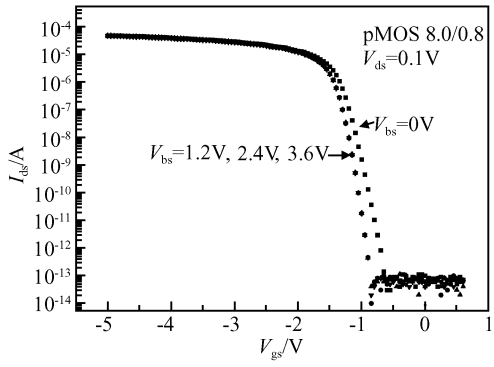

Fig. 4 Input characteristics of an 8.0/0.8 pMOSFET

Before radiation testing, the front channel threshold voltages (V_{t1}) and back channel threshold voltages (V_{t2}) of individual transistors were measured. Their average values are summarized in Table 1. We also measured the breakdown voltages of these transistors, which are greater than 10V.

Table 1 Pre-radiation threshold voltages

Parameter	V_{t1}/V	V_{t2}/V
nMOS	1.2±0.05	38±2
pMOS	−0.9±0.05	−13±1.5

3.2 Post-radiation results

First, we did the radiation response test on bench for individual 8.0/0.8 transistors. The total dose conditions used were 100krad(Si), 200krad(Si), 500krad(Si), and 1Mrad(Si). The threshold voltage of the front and back channels shift toward the negative direction for nMOS and pMOS devices because of the radiation-generated holes in the buried oxide.

Figure 5 shows the radiation-induced shift in input characteristics for a front channel nMOSFET at on-gate radiation bias ($V_g = 5V$, $V_s = V_d = V_{body} = V_{back} = 0V$). A small shift is observed, implying that the gate oxide is hard. The worst case threshold voltage shifts of the front channels are less than 120mV for nMOS transistors at 1Mrad(Si).

Figure 6 shows the radiation-induced shift in input characteristics of an 8.0/0.8 back channel nMOSFET at on-gate radiation bias ($V_g = 5V$, $V_s = V_d = V_{body} = V_{back} = 0V$). The threshold voltage of the back channel is taken at a back gate voltage where the conduction current is 1μA. Although a large shift (16V) is seen, the back channel threshold voltage is 23V at 1Mrad(Si); that is, a large margin still exists for the back channel nMOS transistor.

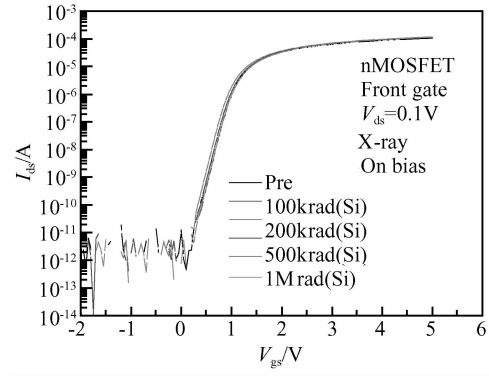

Fig. 5 Radiation-induced shift of input characteristics of an 8/0.8 front channel nMOSFET (Radiation bias: $V_g = 5V$, $V_s = V_d = V_{body} = V_{back} = 0V$)

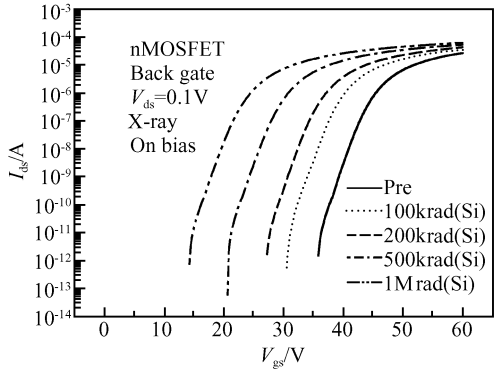

Fig. 6 Radiation-induced shift of input characteristics of an 8/0.8 back channel nMOSFET (Radiation bias: $V_g = 5V$, $V_s = V_d = V_{body} = V_{back} = 0V$)

The back channel threshold voltage shift of nMOS is relatively large, which is similar to the result of Ref. [11]. In Ref. [11], the back channel threshold voltage shift of nMOS goes toward saturation when the total dose of radiation exceeds 1Mrad(SiO_2), but this phenomenon has not been observed in this work.

Figure 7 shows the radiation-induced shift in input characteristics of a front channel pMOSFET at off-gate radiation bias ($V_g = V_s = V_{body} = 5V$, $V_{back} = V_d = 0V$). A larger shift is seen for the pMOS transistor than for the nMOS transistor. The worst case threshold voltage shifts of the front channels are less than 320mV for pMOS transistors at 1Mrad(Si).

Figure 8 shows the radiation-induced shift in input characteristics of an 8.0/0.8 back channel pMOSFET at off-gate radiation bias ($V_s = V_g =$

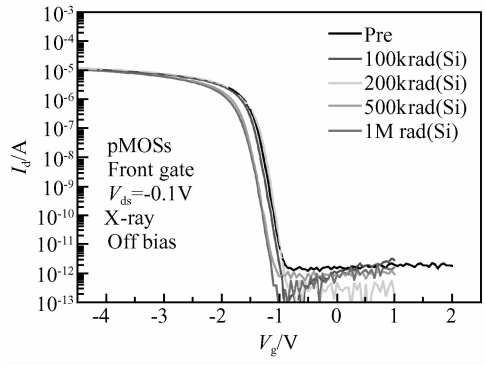

Fig. 7　Radiation-induced shift of input characteristics of an 8/0.8 front channel pMOSFET (Radiation bias: $V_g = V_s = V_{body} = 5V$, $V_{back} = V_d = 0V$)

$V_{body} = 5V$, $V_{back} = V_d = 0V$). The threshold voltage of the back channel is again taken at a back gate voltage where the conduction current is 1μA. The radiation-induced threshold shift is less than 3V. The back channel threshold voltage at 1Mrad(Si) is $\sim -15.4V$, so a large margin also exists for the pMOSFET.

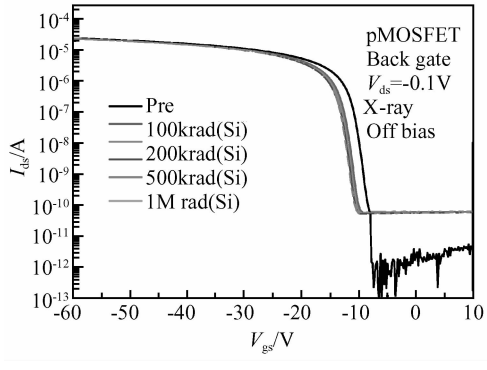

Fig. 8　Radiation-induced shift of input characteristics of an 8/0.8 back channel pMOSFET (Radiation bias: $V_g = V_s = V_{body} = 5V$, $V_{back} = V_d = 0V$)

It can be seen from Figs. 5$\sim$8 that the saturation current of nMOS rises with the increase of the total dose radiation. After the radiation at 1Mrad (Si) total dose, the saturation current I_{dsat} ($V_{gs} = 5V$, $V_{ds} = 5V$) rises from 1.8mA before radiation to 2.1mA, which is an increase of about 16.7%. Compared to nMOS, the front channel threshold voltage shift of pMOS is much larger. This is because the positive-charged hole trapped in the buried oxide is coupled with the front channel. In addition, the threshold voltage shift of the back and front channels of pMOS goes toward saturation when the total dose radiation reaches 1Mrad(Si). The saturation current of pMOS decreases with the increase of the total dose radiation. Obviously, the saturation current of pMOS is sensitive to total dose radiation that is less than 500krad(Si). When the total dose radiation is larger than 500krad(Si), the saturation current also decreases with the increase of total dose radiation, but the decrease is not so significant. After the 500krad(Si) total dose radiation, the saturation current I_{dsat} ($V_{gs} = 5V$, $V_{ds} = 5V$) is reduced from 1.29mA before radiation to 1.02mA, which is a decrease of about 21%. But after 1Mrad (Si) total dose radiation, the saturation current is reduced to 0.96mA, which is a decrease of about 25.5%.

3.3　Standby currents

We characterized standby currents using ASIC 10k (approx.) gates. Standby currents of chips such as large transistor arrays and ASIC may consist of leakages associated with gate oxide, buried oxide, field edges, defects, LOCOS isolation, and subthreshold conduction. Irradiation experiments were done in a Co^{60} gamma source with a 5V power supply. The experimental results are shown in Table 2.

Table 2　Experimental results of radiation

	Standby current /μA	Function	VOL /mV	VOH /V
Pre-radiation	2.69	pass	88.6	4.33
100krad(Si)	1.99	pass	83.6	4.29
400krad(Si)	1.48	pass	83.6	4.10
500krad(Si)	3.76	pass	83.6	4.10

4　Conclusion

In summary, we have presented worst-case dose radiation data on 0.8μm SOI CMOS transistors fabricated in full dose SIMOX wafers. The results show that: (1) the maximum front channel threshold voltage shift is less than 320mV at 1Mrad(Si) for pMOS and less than 120mV for nMOS transistors; (2) the maximum back channel threshold voltage shift is less than 16V for nMOS at 1Mrad(Si) and less than 3V for pMOS transistors; and (3) standby currents of ASIC 10K gates are well within the 5μA specification up to 500krad(Si).

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抗总剂量辐射 0.8μm SOI CMOS 器件与专用集成电路

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摘要：介绍了采用全剂量 SIMOX SOI 材料制备的 0.8μm SOI CMOS 器件的抗总剂量辐射特性，该特性用器件的阈值电压、漏电流和专用集成电路的静态电流与高达 500krad(Si)的总剂量的关系来表征. 实验结果表明 pMOS 器件在关态下 1Mrad(Si)辐射后最大阈值电压漂移小于 320mV，nMOS 器件在开态下 1Mrad(Si)辐射后最大阈值电压漂移小于 120mV，器件在总剂量 1Mrad(Si)辐射后没有观察到明显漏电，在总剂量 500krad(Si)辐射下专用集成电路的静态电流小于 5μA.

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