A 1.1GHz LC VCO with Automatic Amplitude Control for Tuner Applications *

Yan Jun[1,†], Mao Wei[1], Ma Desheng[1], Gu Ming[1], Xu Qiming[1], Hu Xueqing[1], Shi Yin[1], and Dai F F[2]

(1 Mixed Signal and High Speed Circuit Laboratory, Institute of Semiconductors, Chinese Academy of Science, Beijing 100083, China)
(2 Department of Electrical Computer Engineering, Auburn University, Auburn, Alabama 36849-5201, USA)

Abstract: This paper presents an LC VCO with auto-amplitude control (AAC), in which pMOS FETs are used, and the varactors are directly connected to ground to widen the linear range of K_{vco}. The AAC circuitry adds little noise to the VCO but provides it with robust performance over a wide temperature and carrier frequency range. The VCO is fabricated in a chartered 50GHz 0.35μm SiGe BiCMOS process. The measurements show that it has -127.27dBc/Hz phase noise at 1MHz offset and a linear gain of 32.4MHz/V between 990MHz and 1.14GHz. The whole circuit draws 6.6mA current from 5V supply.

Key words: tuner; receiver IC; LC VCO; auto amplitude control
EEACC: 1230B; 2570K
CLC number: TN75 **Document code:** A **Article ID:** 0253-4177(2006)07-1189-07

1 Introduction

In broadband communication systems, such as those in tuners for HDTV, DVB, or cable-modem applications, voltage control oscillator (VCO) circuits always influence the receiver performance dramatically. In such a receiver, double-conversion architecture is often employed[1]. As shown in Fig. 1, this kind of receiver structure first up-converts a channel from a broadband cable input signal (handling frequencies from 100MHz to 1GHz) to a higher constant IF, and then down-converts it directly to the base band frequency. Because of the system's wide band property, this receiver structure requires wide-tuning-range VCOs to cover all of the operation bands: the down-conversion stage needs a VCO which has a 1.1GHz carrier and a 50MHz tuning range; the up-conversion stage needs a VCO with a tuning range from 100MHz to 1GHz. This can be achieved by shunting several VCOs, each with a different carrier and about a 100MHz tuning range, or by implementing a switch resonant tank network.

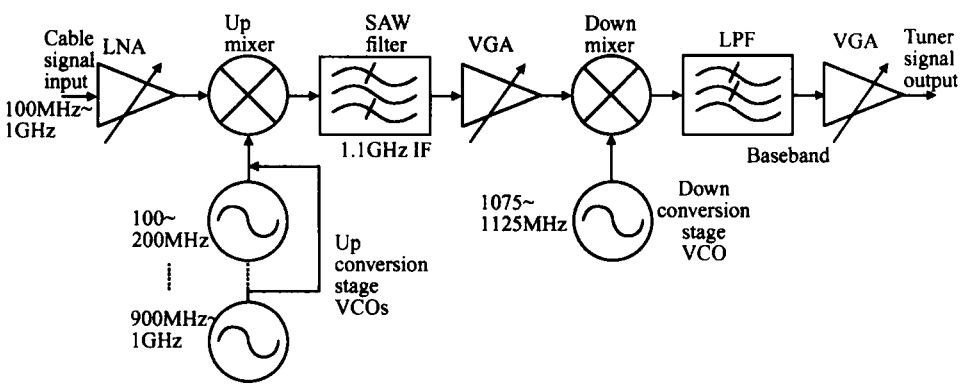

Fig. 1 Diagram of the tuner

* Project supported by the National Natural Science Foundation of China (No. 90207008)
† Corresponding author. Email: jyan@red.semi.ac.cn
Received 21 January 2006, revised manuscript received 4 April 2006

The higher the first IF, the smaller relative tuning range is required from the first LO source. In our system plan, the IF is 1100MHz, which allows us to use a readily available, low-cost SAW filter. Therefore VCOs with a tuning range over 10% are needed for this system. LC VCOs designed for this application have been widely studied and fabricated[1~6]. This paper presents another design of LC VCOs which uses pMOS FETs to get a wide tuning range and engages an auto-amplitude-control circuit to improve the phase noise performance, the ambient-proof characteristic over process, temperature, and frequency variation[7]. The AAC loop is carefully constructed with the fewest possible number of active components to prevent additional noise. The design and simulation of the LC VCO core, AAC loop, and VCO buffer will be discussed.

2 Circuit design and simulation

2.1 Design of pMOS LC VCO[8~13]

The design principles to get a VCO with a wide linear tuning range and low phase noise are described in detail as follows.

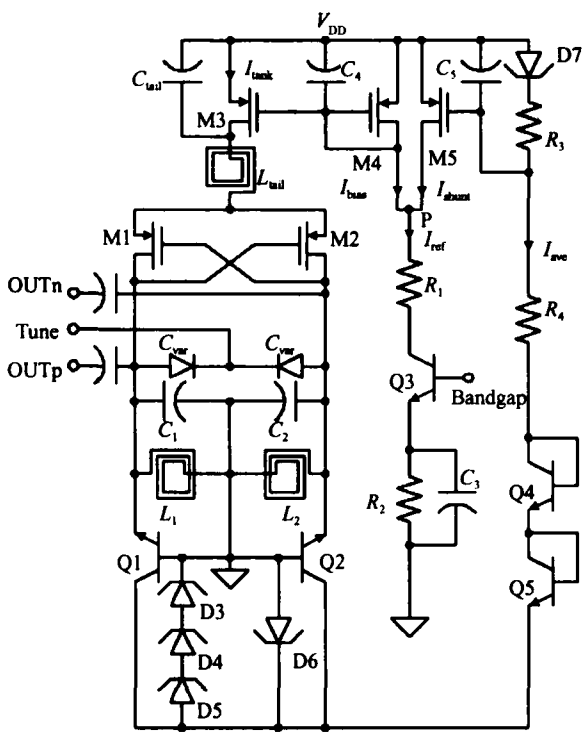

Fig. 2 Schematic of the VCO with AAC

2.1.1 Design of VCO core for high Q and low phase noise

(1) The flicker noise of active devices is due to the random trapping and releasing of charge by defects and impurities that lie in the semiconductor material. The mean-square $1/f$ noise current of a MOSFET is given by[14]

$$\overline{i_n^2} = \frac{K}{f} \times \frac{g_m^2}{WLC_{ox}^2} \times \Delta f \approx \frac{K}{f} \omega_T^2 A \Delta f \qquad (1)$$

where A is the area of the gate and K is a device-specific constant. K varies from process to process and even from run to run, but in the current processes, the K of pMOS is typically much smaller than that of nMOS. Therefore it is more promising to use pMOS rather than nMOS in VCO to reach a finer noise performance. pMOS also offers the advantage of higher output swing, so the phase noise due to the high flicker noise at frequencies below the corner frequency can be tolerated. This is due to the fact that pMOS transistors can operate in the triode region without affecting the VCO noise performance.

The pMOS FETs should be scaled according to the tail current to accommodate it with enough headroom. In a steady-state oscillation condition, $G_m R_p = 1$. To ensure start-up, $G_m R_p > 1$ is needed. When pMOS FETs operate in the saturated region, $G_m \propto W/L$. The pMOS size should be reasonably large in order for G_m to be large enough. Equation (1) shows that larger MOSFETs exhibit less $1/f$ noise, which is because their larger gate capacitances smooth the fluctuations of channel charge.

(2) For getting a tank with high Q, the width of the on-chip spiral inductor's track should be moderate, and the turns should be as few as possible to maximize the tank equivalent parallel resistance. The hole of the tank should be chosen as large as possible according to the chip area limits. In order to get an adequate tuning range and guarantee that the varactor capacitors but not the parasitic capacitors dominate, a large varactor is needed. However, for lower noise, a small varactor is preferred. Additionally, fixed capacitors are needed in the tank to ensure a stable oscillation frequency.

(3) The bias current for the tank should be large enough to minimize the phase noise. The swing will be maximized when the pMOS FETs are

made to alternate between the triode region and cut-off. When the VCO remains in the current-limit region, the amplitude is approximately

$$A = \frac{2}{\pi} I_{bias} R_p \quad (2)$$

where R_p is the equivalent parallel resistance of the tank. Once the pMOS FETs go into the triode region, the VCO will enter the voltage-limit region. Under this condition, raising the current will bring no further swing and even more phase noise and current waste.

(4) The inductor L_{tail} and the capacitor C_{tail} added to the tail current source form a tank filter which is designed to filter out noise from the bias circuitry[15]. Here L_{tail} and C_{tail} are chosen to be large in order to reject noise coming from the power supply as much as possible.

2.1.2 Design of VCO core for wide tuning range and linear gain

Since the varactors used in the tank should be high Q at the frequency of interest, pn junction varactors are more suitable than MOS varactors. However, a pn varactor has a parasitic substrate diode formed by the n side of the junction and the p type substrate, as shown in Fig. 3. Unless the n side of the diode is connected to ac ground, the parasitic devices will be included in the tank.

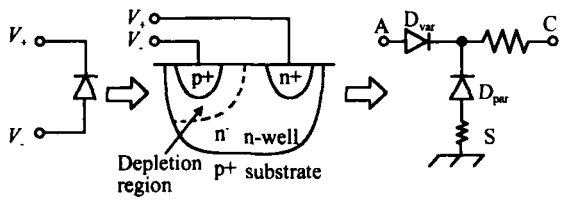

Fig. 3　pn varactor and parasitic diode

The C-V curve of the varactor is shown in Fig. 4. The linear section is where the varactor should operate. In the non-linear section, the tuning curve will bend and the noise contribution will increase significantly. The VCO tuning voltage V_{tune} must be higher than the potential of the varactor anode. Therefore, to get a wider tuning range and a better gain linearity, the anode of the varactor should be connected to the lowest potential of the circuit. In this design we use pMOS FETs, and thus the tank can be connected directly to ground.

2.2 AAC circuit design and analysis

An automatic-amplitude-control (AAC) circuit in the VCO can keep the VCO in the current-limit region to alleviate the amplitude noise and the AM to PM noise. It also makes the VCO ambient-proof and stabilizes its performance.

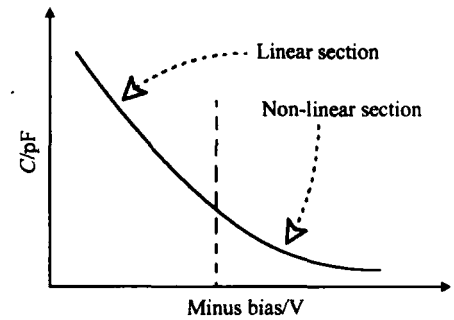

Fig. 4　Varactor capacitor versus tuning voltage

2.2.1 AAC feedback loop design

The AAC loop used in this design is shown in Fig. 2. The pMOS FETs M1 and M2 form a negative resistor across the LC tank. The pMOS FET M3 acts as a current source to draw current for the tank. M4 is connected as a diode to bias the tail current source M3. The reference current I_{ref} is set by biasing the base of Q3 with the bandgap voltage.

The sample transistors Q1 and Q2 are set to behave as a class C amplifier, which is then used to limit the swing of the oscillator to slightly more than one V_{BE}. They are normally set in the cut-off state when the oscillation amplitude is low. Once the amplitude gets close to V_{BE}, these transistors start to turn on slightly at the top or bottom of the oscillation swing and form the current I_{ave} flowing through R_3 and R_4. The potential across R_3 and R_4 invoked by this current will turn on pMOS FET M5 further. This will cause the shunt current to rise, and then the currents I_{bias} and I_{tank} will be cut down. According to Eq. (2), the swing amplitude will be pulled back to a value around V_{BE}. These steps will prevent pMOS FETs M1 and M2 from entering the triode region and ensure that the VCO always draws just enough current to turn on these limiting transistors. Turning on Q1 and Q2 strongly should be prevented; otherwise they will load the tank with their dynamic emitter resistance and de-Q the tank.

C_4 is included here to form a dominant and controllable pole in the AAC feedback loop so that the whole system is stable under all operating conditions. It also filters out the noise coming from the bias. Resistors R_3 and R_4 and diode D7 provide a dc

bias a little under V_{th} for the shunt branch pMOS FET M5, which will improve the sensitivity of the feedback loop. Schottky diodes D3 to D5 are used to confine V_{CE} of the transistors Q1 and Q2 within the breakdown voltage. They also provide bias for the AAC feedback loop. D6 is reversely connected to prevent Q1 and Q2 from deep saturation. That is to say, they prevent the CB junction from being negatively biased too far.

Adjusting the ratio of R_3 and R_4 can control the response sensitivity of the AAC feedback loop. In our design, the AAC loop feedback current I_{ave} is only 200μA. Thus it is a power saving scheme for amplitude controlling. Compared with previous works[7,16], this AAC loop is constructed with fewer active components so it introduces less noise from the bias circuit to the oscillation part and saves chip space at the same time.

2.2.2 AAC system analysis[16,17]

The point P shown in Fig. 2 acts as a summing node for the three currents I_{ref}, I_{shunt}, and I_{bias}. The VCO with the AAC feedback loop system can be conceptually drawn as shown in Fig. 5. The transfer function of the current mirror block can be written as

$$A_1(s) = \frac{I_{tank}}{I_{bias}} = \frac{\frac{g_{m3}}{C_4}}{s + \frac{g_{m4}}{C_4}} \tag{3}$$

Capacitor C_4 creates a dominant pole at $P_1 = g_{m4}/C_4$. When C_4 increases, the loop will be more stable but the control delay will increase.

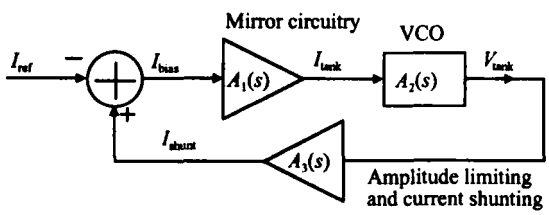

Fig. 5 Diagram of AAC feedback loop system

Note that Eq. (2) has its obvious limitations in determining the amplitude of the tank because it does not include the influence of frequency. For exact analysis, the oscillator should be treated as a resonator with a current pulse applied to the tank by M1 and M2 alternately in each equal half cycle. The second order transfer function can then be written as

$$V_{osc}(s) = \frac{2}{C_{var}} \times \frac{\omega}{(s + \frac{1}{R_p C_{var}})^2 + \omega^2} \tag{4}$$

where ω is approximately equal to the frequency of oscillation. From the above equation, the transient behavior of this circuit can be determined. The time constant $R_p C_{var}$ in Eq. (4) is equivalent to a pole in the response of the oscillation amplitude versus bias current. This pole can be added to Eq. (2) to describe the frequency response of the oscillation amplitude.

For the resonator block, the transfer function can be written as

$$A_2(s) = \frac{V_{tank}}{I_{tank}} = \frac{2}{\pi} \times \frac{\frac{1}{C_{var}}}{s + \frac{1}{R_p C_{var}}} \tag{5}$$

The pole can be written as a function of Q:

$$P_2 = \frac{1}{R_p C_{var}} = \frac{\omega_{osc}}{2Q} \tag{6}$$

Equation (6) shows the impact of the oscillator's behavior on the AAC loop. A tank with a higher Q will respond more slowly and therefore has a lower frequency pole than a lower Q oscillator. A high Q VCO will lead to a less stable loop because it has a greater phase shift at a lower frequency. Because the frequency of P_2 and the gain of $A_2(s)$ are set and are not allowed to be adjusted arbitrarily once the oscillator is settled according to the design requirements, the intrinsic sensitivity of the AAC loop is fixed.

When V_{tank} reaches V_{BE}, the limiting transistors Q1 and Q2 turn on and form narrow pulses with peak amplitude. The transfer function of the amplitude limiting block in Fig. 5 can be written as

$$A_3(t) = 2 \times \frac{\partial I_{shunt}}{\partial V_{tank}} = K\left(\frac{I_s(R_3 + \frac{1}{j\omega C_5}) e^{\frac{V_{tank}}{2v_T}}}{\sqrt{2\pi} \times \frac{V_{tank}}{2v_T}} + V_{D7} - V_{th}\right)(R_3 + \frac{1}{j\omega C_5})\left(\frac{I_s e^{\frac{V_{tank}}{2v_T}}}{\sqrt{\pi v_T V_{tank}}} - \frac{I_s e^{\frac{V_{tank}}{2v_T}}}{\sqrt{\pi v_T V_{tank}^3}}\right) \tag{7}$$

where $K = -4\mu_0 C_{ox} W/L$. This is a nonlinear transfer function. The pole created by C_4 is near the pole of the VCO core, so a resonance condition will easily occur. C_5 is introduced to this block to produce another pole that acts as the new dominant pole with a much lower frequency and pulls the original pole to a larger frequency and one zero that mini-

mizes the phase shift caused by the dominant pole at low frequencies. Thus we get two poles split far apart and a large phase margin. For a greater phase margin ,the loop gain can be adjusted by changing the gain $A_1(s)$ (by adjusting the ratio of M3 to M4) or $A_3(s)$ (by adjusting the size of limiting transistors Q1 and Q2). In any case, the gain should be kept high enough to settle the VCO amplitude at an exact and stable final value.

2.3 Differential VCO buffer

The VCO output buffer is constructed to be a differential pair amplifier. Just as Fig. 6 depicts ,Q5 and Q6 provide the bias tail current ,and Q1 and Q2 are the main amplifier pair. Q3 and Q4 form the cascode structure for isolating the VCO core from outside to avoid the influence of load and to prevent the pulling effect when the VCO is located on the same substrate as other high power blocks with close operation frequency.

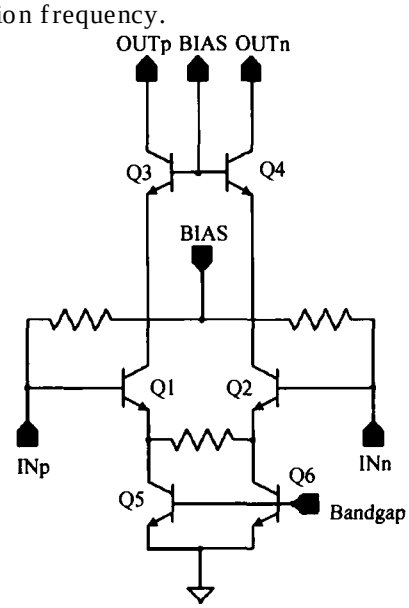

Fig. 6　Schematic of VCO buffer

3 Experimental results

Figure 7 shows the experimental phase noise value of the VCO with the AAC. At a 1MHz frequency offset ,a - 127. 27dBc/ Hz phase noise has been attained from a 1. 14GHz carrier. This result is measured using an Agilent E4440A spectrum analyzer. The experimental result is worse by about 3. 3dBc/ Hz than the simulation result (- 130. 6dBc/ Hz @1MHz when the carrier frequency is 1209MHz) .

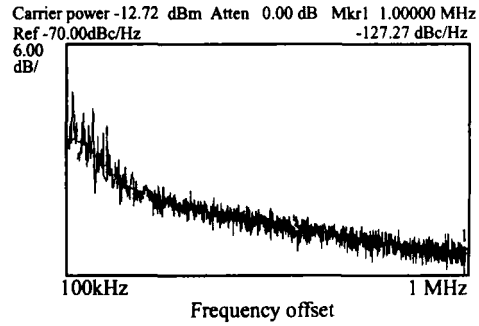

Fig. 7　Phase noise performance of VCO　Carrier frequency is 1. 14GHz.

Figure 8 shows the tuning curves and phase noise variation when V_{tune} is set from low to high. It can be seen that this VCO has a linear tuning range which covers the carrier frequency over a 100MHz tuning range (over 10 %) when V_{tune} varies from 0. 55 to 5. 237V. The gain is approximately 32. 4MHz/ V in the linear section (V_{tune} from 1. 5 to 5. 0V) . However ,the measured carrier frequency is lower than the design result by about 69MHz. This may be due to the parasitic parameters in the layout. Figure 8 also shows the AAC 's function of rejecting the change of phase noise. The experiment shows that with the carrier frequency varying from 990 to 1140MHz ,the phase noise changes by only a couple of dB.

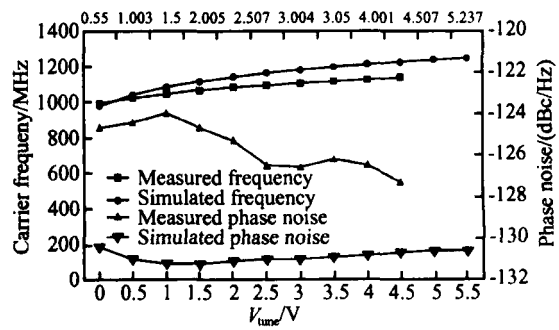

Fig. 8　Oscillation frequency and phase noise versus V_{tune}

Figure 9 shows the VCO phase noise versus the temperature. With the temperature varying from about 15 to 95 ℃,the phase noise only changes by less than 2dB. For the experiment condition limits ,the lower temperature performance cannot be presented ,and the 15 ℃temperature value is obtained by estimate.

Table 1 shows the similar work for the LC VCO. It can be seen from this table that this VCO design exhibits a good phase noise performance over a wide tun-

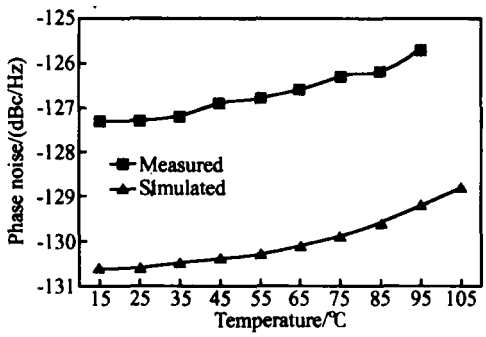

Fig. 9 Phase noise versus temperature (V_{tune} = 5V)

ing range and consumes less power. At the same time, this work of the VCO is the only one with an AAC and a robust, ambient-proof property.

Figure 10 is the die photo of the AAC VCO with buffer.

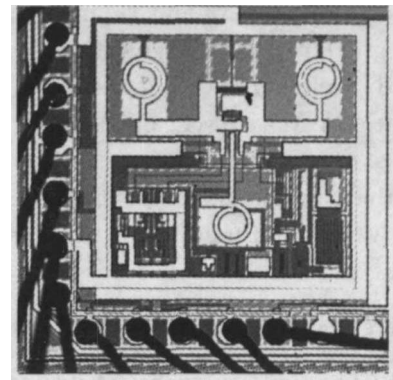

Fig. 10 Photomicrograph of the AAC VCO and buffer

Table 1 Comparison of tuner VCO performance

Reference	Phase noise	Tuning range	Current dissipation	Process technology
[8]	- 125.1dBc/ Hz @600kHz	1.79～2GHz/ VCO(10.5%)	19mA(1.8V supply)	0.65μm BiCMOS
[5]	- 133dBc/ Hz @1.45MHz About - 130dBc/ Hz @1MHz	About 890～1000MHz/ VCO(11%)	8mA(2.775V supply)	SiGe :C BiCMOS
[6]	- 126dBc/ Hz @1MHz	1580～1874MHz/ VCO(15.7%)	Not presented(5V supply)	0.9μm SiGe BiCMOS
[18]	- 78dBc/ Hz @10kHz About - 125dBc/ Hz @1MHz	1.32～1.9GHz/ VCO(31%)	13.5mA(3V supply)	0.35μm 27GHz SOI BiCMOS
This work	- 127.27dBc/ Hz @1MHz	990～1140MHz/ VCO(13.2%)	6.6mA(5V supply)	0.35μm 50GHz SiGe BiCMOS

4 Conclusion

This paper presents a 1.1GHz LC VCO with a low phase noise of - 127.27dBc/ Hz at 1MHz offset and with wide tuning range and linear tuning curve. It exhibits about 32.4MHz/ V linear gain from to 1140MHz. The phase noise is almost constant over a wide temperature and carrier frequency range. This optimized performance is due to the pMOS VCO structure design and the optimization of the AAC circuitry design which has been discussed in detail above. If we reconstruct the VCO resonant tank using this design to meet the lower frequency band, it will be adequate to get all the VCOs for a whole tuner receiver system to cover its entire operation frequency range.

References

[1] Samueli H. Broadband communication ICs: enabling high-bandwidth connectivity in the home and office. Proc International Solid-State Circuit Conference, 1999:26

[2] Stadius K, Halonen K. Wide-tuning-range dual-VCOs for cable-modem receivers. Proc IEEE Radio Frequency Integrated Circuits Symp, 2002:471

[3] Montemayor R. A 410mW 1.22GHz downconverter in a dual-conversion tuner IC for open cable applications. IEEE J Solid-State Circuits, 2004, 39:714

[4] Washio K, Okabe T. An all-band TV tuner IC with 10-GHz/ 100-V mixed analog/ digital Si bipolar technology. IEEE J Solid-State Circuits, 1992, 27:1034

[5] Antoine P, Bauser P, Beaulaton H, et al. A direct-conversion receiver for DVB-H. IEEE J Solid-State Circuits, 2005, 40: 2536

[6] Stadius K, Malinen A, Jarvio P, et al. A cable-modem RF tuner. IEEE ESSCIRC, 2003

[7] Rogers J, Rahn D, Plett C. A 2.4GHz wide tuning range VCO with automatic level control circuitry. IEEE Solid-State Circuit Conference, 2001:341

[8] Muer B D, Borremans M, Steyaert M. A 2-GHz low-phase-noise integrated LC-VCO set with flicker-noise upconversion minimization. IEEE J Solid-State Circuits, 2000, 35:1264

[9] Hegazi E. Varactor characteristics, oscillator tuning curves, and AMCFM conversion. IEEE J Solid-State Circuits, 2003, 38:1033

[10] Rogers J W M, Dai F F, Cavin M S. A multiband Delta sigma fractional-N frequency synthesizer for a MIMO WLAN transceiver RFIC. IEEE J Solid-State Circuits, 2005, 40:678

[11] Levantino S, Samori C, Bonfanti A. Frequency dependence on bias current in 5-GHz CMOS VCOs: impact on tuning range

and flicker noise upconversion. IEEE J Solid-State Circuits, 2002, 37: 1003
[12] Hajimiri A, Lee T H. Design issues in CMOS differential LC oscillators. IEEE J Solid-State Circuits, 1999, 34: 717
[13] Ham D, Hajimiri A. Concepts and methods in optimization of integrated LC VCOs. IEEE J Solid-State Circuits, 2001, 36: 896
[14] Lee T H. The design of CMOS radio-frequency integrated circuits. Cambridge University Press, 1998
[15] Hegazi E, Sjoland H, Abidi A. A filtering technique to lower LC oscillator phase noise. IEEE J Solid-State Circuits, 2001, 36: 1921
[16] Rogers J W M, Rahn D, Plett C. A study of digital and analog automatic-amplified control circuitry for voltage-controlled oscillators. IEEE J Solid-State Circuits, 2003, 38: 352
[17] Rogers J, Plett C. Radio frequency integrated circuit design. Artech House, Inc, 2003
[18] Ling C, Montemayor R, Cicalini A, et al. A low-power integrated tuner for cable telephony applications. IEEE J Solid-State Circuits, 2002, 37: 1757

为调谐器设计的带自动幅度控制 1.1GHz 差分压控振荡器*

颜　峻[1,†]　毛　威[1]　马德胜[1]　顾　明[1]　许奇明[1]　胡雪青[1]　石　寅[1]　代　伐[2]

(1 中国科学院半导体研究所 混合信号与高速电路实验室，北京　100083)
(2 奥本大学电子与计算机工程系，亚拉巴马州　36849-5201，美国)

摘要：为集成调谐器接收机芯片系统设计了一个带自动幅度控制回路的差分结构电容电感压控振荡器.通过采用 pMOS 管作为有源负阻使振荡器谐振回路可以直接接地电平,减小了寄生效应,扩大了频率调谐的线性及其范围.采用的自动幅度控制 AAC 回路具有元件少,噪声低,控制灵敏,调节容易,结构简单及设计方便的优点,并保证振荡器电路的性能最小地依赖于环境和制造工艺参数的变化.所设计的压控振荡器采用新加坡特许 50GHz 0.35μm SiGe BiCMOS 工艺流片,经测试在 1MHz 频率偏移处达到了 -127.27dBc/Hz 的相位噪声性能,具有宽的(990～1140MHz)和线性(调谐增益 32.4MHz/V)的频率调谐曲线.整个振荡器电路在 5V 的供电电压下仅消耗 6.6mA 的电流,可以满足调谐器的应用需要.

关键词：调谐器；集成接收机芯片；电容电感压控振荡器；自动幅度控制
EEACC：1230B；2570K
中图分类号：TN75　　**文献标识码**：A　　**文章编号**：0253-4177(2006)07-1189-07

*国家自然科学基金资助项目(批准号:90207008)
†通信作者. Email: jyan@red.semi.ac.cn
2006-01-21 收到,2006-04-04 定稿