A Wide-Band High-Linearity Down-Conversion Mixer for Cable Receptions*

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Abstract: We analyze a wide-band, high-linearity down-conversion mixer for cable receptions that is implemented in 0.35μm SiGe BiCMOS technology. The bandwidth of the RF (radio frequency) input covers the range from 1 to 1.8GHz. The measured input power at the -1dB compression point of the mixer reaches +14.23dBm. The highest voltage conversion gain is 8.31dB, while the lowest noise figure is 19.4dB. The power consumed is 54mW with a 5V supply. The test result of the down-conversion mixer is outlined.

Key words: BiCMOS; wide band; linearity; down conversion; mixer; SiGe
EEACC: 1205; 1290; 2570K
CLC number: TN77　　**Document code:** A　　**Article ID:** 0253-4177(2006)07-11559-05

1 Introduction

Nowadays, mobile electronic equipments, including wireless LANs, mobile phones, and televisions, are becoming more popular. In these equipments, the RF front-end is one of the most important devices for communication. For most applications, such as wireless LANs, a narrow-band RF front-end is enough, which is normally below 20MHz. However, wide-band applications such as wide-band tuners for TVs and GPS (global position system) are becoming more popular, which require bandwidths above 100MHz. In these applications, wide bands and high linearity are required.

The mixer is one of the most important components in RF front-end devices, whose function is to convert the frequency of the signals. Most mixers are designed as Gilbert cells. The band-width of the mixers is narrow because of the inductors and capacitors in the signal path. The linearity of the mixers is limited by the inductors and capacitors in the degeneration path of the input stage. Therefore the normal Gilbert cells are not suitable for wide-band applications.

This paper analyzes the design of a wide-band, high-linearity down-conversion mixer for cable receptions with an input bandwidth of 800MHz. The cable reception employs a dual-conversion architecture, which has an up-conversion mixer to raise the frequency and a down-conversion mixer to lower the frequency. Therefore the input frequency of the down-conversion mixer covers the range from 1 to 1.8GHz. The down-conversion mixer introduced in this paper employs no inductors or capacitors to enlarge the bandwidth. The measured -1dB compression point can reach +14.23dBm, while the third-order intercept point (IIP3) is +23.87dBm. The test highest voltage conversion gain is 8.31dB, while the lowest noise figure is 19.4dB, with a power consumption of 54mW.

2 Analysis of the circuit

2.1 Architecture of the circuit

Figure 1 shows the architecture of the circuit. When designing the down-conversion mixer, the size and the collector current of the switch transistors (Q3, Q4, Q5, Q6) should be set carefully to reduce the noise figure at the point where the transistor can achieve a highest f_t when the collector current is supplied. After setting the size of the switch transistors, the size of the input stage transistors should be set at 6～8 times as large as the

* Project supported by the National Natural Science Foundation of China (No. 90207008)
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Received 23 February 2006, revised manuscript received 17 March 2006
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switch transistors to improve the linearity. Then the trade-off among linearity, noise figure, and conversion gain should be made by adjusting the current and the resistors.

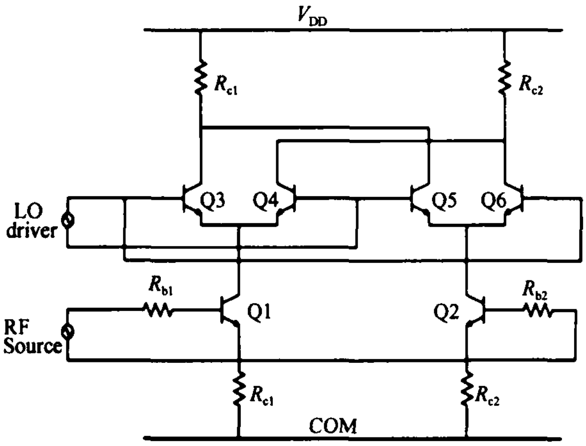

Fig. 1 Architecture of the down-conversion mixer

In a traditional Gilbert cell, the input stage of the mixer restricts the bandwidth and linearity of the whole mixer because of the LC matching net, which is composed of degeneration inductors and capacitors. Eliminating the LC effect is an effective way to enlarge the bandwidth of the input stage and improve the linearity. As shown in Fig. 1, the LC matching net is replaced with the emitter degeneration resistors in the input stage for the wide-band match. The input impedance increases because of the resistors R_{e1} and R_{e2}. Therefore if the input source, such as an LNA (low noise amplifier), has a low output impedance, the wide-band match is realized by the high input impedance driven by the low source impedance. In most situations, the source impedance is low enough to satisfy the condition of low source impedance.

The reason for adding the degeneration resistors and the attenuation resistors at the input transistors base is also to keep the conversion linearity. The disadvantage is that they increase the noise figure and reduce the voltage gain. Therefore the rest of the paper uses the basic mixer architecture to analyze the impact of the degeneration resistors R_{e1} and R_{e2} and the attenuation resistors R_{b1} and R_{b2}.

2.2 Linearity analysis

The most important contributions to the linearity come from the degeneration resistors and the attenuation resistors in this mixer. The presented linearity analysis is valid for small signals. Accurate linearity analysis can be obtained using techniques such as Volterra series[1].

In this analysis, the third-order intercept point (IP3) is used to scale the linearity of the mixer. Any nonlinear transfer function can be written as a series expansion of power terms[1]:

$$v_{out} = k_0 + k_1 v_{in} + k_2 v_{in}^2 + k_3 v_{in}^3 + \cdots \quad (1)$$

The input voltage at the third-order intercept point is used to discuss the linearity in this paper. The relation between the coefficients in Eq. (1) with the input voltage at the third-order intercept point is as follows[1]:

$$v_{IP3} = 2\sqrt{\frac{k_1}{3k_3}} \quad (2)$$

We analyze the single-side input stage. First, the coefficients k_1 and k_3 should be determined by the model. The output voltage is proportional to v_{be}. The expression for v_{be} can be obtained from the small signal model (Fig. 2) as follows [1]:

$$\begin{aligned} v_{be} &= V_T \ln\left(1 + \frac{i_c}{I_c}\right) \\ &= V_T\left[\frac{i_c}{I_c} - \frac{1}{2}\left(\frac{i_c}{I_c}\right)^2 + \frac{1}{3}\left(\frac{i_c}{I_c}\right)^3 \cdots\right] \quad (3) \end{aligned}$$

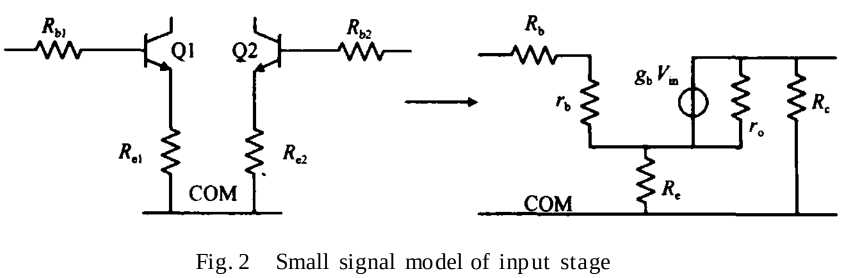

Fig. 2 Small signal model of input stage

The expression of i_c can be obtained from the small signal model. Then the coefficients k_1 and k_3 can be calculated:

$$k_1 = \frac{1}{R_e + \frac{R_b}{\beta} + r_e} \quad (4)$$

$$k_3 = \frac{1}{(R_e + \frac{R_b}{\beta} + r_e)^4} \times \left[\frac{r_e^2}{2 I_c^2 (R_e + \frac{R_b}{\beta} + r_e)} - \frac{r_e}{3 I_c^2}\right] \tag{5}$$

Here r_e represents the emitter impedance of the bipolar transistor. The coefficients k_1 and k_3 in Eq. (2) are replaced by Eqs. (4) and (5), respectively. The input voltage at the third-order intercept point is achieved.

$$v_{IP3} = 2\sqrt{2} V_T \left(\frac{R_e + \frac{R_b}{\beta} + r_e}{r_e}\right)^{\frac{3}{2}} \tag{6}$$

For the differential input stage, the input voltage at the third-order intercept point has an extra factor of 2. The result shows that the degeneration resistor R_e and the attenuation resistor R_b can improve the linearity dramatically.

2.3 Voltage conversion gain analysis

The voltage conversion gain of the mixer is decided by the input stage. Therefore the analysis of the voltage gain is focused on the input stage. Three equations follow from the small signal model (Fig. 2):

$$i_e R_e + i_b r_b + i_b R_b = V_i \tag{7}$$

$$i_c \frac{r_o R_c}{r_o + R_c} = V_o \tag{8}$$

$$i_b + g_m i_b r_b = i_e + i_c \tag{9}$$

Here i_e, i_b, and i_c stand for the emitter current, the base current, and the collector current of the transistor, respectively; and R_b, R_e, and R_c stand for the attenuation resistor, degeneration resistor, and the load resistor, respectively; V_i is the input voltage and V_o is the output voltage. The output resistance of the transistor r_o is ignored because it is too large. The voltage gain can then be achieved from the three equations.

$$A_v \approx \frac{\beta R_c}{\beta R_e + R_b + r_b} \tag{10}$$

The result shows that both the degeneration resistor and the attenuation resistor reduce the voltage gain.

2.4 Noise figure analysis

The noise of the mixer comes from the switch transistors, input stage, and other factors. We will discuss the noise in the input stage now because the degeneration and attenuation resistors are included in the input stage. The input stage noise is composed of four sources (Fig. 3): the base noise $\overline{v_b^2}$ and $\overline{i_b^2}$; the emitter noise $\overline{v_e^2}$; and the collector noise $\overline{i_c^2}$. The attenuation resistor and degeneration resistor contribute to the noise in the base noise voltage $\overline{v_b^2}$ and the emitter voltage noise $\overline{v_e^2}$:

$$\overline{v_b^2} = 4 KTR_b \Delta f \tag{11}$$

$$\overline{v_e^2} = 4 KTR_e \Delta f \tag{12}$$

The equations show how much voltage noise the attenuation resistor and the degeneration resistor produce.

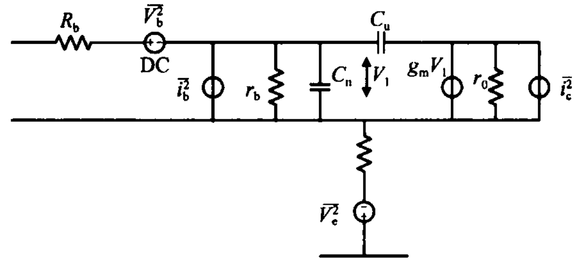

Fig. 3　Noise model of input stage

2.5 Summary

The results show that the degeneration and attenuation resistors can improve linearity dramatically while the voltage gain and the noise figure are affected by these resistances. In most situations, the gain and the noise figure of the LNA determine the gain and the noise figure of the RF front-end. Thus the gain and the noise figure of the mixer are not important if the gain of the LNA is big enough. In the wide-band applications, the most critical characteristic of the mixer is linearity. Thus adding the degeneration and attenuation resistors to improve the linearity is feasible.

3 Test results of the wide-band high-linearity mixer

A wide-band high-linearity down-conversion mixer using degeneration and attenuation resistors is designed in 0.35μm SiGe BiCMOS technology. The heterogeneous junction between silicon and germanium reduces the noise figure. Therefore SiGe is one of most popular materials used to design RF front-ends. BiCMOS technology is used because the bipolar transistors in the technology have high f_t, which can improve the performance of the device in high frequency situations. The die of the whole front-end is fabricated in the Chartered manufactory.

In the experiment, the down-conversion mixer has an RF input bandwidth from 1 to 1.8GHz that is generated from an Agilent signal generator E8257D. A 900MHz sine wave signal is used as the LO (local oscillator) frequency from the output of an Agilent E8362B network analyzer. Then the intermediate frequency can cover a range from 100 to 900MHz.

3.1 Linearity test

The -1dB compression point is tested to express the linearity instead of the third-order intercept point (IP3) because of the experimental equipment. The output power is gotten from an Agilent E4440A spectrum analyzer. Figure 4 shows that the input power at the -1dB compression point is +14.23dBm. That means the input power at the IP3 is +23.83dBm[1]. The linearity of this mixer is high enough to be applied in cable reception.

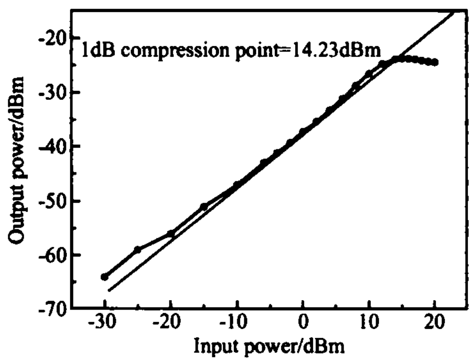

Fig.4 Test result of -1dB compression point

3.2 Conversion gain test

The output power can be gotten from the spectrum analyzer, and the conversion gain can be calculated. Figure 5 shows that the voltage conversion gain is 8.31dB at 100MHz. The conversion gain is reduced along with the frequency. The reason for the reduction is the parasitic effect of the bipolar transistor at high frequency. Since the voltage conversion gain of the mixer is not critical, the conversion gain of the mixer used in this paper is high enough.

3.3 Noise figure test

The experiment shows that the lowest noise figure in the whole band is about 19.4dB. In the RF front-end, the noise of the mixer is not important. The noise factor of components in series is:

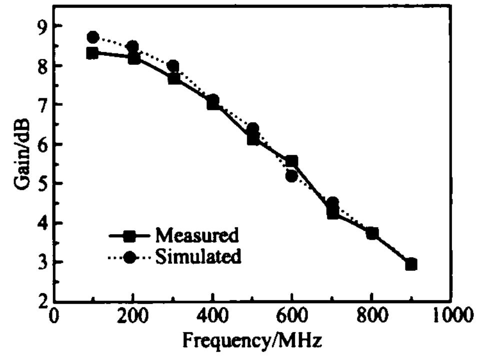

Fig.5 Test result of voltage conversion gain

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots \qquad (13)$$

As shown in Eq. (13), the noise of the LNA, which is the first stage in the RF front-end, determines the noise factor of the whole system. Generally, the gain of the LNA is large. For example, in some wide-band tuner systems, the LNA can produce a gain of 20 to 25dB. Thus the mixer mentioned in this paper contributes no noise to the whole system.

4 Conclusion

In this paper, we have analyzed a wide-band, high-linearity down-conversion mixer. Table 1 lists the parameters of the mixer. As shown in the table 1, the degeneration resistors and the attenuation resistors improve the linearity dramatically and have little influence on the conversion gain and the noise figure. The die area displayed in Fig. 6 is 0.45mm × 0.47mm.

Table 1 Performance of the wide-band mixer

Parameter	This work	Other work[2]
Intermediate frequency bandwidth/MHz	800	360
Voltage conversion gain(max)/dB	8.31	8.7
Noise figure(min)/dB	19.4	9.8
Input power at -1dB point/dBm	+14.23	-10
Technology	0.35μm/SiGe BiCMOS	SiGe BJT

The advantage of this mixer is that the fixed attenuation impedance has become an alterable impedance. The alterable impedance can change the attenuation coefficient according to the input signal. Therefore the voltage conversion gain is alterable according to the input signal, and it also can be improved.

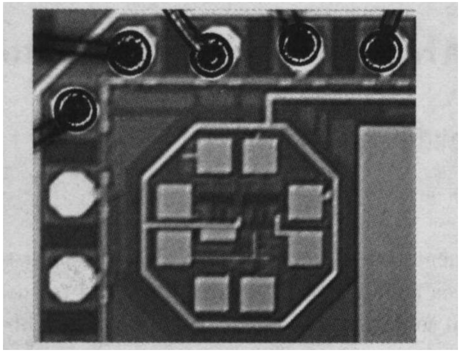

Fig. 6　Die photograph of the wide-band high-linearity mixer

Acknowledgement　The authors gratefully acknowledges the guidance of Yan Jun in implementing these concepts in a practical monolithic context.

References

[1]　Rogers J , Plet C. Radio frequency integrated circuit design. Artech House ,INC ,2003
[2]　Otaka S ,Ashida M ,Ishii M ,et al. A +10-dBm IIP3 SiGe mixer with IM3 cancellation technique. IEEE J Solid-State Circuits ,2004 ,39 (12) :2333
[3]　Razavi B. RF microelectronics. Pearson Education , INC , 2003
[4]　Gray P R , Hurst P J ,Lewis S H ,et al. Analysis and design of analog integrated circuits. John Wiley & Sons ,INC ,2001

一种用于有线接收机的宽带高线性度的下变频混频器 *

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摘要: 分析了一种宽带高线性度的用于有线接收机的下变频混频器. 该设计采用 0.35μm SiGe BiCMOS 工艺. 射频输入信号频率范围设计为 1～1.8GHz ,测得的 1dB 压缩点达到 +14.23dBm ,最大转换增益为 8.31dB ,最小噪声系数为 19.4dB ,在 5V 供电情况下,直流功耗为 54mW.

关键词: BiCMOS; 宽带; 线性度; 下变频; 混频器; SiGe
EEACC: 1205; 1290; 2570K
中图分类号: TN77　　**文献标识码**: A　　**文章编号**: 0253-4177(2006)07-1159-05

* 国家自然科学基金资助项目(批准号:90207008)
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2006-02-23 收到,2006-03-17 定稿
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