A 162GHz Self-Aligned InP/InGaAs Heterojunction Bipolar Transistor*

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Abstract: An emitter self-aligned InP-based single heterojunction bipolar transistor with a cutoff frequency (f_T) of 162GHz is reported. The emitter size is 0.8μm × 12μm, the maximum DC gain is 120, the offset voltage is 0.10V, and the typical breakdown voltage at I_C = 0.1μA is 3.8V. This device is suitable for high-speed low-power applications, such as OEIC receivers and analog-to-digital converters.

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1 Introduction

InP/InGaAs HBTs have many advantages for high-speed and low power applications owing to the excellent properties of InP and InGaAs material[1]. Compared to double-heterojunction bipolar transistors (DHBT), single heterojunction bipolar transistors (SHBTs) have higher speed and a simpler epitaxy layer structure since SHBTs do not need complex collector layers to overcome the current blocking effect at the base-collector junction[2]. Some researches on InP/InGaAs HBT have been done. For example, a self-aligned InP/InGaAs SHBT using a T-shaped emitter was reported by Su *et al*[3]. In that work, the current gain cutoff frequency is 85GHz, and the maximum oscillation frequency of the device is 72GHz. In addition, an InP/$GaAs_{0.5}Sb_{0.5}$/InP DHBT with a cutoff frequency(f_T) higher than 100GHz was reported by Xu and Watkins[4].

In this paper, an emitter self-aligned InP-based SHBT with f_T of 162GHz is reported, and the maximum oscillation frequency (f_{max}) at the collector current I_C = 34.2mA is 52GHz. The emitter size is 0.8μm × 12μm. The maximum DC gain is 120. The offset voltage is 0.10V.

2 Design and fabrication

One of the key points for enhancing the operation speed of InP HBTs is minimizing the parasitic effects of the devices by using advanced fabrication technology. Various technologies for fabricating InP HBTs with self-aligned structures have been proposed to reduce the parasitic resistance and capacitance. Among them, self-aligned HBTs with a base-metal overlaid structure are often used. However HBTs with rectangular emitters, using this technology, suffer from a possible short circuit between the base and the emitter. Therefore, hexagonal emitters were proposed by Matsuoka *et al*.[5].

In this work, self-aligned technology with a base-metal overlaid structure is used, and the emitters are designed to be hexagonal. In order to minimize the base collector capacitance, the width of the base is designed to be only 1μm. The fabrication process is as follows.

The epitaxial layers were grown on Fe-doped semi-insulating InP (100) substrates by MBE. The layer structure is listed in Table 1. Silicon is used as the n-type dopant, and beryllium (Be) is used as the p-type dopant. The emitter contact layer and sub-collector layer are both InGaAs, and they

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Table 1 Layer structure of the InP SHBT

Layer	Thickness/nm	Dopant	Doping/cm^{-3}
$In_{0.53}Ga_{0.47}As$	150	Si	1×10^{19}
InP	50	Si	1×10^{19}
InP	70	Si	3×10^{17}
$In_{0.53}Ga_{0.47}As$	5	undoped	—
$In_{0.53}Ga_{0.47}As$	50	Be	3×10^{19}
$In_{0.53}Ga_{0.47}As$	300	Si	1×10^{16}
$In_{0.53}Ga_{0.47}As$	50	Si	1×10^{19}
InP	20	Si	1×10^{19}
$In_{0.53}Ga_{0.47}As$	400	Si	1×10^{19}
Fe-doped semi-insulating InP (100) substrate			

are highly doped with a concentration of 1×10^{19} cm^{-3} to reduce the contact resistivity of the electrodes. A 120nm thick InP layer is grown as the emitter layer. The base layer is InGaAs with a thickness of 50nm and a p-type carrier concentration of $3\times10^{19}cm^{-3}$. A 5nm un-doped InGaAs layer between the emitter and the base is for stopping the diffusion of Be impurity from the base to the emitter. Just as in conventional InP based SHBTs, InGaAs is used for both the base and the collector in this work. This enhances the speed of the InP SHBT, but the narrow energy band-gap of InGaAs gives rise to a poor collector breakdown voltage.

It is well known that the selective wet etching of InP by HCl：H_3PO_4 shows strong anisotropic effects[6]. The etching rate is higher in crystal directions parallel to [001] and [010] than other directions. The lack of undercut under the emitter edges parallel to the $[01\bar{1}]$ direction makes self-aligned structures impossible without massive over etching[7]. The etching rate in directions parallel to [001] and [010] is so high that it is fatal to narrow emitter HBTs. Only in the direction parallel to [011] is the etching rate appropriate and the best undercut shape can be made. Thus it is wise to use the direction parallel to [011] as the major self-aligned direction. However, the shape of the undercut under a mask depends strongly on the etching time. According to the experimental results, the etching times of the InGaAs contact layer and the InP emitter layer are 120 and 20s, respectively, just as shown in Fig. 1. In order to eliminate short circuits in other directions between the base and the emitter, the mask is designed to be hexagonal[8].

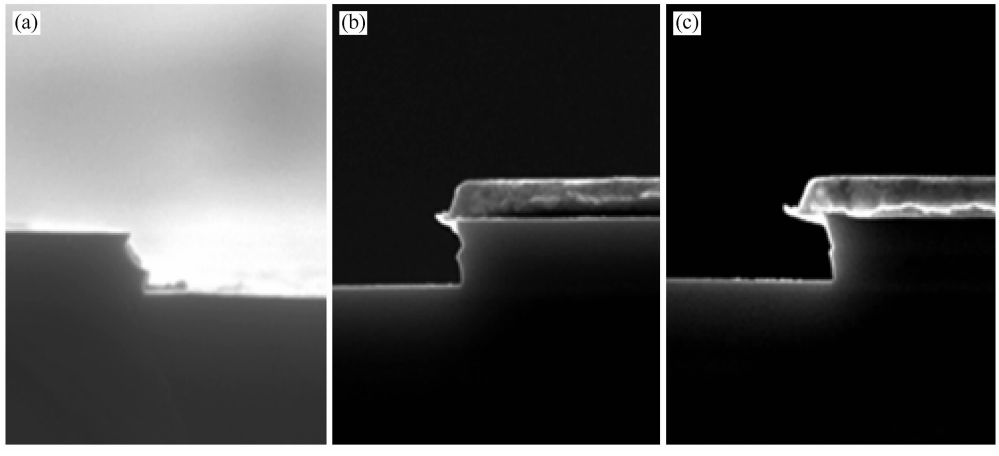

Fig. 1　SEM pictures of a transistor profile after laterally etching InGaAs and InP with different etching times
The test structure is parallel to the [011] direction. Etching times of InGaAs and InP in Figs. 1(a)～(c) are 160s/10s, 80s/61s, and 120s/20s, respectively. We use the etching time of 120s/20s, as in Fig. 1(c).

The devices are fabricated using a standard mesa process with wet chemical etching and contact photolithography. The fabrication process starts with the formation of the $1\mu m\times12\mu m$ emitter electrodes on the top InGaAs layer with photolithography and lift-off techniques. The emitter electrodes are used as a mask for emitter mesa etching. Selective wet etching is used to form an appropriate undercut around the emitter mesa and to reveal the base layer. The lateral etching is about $0.1\mu m$ on each edge parallel to the [011] direction, so the intrinsic emitter width is about $0.8\mu m$. The base metal of Ti/Pt/Au is then evaporated over the base region, including the entire e-

mitter metal, thus forming the base metal overlaid structure. Owing to the undercut of the emitter electrode, the base electrode, emitter mesa, and emitter electrode are all self-aligned without any short-circuit. The extrinsic base resistance is reduced greatly compared to un-self-aligned InP HBTs. Base and collector layers are also etched by wet etching. Then the sub-collector layer is etched until the semi-insulating InP substrate is revealed. After Ti/Pt/Au metal for collector ohmic contact is evaporated and lifted-off, an inter-connection metal is formed to connect the electrodes of the transistors to pads. In order to avoid the break of the metal at the edge of the emitter electrodes, air-bridges are used. A scanning electron micrograph (SEM) image of the device is shown in Fig. 2.

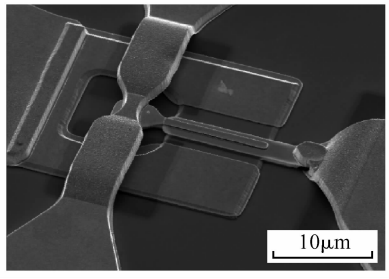

Fig. 2 SEM image of the 0.8μm×12μm InP SHBT

3 Results

The common emitter output characteristics are shown in Fig. 3, where the collector-emitter offset voltage is approximately 0.1V, the knee voltage is 0.42V at I_C = 23mA, and the common emitter breakdown voltage is 3.8V. A typical Gummel plot of this device is shown in Fig. 4. The DC gain increases as the I_C increases, and the gain reaches the maximum value of 120 at I_C = 40mA. The base and collector current ideality factors are 1.41 and 1.43 at low V_{BE}, respectively. The ideal factors increase at higher V_{BE}, and that of the base even almost reaches 2.

The RF performance of the InP/InGaAs HBTs is characterized with an HP8510C network analyzer. The current gain and the maximum stable/available gain (MSG/MAG) for the 0.8μm×12μm HBT are shown in Fig. 5. From the *S*-parameter measurements, the extrapolated current gain cutoff frequency f_T is 162GHz, and the maximum oscillation frequency f_{max} is 52GHz. f_T and

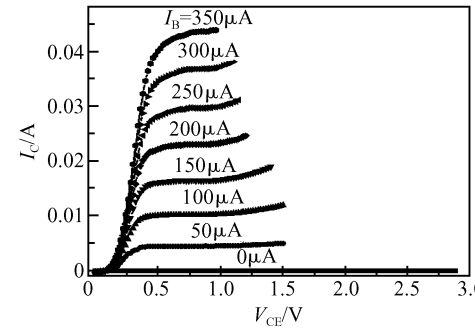

Fig. 3 Collector *I-V* characteristics of 0.8μm×12μm InP SHBT

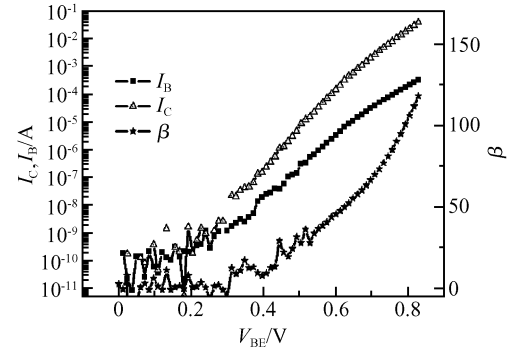

Fig. 4 Measured Gummel plot of base, collector current and current gain as function of V_{BE}

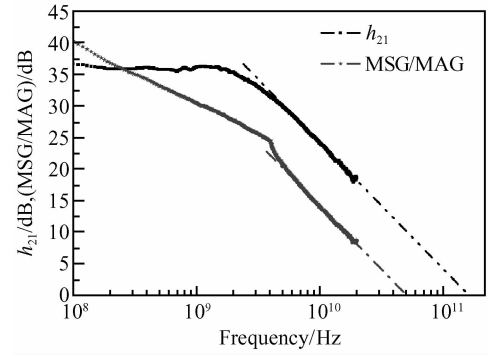

Fig. 5 Current gain, maximum stable/available gain at I_C = 20.4mA, V_{CE} = 0.85V

f_{max} reach their maximum values at I_C = 34.2mA, as shown in Fig. 6.

4 Discussion

The ideality factors reflect the surface recombination of the base. The recombination on the surface of extrinsic base is decided by one or both of the following two factors: surface recombination velocity and availability of minority carriers in the extrinsic base. If the surface recombi-

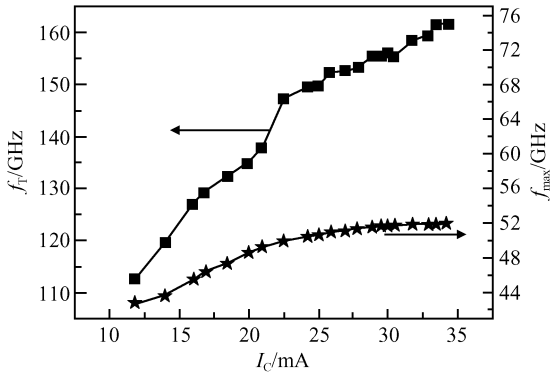

Fig. 6　Measured f_T and f_{max} as a function of collector current I_C

nation is limited by the first factor, the current has an ideality factor of two. Otherwise, the ideality factor is one. When V_{BE} is small, both factors contribute to the recombination, but at high V_{BE}, there are enough electrons diffused to the extrinsic base, and a low surface recombination velocity of InGaAs material limits the surface recombination. The ideality factor approaches two[9].

According to Eq. (1), f_T shows an increasing trend when C_{BC} is reduced. In this work, the base width is only 1μm wide (two fingers). This reduces the base collector capacitance C_{BC}, so a high f_T is achieved[1].

$$f_T = \frac{1}{2\pi}\left[\frac{\eta kT}{qI_C}(C_{je} + C_{BC}) + \frac{X_B^2}{\nu D_n} + \frac{X_{dep}}{2v_{sat}} + (R_E + R_C)C_{BC}\right]^{-1} \quad (1)$$

As shown in Fig. 5, the f_{max} is about 100GHz lower than f_T. f_{max} is described by the equation $f_{max} = \sqrt{f_T/(8\pi r_B C_{BC})}$[1]. The base resistance is[1]

$$r_b = \frac{1}{2} \times \frac{\sqrt{R_{SHB}\rho_B}}{L_B}\coth(W_B\sqrt{R_{SHB}/\rho_B}) + \frac{1}{2}R_{ex(epi)} + \frac{1}{2}R_{Bi(tvs)} + \frac{1}{2}R_{BM} \quad (2)$$

where R_{SHB} is the base sheet resistance, ρ_B is the specific contact resistance of the base metal-semiconductor contact, $R_{ex(epi)}$, $R_{Bi(tvs)}$, R_{BM} are the extrinsic base resistance, base contact resistance, and base metal resistance, respectively, L_E is the length of the base, and W_B is the width of the base. The measured specific contact resistance of the base metal-semiconductor contact is $2.4 \times 10^{-6}\Omega \cdot cm^2$, so the base contact resistance $R_{Bi(tvs)}$ is about 12Ω. Because self-aligned technology is used, $R_{ex(epi)}$ is about 1.1Ω according to the equation $R_{ex(epi)} = \rho_B S_{BE}/X_B L_B$ (where ρ_B, S_{BE}, X_B, L_B are the resistivity of the extrinsic base layer, the base emitter contact spacing, the base thickness, and the base length, respectively). The base metal resistance is only about 0.14Ω, so it can be neglected. The first part of Eq. (2) is 22.5Ω where the sheet resistance of the base measured by the transmission line structure is 1255$\Omega/\square$. Compared to the values reported for InP/InGaAs HBTs, $R_{ex(epi)}$ is smaller when the self-aligned technology is used, and the sheet resistance of the base is too high. Such a high base resistance leads to a very low f_{max} according to the equation $f_{max} = \sqrt{f_T/(8\pi r_B C_{BC})}$.

The high base sheet resistance might be due to the base layer structure and dopant. Just as shown in Table 1, Be is used as the dopant of the base. Since the diffusivity of Be is relatively high, Be diffuses from the base region into the emitter region during the growth. Redistribution of the base dopant can cause severe degradation of the HBT characteristics by decreasing the injection efficiency and increasing the recombination current at the base-emitter interface[10]. Therefore an un-doped $In_{0.53}Ga_{0.47}As$ layer is grown between the emitter and base to stop the diffusion of Be impurities. During the fabrication process, the base electrodes are evaporated on the un-doped layer after etching the emitter. This leads to a high base resistance. Compared to Be, carbon has higher acceptor efficiency and low diffusivity[11]. Using carbon as the p-type dopant of the base, the un-doped layer is not needed to stop the diffusion. The net hole concentration of a carbon-doped InGaAs base can be as high as 2×10^{20} cm^{-3}[12], which is much higher than that of a Be-doped base. Therefore, a carbon-doped InGaAs base can solve the problem of high base resistance, and a higher f_{max} could be expected.

5　Summary

InP HBTs with a high cutoff frequency are fabricated using a conventional wet chemical etching process. Because the base is narrow, which reduces base-collector capacitance, the cutoff frequency of the InP/InGaAs SHBT is 162GHz. The self-aligned technology reduces the extrinsic base resistance greatly. But the very high base sheet re-

sistance leads to small f_{max}, which is only 52GHz. A structure with a carbon-doped base layer will be helpful to improve f_{max}.

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162GHz 自对准 InP/InGaAs 异质结双极型晶体管*

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摘要： 报道了发射极自对准的 InP 基异质结双极型晶体管. 在集电极电流 $I_C = 34.2$mA 的条件下，发射极面积为 $0.8\mu m \times 12\mu m$ 的 InP HBT 截止频率 f_T 为 162GHz，最大振荡频率 f_{max} 为 52GHz，最大直流增益为 120，偏移电压为 0.10V，击穿电压 BVCEO 达到 3.8V($I_C = 0.1\mu A$). 这种器件非常适合在高速低功耗方面的应用，例如 OEIC 接收机以及模拟数字转换器.

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