Digital Coarse Tuning Loop for Wide-Band Fast-Settling Dual-Loop Frequency Synthesizers

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Abstract: A new coarse tuning loop for a wide-band dual-loop frequency synthesizer is presented. The coarse tuning structure is composed of two digital modules, including a successive approximation register and a frequency comparator with a novel structure. The frequency comparator counts the prescaler cycles within a certain reference time and compares the number with preset data to estimate the VCO frequency. The frequency comparison error is analyzed in detail. Within a given coarse tuning time, our proposed structure shows a comparison error 20 times smaller than that of other reported structures. This structure also reuses the programmable divider as a part of the coarse tuning loop so that the circuit is greatly simplified.

Key words: wide-band; coarse tuning loop; frequency synthesizer; voltage-controlled oscillator
EEACC: 2560
CLC number: TN43 **Document code**: A **Article ID**: 0253-4177(2006)11-1911-07

1 Introduction

As integrated phase-locked loop (PLL) frequency synthesizers have been more widely used in modern communication, a large, multi-band tuning range is required for compatibility between various standards, and this in turn requires a high VCO gain for a single loop PLL. However, a high VCO gain means high sensitivity of the PLL with respect to noise in the control line. Scaled supply voltage in submicron CMOS technology makes the situation even worse for the shrunken VCO tuning voltage.

One way to achieve both wide tuning range and low VCO gain is to use digital controlled switched-capacitors (SCs) in the VCO's resonant tank [1] and dual loops, i.e., a coarse tuning loop and a fine tuning loop, to control the SCs and the tuning voltage, respectively. The coarse tuning loop in Ref. [2], which is composed of an analog phase detector, a charge pump, a loop filter, and an ADC, can easily realize dual-loop settling with large loop band width, but it consumes too much chip area and current. Inspecting the tuning voltage to estimate the VCO frequency simplifies the coarse tuning loop[3], but the fixed bandwidth can hardly compromise between settling time and phase noise. The digital filter after the divider in Ref. [4] with a look-up table can get the right tuning curve quickly, but the loop is also complex. A direct digital calibrating loop was then brought into applications to simplify the control circuit and speed the coarse tuning process in Refs. [5~7]. In these structures, all digital adaptive frequency calibration (AFC), including the frequency comparator and coarse tuning controller, are used. The reference frequency and divided output frequency are compared before being counted long enough to detect the frequency, and then the control word is calibrated[5,6]. Since enough accuracy must be guaranteed, the counting process lasts a very long time. Lee *et al*.[7] reported an improved AFC structure with an additional reference multiplier to shorten the course tuning time. However, according to the analysis in section 3, the frequency tuning error can be optimized. As mentioned in Ref. [7], the frequency comparison error is due to asynchronous signal edges of the two input frequencies, which is inevitable, so comparison error is a problem for this kind of structure. But in all the papers referred to above, no comparison error has been discussed in detail for a digital coarse tuning loop. In this paper, a new all-digital coarse tuning loop for a multi-band frequency synthesizer is presented. The most signifi-

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Received 12 March 2006, revised manuscript received 31 July 2006

cant feature of this structure is that the high frequency of the fine tuning loop is used as a clock to count the cycles within the reference time to detect the VCO frequency. As analyzed in the following section, the proposed structure introduces less comparison error within a given tuning time. The idea is also designed with digital circuitry and verified by simulation.

2 Proposed structure

As shown in Fig. 1, the fine tuning loop is composed of a phase/frequency detector (PFD), a charge pump, a voltage-controlled oscillator (VCO), a divider (composed of a prescaler and a programmable divider), and a loop filter. The divider and the VCO are also parts of the coarse tuning loop. The coarse tuning loop compares the VCO frequency with preset one, and the SAR controls the coarse tuning process. The switch SW

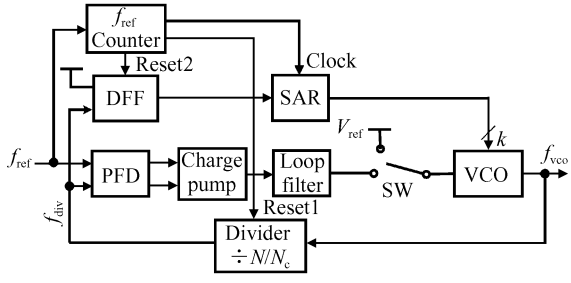

Fig. 1 Proposed dual-loop frequency synthesizer diagram (sigma-delta modulator not included)

in Fig. 1 connects to V_{ref} during the coarse tuning process and to the output of the loop filter during the fine tuning process. The divider ratio of the divider is N/N_c during the fine/coarse tuning process. Each time the synthesizer is powered on or reset to a new frequency, the coarse tuning loop is enabled, and the proper VCO tuning curve is selected within k comparing cycles. k cycles later, the k-bit control word is frozen for the fine tuning process. The SAR sets the VCO control bits one by one to realize binary searching, which is explained in Fig. 2. The SAR first presets the MSB of the control word and then compares the counter result with preset data M to detect the frequency. Finally, it revises the preset bit according to the comparison result. Then it does the same for the next significant bit, until the LSB is preset and revised. The process is similar to that in Ref. [7], except that we use only one signal to indicate the frequency comparison result, which simplifies the comparison modules. After all VCO control bits from the MSB to the LSB are preset and revised, the control word is frozen, and the fine tuning loop begins to work.

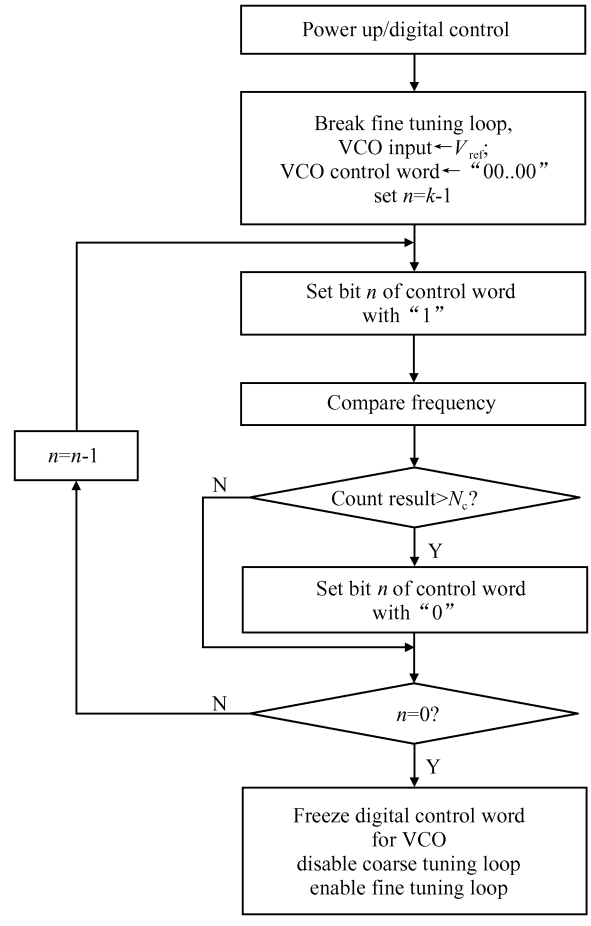

Fig. 2 Binary search diagram of SAR

3 Frequency comparator and comparison error

Figure 3 shows the coarse tuning block diagrams of the coarse tuning structure. Figure 3(a) is the conventional structure, and Figure 3(b) is the new structure proposed in this paper. As mentioned above, there is a comparison error in the digital frequency comparator because of the variable phase difference between input signals at the start and end points of each comparison. In order to estimate the comparison errors of above structures, we observe the general comparing process. As shown in Fig. 4, R represents the reference frequency with fixed period, and M (here $M=6$) cycles make up a comparison reference time T_{rc}.

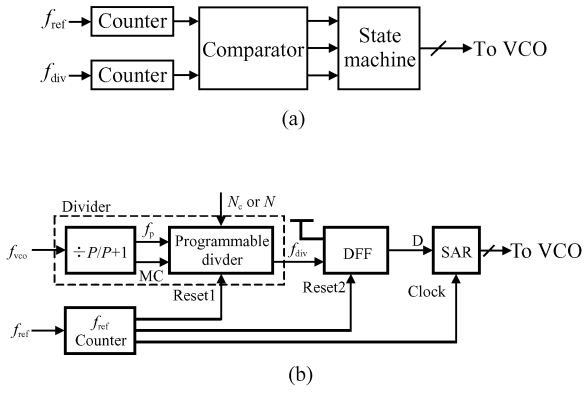

Fig.3　Coarse tuning block diagram　(a) Conventional structure; (b) Proposed new structure

Marks a and b are the start and end points, respectively. V is the signal being compared, and V_1 and V_2 are the two instances with very close frequency but very different phases at start point a.

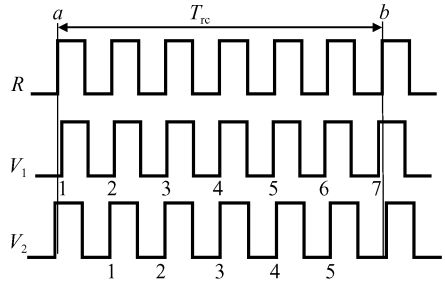

Fig.4　General frequency comparison waveform

Given that the positive edge is the active edge, the count results of V_1 and V_2 are very different. As shown in Fig.4, V_1's first positive edge comes just after the counting process start point a, and the last positive edge comes just before the count process end point b, and the counting result is 7. Meanwhile, V_2 just misses the two chances at points a and b, and the counting result is 5. As can be seen in Fig.4, the frequencies of V_1 and V_2 are very close, but the counting results are very different.

Here V_1 and V_2 represent two extreme conditions, and the counting results reflect the count error range. If X is the expected count, then the count result may be $X-1$, X, or $X+1$. Thus the maximum counting error is ± 1. If the count result is X, the actual count may be $X-1$, X, or $X+1$, so the extreme period of the V is

$$T_V = \frac{T_{rc}}{X \pm 1} = \frac{M}{X \pm 1} T_R \tag{1}$$

Since

$$T_{rc} = MT_R$$

The corresponding frequency is

$$f_V = \frac{X \pm 1}{M} \times f_R \tag{2}$$

Thus, the maximum frequency comparison error is

$$f_{V,error,max} = \frac{X \pm 1}{M} \times f_R - \frac{Xf_R}{M} = \pm \frac{f_R}{M} = \pm \frac{1}{T_{rc}} \tag{3}$$

As shown in Eq. (3), the frequency comparison error caused by counting error1 is inversely proportional to the counting time T_{rc}, which is also the time for one VCO bit calibration. Different M or X will not affect the above comparison error estimation.

For k-bit VCO control bits and binary searching, the coarse tuning time is

$$T_{AFC} = kT_{rc}$$

Thus, reducing the comparison error is at the cost of increasing the coarse tuning time, and vice versa.

Note that the frequency comparison error in Eq. (3) is not for our target——VCO frequency error. In the structure of Fig.3(a), as

$$f_{vco} = Nf_{div} \tag{4}$$

the maximum VCO frequency comparison error is

$$f_{vco,error,max} = Nf_{div,error,max} = \pm Nf_{rc} \tag{5}$$

As for a fractional-N frequency synthesizer, the "N" in Eq. (5) is the integer part of the fractional divide ratio, and additional error may be introduced into the total error, so for a fractional-N structure,

$$f_{vco,error,max} = \pm (N+1) f_{rc} \tag{6}$$

For any condition, the VCO frequency comparison error is inversely proportional to the comparison time T_{rc}, so we can improve one parameter only at the cost of the other.

In order to compare the performance of the structures in Fig.3, a new figure of merit, ETP, is defined as the product of the maximum VCO comparison error and the time for one bit calibration:

$$\mathrm{ETP} = | f_{vco,error,max} | T_{rc} \tag{7}$$

As small calibration time and small calibration error are expected, the smaller the ETP, the higher performance we will get.

Substituting Eq. (6) into Eq. (7), we get the ETP for the normal frequency comparison structure:

$$\mathrm{ETP} = N + 1 \tag{8}$$

In Eq. (8), M has disappeared, which means that

ETP is independent of M. Although changing M may help to tradeoff between the comparison error and the comparison time, the general performance remains unchanged.

We also find in Eq. (5) that N comes from the divider ratio between f_{VCO} and f_{div}, which is the frequency being compared with the reference frequency. Thus an effective way to decrease ETP is to decrease this ratio. In Ref. [7], the ETP can be optimized according to the analysis above.

If f_{vco} can be used as the input of the frequency comparator, we will get the best result, in Eq. (8) with $N = 1$. As shown in Fig. 4, the counter must be resetable before point a, but in an RF frequency synthesizer, the VCO frequency is too high for digital counters to reset. Although high speed prescalers are inserted to slow down the VCO frequency, they are hard to reset in critical time. Therefore, the prescaler output frequency f_p is the highest frequency that can be used as the input of the frequency comparator, and using this signal is the idea behind the structure in Fig. 3 (b).

In Fig. 3 (b), the prescaler output frequency f_p is used as the input of the programmable divider with reset. The divider is reused as a "frequency comparator", and the divider ratio between f_{vco} and f_{ref} is N_c. The programmable divider output MC controls the prescaler divide ratio. The f_{ref} counter generates a comparison reference time T_{rc} for the coarse tuning. Reset1, Reset2, and Clock have the same frequency of $f_{ref}/(M+1)$ and different timings for correct counting and result estimation. In each clock cycle, the programmable divider is reset and begins to count and output f_{div} as a normal divider. The D-flip-flop (DFF) captures the first edge of f_{div} and output signal D for the SAR.

Figure 5 shows the waveform of the proposed

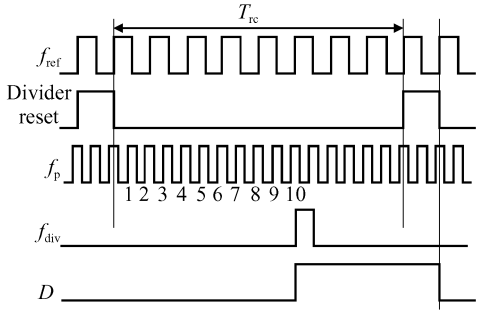

Fig. 5 Waveform for Fig. 3(b)

structure in Fig. 3 (b). Here, the reference frequency is used to generate the reference time for frequency comparison, and the reference time T_{rc} can be generated with the same reference frequency as the fine tuning loop used. In Fig. 5, the reset signal divider reset controls the reset of the programmable divider, and the positive edge of f_{div} is captured by the DFF and output D to indicate whether the count result is greater than the preset frequency. Here, $M = 8$, and the divide ratio between f_p and f_{div} for the main counter is 10. In this condition, signal D indicates that the frequency of f_{vco} is greater than the preset one. If the frequency of f_{vco} is smaller than the preset one, no pulse of f_{div} will be observed and D remains low, because the divider is reset before it can generate this pulse.

With the structure in Fig. 3(b), the VCO frequency is divided by P or $P+1$ by the prescaler, and without prescaler resetting, the maximum VCO counting error can be readily deduced as

$$f_{vco,error,max} = \pm Pf_{rc} \tag{9}$$

where P instead of $P+1$ is used in Eq. (9) because we can easily control the prescaler to divider by P at the start and end points. For the fractional-N frequency synthesizer, we can also get

$$f_{vco,error,max} = \pm (P+1)f_{rc} \tag{10}$$

Finally we can get the ETP for our proposed structure:

$$\mathrm{ETP} = P + 1 \tag{11}$$

Generally speaking, P is much smaller than N, so the new coarse tuning structure in Fig. 3(a) shows much higher performance than that of the normal structure.

4 Simulation results

A fractional-N wide-band frequency synthesizer with the structure shown in Fig. 1 was designed with Jazz 0.35μm 3.3V CMOS technology and simulated with Cadence, where the sigma-delta modulator (SDM) is not shown. Since the SDM was not needed during the coarse tuning process, its output was shut down for coarse tuning. This had little effect on the fine tuning loop. The VCO tuning range is 1.7～2.6GHz, which covers multiple modern communication bands, such as 1.8, 1.9, 2, and 2.45GHz. Dividing by two, another two bands, 850 and 900MHz, can be covered. The

coarse tuning part, including the programmable divider, SAR, f_{ref} counter, and control bus, were synthesized and routed, with a total area of 0.104mm^2.

The VCO is designed as that in Ref.[7], and the prescaler divider ratio of 4/5 is chosen. The VCO total tuning range is 900MHz, with a 4-bit control word. A frequency overlap between adjacent tuning curves of about 25% is designed, as shown in Fig.6.

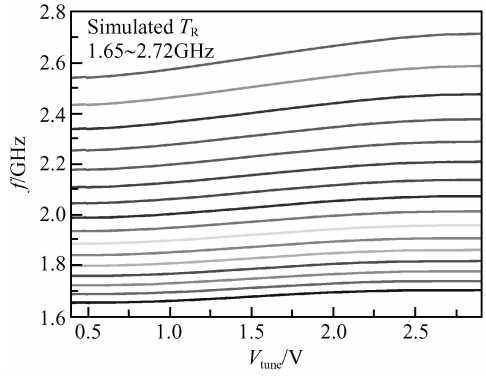

Fig.6　VCO tuning curves

As we want the VCO frequency error of the coarse tuning process to be less than 10% of the average effective tuning range of one tuning curve,

$$|f_{\text{vco,error,max}}| = 10\% \times \frac{2 \times 900\text{MHz}}{2^4} = 11.25\text{MHz}$$

Introducing the above equation into Eq.(10), we get the smallest T_{rc}:

$$T_{rc} = \frac{P+1}{|f_{\text{vco,error,max}}|} = \frac{5}{11.25\text{MHz}} = 0.45\mu\text{s}$$

In this design, the frequency $f_{ref}/16$ can easily be obtained, i.e., $M = 16$, and

$$T_{rc} = \frac{16}{20\text{MHz}} = 0.8\mu\text{s}$$

The coarse tuning process is shown in Fig.7 for a target VCO frequency of 2.15GHz. The divider ratio is

$$N = 107 = 0110\ 1011_2$$

and the 12-bit sigma-delta input is

$$K_{SDM} = 0.5 = 100000000000_2$$

The divider ratio for coarse tuning frequency comparison is

$$N_c = [NK_{SDM} \times 16] = 011010111000_2 = 1720$$

In this design, $P = 4$ and $N = 107$, as $(107+1)/(4+1) = 21.6$, and the proposed structure shows 20 times higher performance than that of the normal structure.

Figure 7 shows the simulation waveform for the proposed structure. The signal bus b〈3∶0〉 represents a 4-bit VCO control word. The signal "state" is the output of the SAR (not shown in Fig.3(b)), which indicates whether the frequency tuning state is in coarse tuning (when state = 1) or in fine tuning (when state = 0). The signal MC is the prescaler mode control bit, and it works during both the coarse tuning and the fine tuning processes. f_{div} is the output of the divider, and its pulse signal is captured to calibrate the control word b〈3∶0〉. In the beginning, one additional T_{rc} cycle is for system resetting.

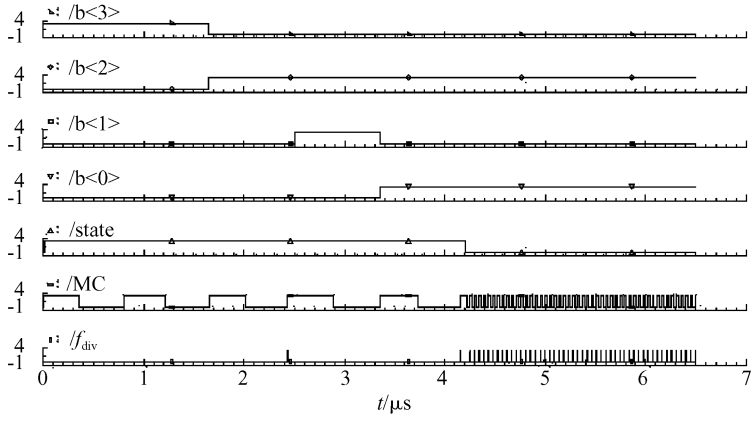

Fig.7　Simulation result of the VCO control word waveform

As shown in Fig.7, the VCO control word b〈3∶0〉 is frozen to 0101 when the coarse tuning is finished, and b〈3∶0〉 = 0101 represents the sixth tuning curve in Fig.6, which is the expected

one. The total coarse tuning time is less than 4μs, including the one additional resetting cycle, and after the coarse tuning process, the fine tuning begins. The coarse tuning loop shrinks the tuning range from 900MHz (1.7～2.6GHz) to nearly 56MHz (900MHz/16) within only 4μs. In Ref. [7], it takes 12.6μs to finish the AFC even with two additional frequency doublers, so our proposed structure provides an improved way to design a high performance frequency synthesizer for future communication.

A fine tuning loop with a loop band-width of 100kHz is designed. In Fig. 8, the waveform of $V_{\rm tune}$ is shown. During the coarse tuning, $V_{\rm tune}$ remains unchanged, while during the fine tuning process, $V_{\rm tune}$ quickly settles down. After coarse tuning, the VCO frequency is very close to the target one, so the fine tuning loop easily locks. In Fig. 8, the total locking process including coarse and fine tuning takes only 15μs. This indirectly verifies the success of the proposed coarse tuning structure.

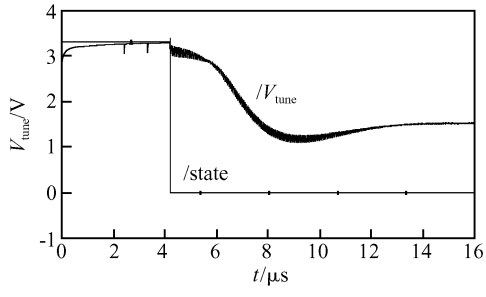

Fig. 8 Simulation result of $V_{\rm tune}$ and state

5 Conclusion

A new coarse tuning loop for a dual-loop frequency synthesizer is proposed in this paper, and the frequency comparison error is analyzed in detail. With the newly defined figure of merit ETP, the proposed coarse tuning loop shows much higher performance than conventional ones. This structure also reuses the divider as part of the frequency comparator, and the idea is verified by the simulation of a 1.7～2.6GHz multi-band frequency synthesizer.

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快速锁定、宽带双环路频率综合器的数字粗调环路

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摘要：提出了一种用于宽带、双环路频率综合器的粗调环路结构.该粗调环路由数字电路设计实现，包含逐次逼近寄存器和新结构的频率比较单元两个模块.其中，频率比较单元在一定的参考时间内对预分频器的输出信号周期进行计数，然后通过比较计数结果与预设值的大小来估计 VCO 输出频率.对比较误差进行了详细分析，分析表明，在一定的比较时间内该结构的比较误差比现有结构小 20 倍，而且由于重复利用可编程分频器作为粗调环路的一部分，整体电路也大为简化.

关键词：宽带；粗调环路；频率综合器；压控振荡器

EEACC：2560

中图分类号：TN43　　**文献标识码**：A　　**文章编号**：0253-4177(2006)11-1911-07

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2006-03-12 收到，2006-07-31 定稿