A 2GHz Low Power Differentially Tuned CMOS Monolithic LC-VCO *

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Abstract: A 2GHz differentially tuned CMOS monolithic LC-VCO is designed and fabricated in a 0.18μm CMOS process. The VCO has a 16.15% tuning range (from 1.8998 to 2.2335GHz) through a combination of analog and digital tuning techniques (4-bit binary switch-capacitor array). The measured phase noise is -118.17dBc/Hz at a 1MHz offset from a 2.158GHz carrier. With the presented improved switch, the phase noise varies no more than 3dB at different digital control bits. The phase noise changes only by about 2dB in the tuning range because of the pn-junctions as the varactors. The VCO draws a current of about 2.1mA from a 1.8V power supply and works normally with a 1.5V power supply.

Key words: binary switchable-capacitor array; CMOS; differentially tuned; phase noise; VCO
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1 Introduction

The growing development and popular application of portable communications and short range wireless communications is driving a need for a higher degree of integration in wireless transceivers, especially system-on-chip (SOC) devices, in order to achieve lower cost, lower power consumption, and smaller size. The voltage-controlled oscillator (VCO), which is the most important part of PLL-based frequency synthesizers, consumes a major fraction of the overall power of a synthesizer. The phase noise performance of the VCO directly affects the PLL's performance. Therefore low-power, high-performance, and fully-integrated VCOs have been widely researched[1~8].

In SOC design, the common-mode noise, especially the substrate noise, can contribute to the phase noise of the VCO. Differentially tuning the VCO[4~8] is a good way to improve its substrate noise immunity.

A 2GHz differentially tuned VCO is presented in this paper. It works with a power supply as low as 1.5V because of the binary switch-capacitor array technique with an improved switch and the differential tuning technique. The circuit design, including the VCO and the on-chip bandgap references, are also described.

2 LC-VCO design

It is difficult to realize a wide tuning range and high linearity in a VCO's gain in low voltage operation. Here we apply the differential tuning and binary switchable-capacitor techniques to expand the tuning range, and we improve the linearity of the VCO's gain (K_{VCO}) by using pn-junction varactors. The choice of the structure of the VCO, the improved switch, the low power design, and the high degree of integration will be introduced below.

2.1 VCO design

To reduce the power consumption of the VCO, we limit the current to about 2mA in the design. Thus, the VCO works in the current-limited region[9]. A structure of complementary nMOS and pMOS cross-coupled pairs, which provides better phase noise performance in the current-limited region[10], is chosen, as shown in Fig. 1. The current of the VCO is provided by the on-chip bandgap cir-

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cuit ,and the fully-integrated VCO is realized.

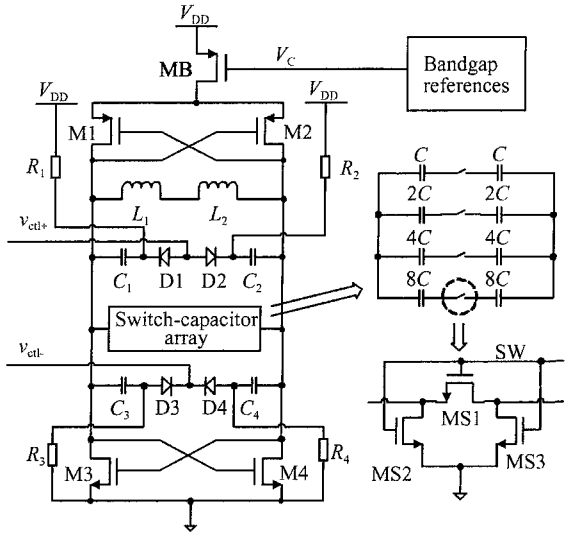

Fig. 1 Schematic of the VCO

Differentially tuning the LC-VCO reduces the effect of common noise on the control input signal[5] and extends the tuning range of the VCO, which is important for low-voltage operation. K_{VCO} can be reduced to improve the phase noise performance[3] within the expanded tuning range. The differentially tuned LC-VCO is adopted ,and the binary switchable-capacitor array is implemented to extend the tuning range further. With the expanded tuning range , K_{VCO} of the VCO is reduced to about 20MHz/V.

In order to reduce the effect of the switch in the switchable-capacitor array on the LC-tank ,the improved switch shown in Fig. 1 is adopted. It is a simple version of the switch in Ref. [11]. When the switch transistor MS1 is on ,the nMOS transistors MS2 and MS3 are also turned on and connect the drain and source of MS1 to ground to reduce MS1's turn-on resistance, which can deteriorate the quality factor of the LC-tank. The complexity of this improved switch is reduced compared to Ref. [11].

A pn-junction varactor is more linear than an accumulation-MOS varactor. Therefore we adopt pn-junction varactors D1 ,D2 ,D3 ,and D4 as shown in Fig. 1. To avoid positive-bias of the varactors ,we use the capacitors C_1 , C_2 , C_3 ,and C_4 to directly bias D1 and D2 to the power supply ,and we use the resistors R_1 , R_2 , R_3 ,and R_4 to directly bias D3 and D4 to ground. In this way ,we avoid complex bias circuits.

The pMOS transistors M1 and M2 , and the nMOS transistors M3 and M4 constitute the cross-coupled pairs. They generate a negative resistance to cancel the loss in the LC tank. The inductors L_1 and L_2 are circular inductors. The quality factor of the inductors reaches about 8 at 2GHz. The bias current is provided by the pMOS transistor MB. We chose to use a pMOS transistor because the $1/f$ noise of a pMOS transistor is less than that of an nMOS transistor.

2.2 Bandgap reference design

Figure 2 shows a simple schematic of the bandgap references shown in Fig. 1. The most important problem in low voltage (1.8V) bandgap design is the startup of the reference source. As shown in Fig. 2 ,the transistors M3 , M4 , M6 , M7 , M8 , and M9 and the capacitor C_2 constitute the startup circuit ,which injects current to the core of the bandgap through transistors M3 and M4 when the circuit is powered on. C_2 is used to compensate the feedback loop composed of the startup circuit and the core circuit of the bandgap in order to avoid oscillation. The transistor M10 provides current for the VCO. Only the resistor R_{exit} is realized by an off-chip component. With the on-chip bandgap references ,the fully-integrated VCO is realized.

3 Experimental results

The VCO is fabricated in 0.18μm 1P6M CMOS technology. The implemented VCO is measured with an Agilent 8563EC spectrum analyzer. A die microphotograph is shown in Fig. 3. The core circuit of the VCO is about 740μm ×890μm.

The measured frequency tuning range curve is shown in Fig. 4. The tuning range is from 1.8998 to 2.2335GHz (about 16.15%). The frequency space of each pair of adjacent control bits is about 16MHz ,and the K_{VCO} is about 20MHz/V.

The measured output spectrum and the phase noise are shown in Figs. 5 and 6 ,respectively. The measured phase noise at 2.158GHz is -118.17 dBc/Hz at a 1MHz offset from the carrier as shown in Fig. 6. The phase noise performance is shown in Fig. 7 for when the controlling bits are "1000" and the differentially controlled voltage is varied from -0.8 to 0.8V. As can be seen , the phase noise variation is only about 2dB ,which was

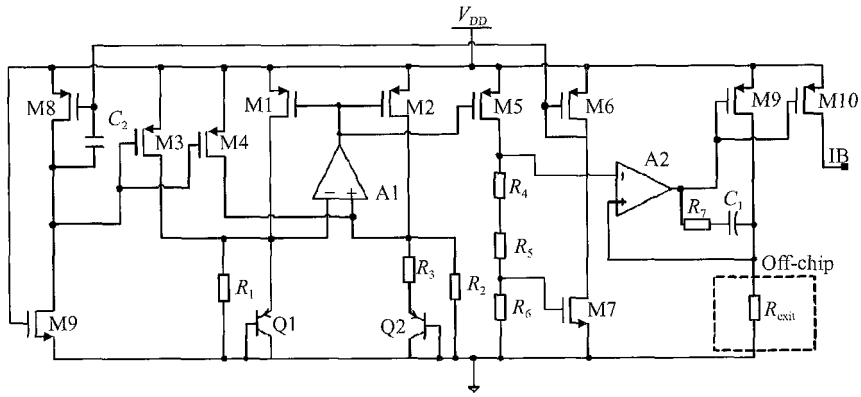

Fig. 2　Schematic of the bandgap references

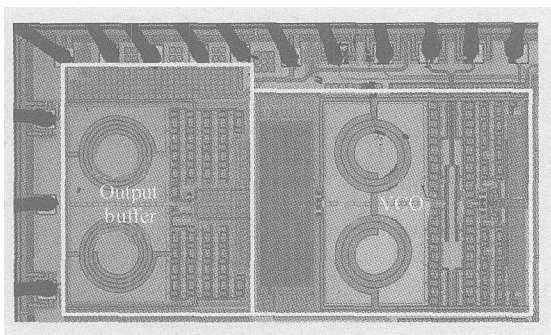

Fig. 3　Die microphotograph of the VCO

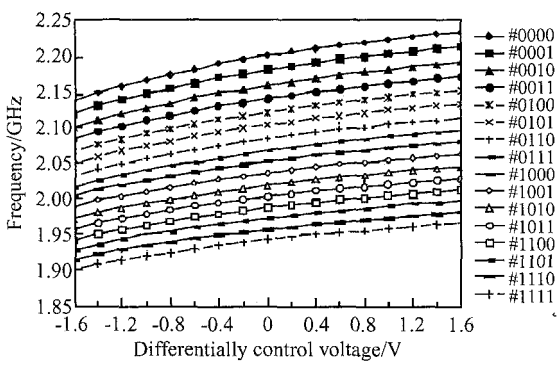

Fig. 4　Measured tuning range of the VCO

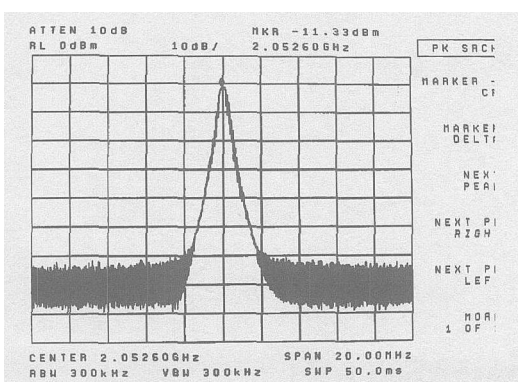

Fig. 5　Measured output spectrum of the fabricated VCO

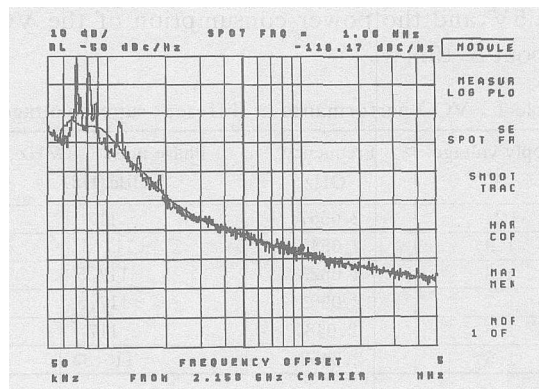

Fig. 6　Phase noise versus frequency offset at 2. 158GHz

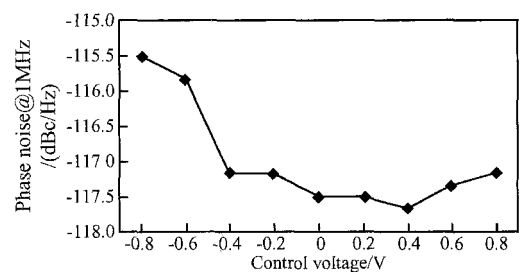

Fig. 7　Phase noise of the VCO for differentially controlled voltage from - 0. 8 to 0. 8V

achieved by applying the pn-junction varactors.

The phase noise of the VCO is shown in Fig. 8 for different values of the control bits and a differentially controlled voltage of 0V. The phase noise varies by no more than 3dB. This proves that the improved switch does not deteriorate the phase noise performance very much.

The VCO 's performance is summarized in Table 1 for when the control bits are set at "1000". The frequency changes by about 11. 5MHz when the supply voltage changes from 1. 5 to 2V. When

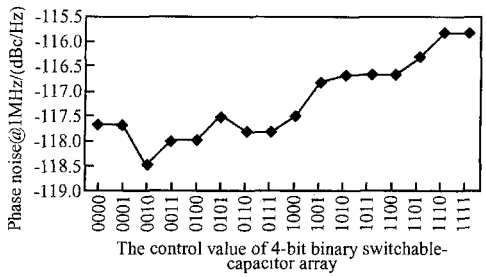

Fig. 8 Phase noise of VCO at different control bits

the supply voltage is 1. 8V , the current consumption of the VCO is about 2. 1mA. The VCO works normally even when the supply is reduced to 1. 5V , and the power consumption of the VCO is about 3. 15mW.

Table 1 VCO performance at different supply voltages

Supply voltage / V	Frequency / GHz	Phase noise @1MHz / (dBc/ Hz)
2	2. 0567	- 117
1. 9	2. 0543	- 117. 83
1. 8	2. 0523	- 117. 5
1. 7	2. 0503	- 117. 5
1. 6	2. 048	- 117
1. 5	2. 0452	- 115. 33

4 Conclusion

A differentially tuned CMOS monolithic LC-VCO with a tuning range of 16. 15 % is presented in this paper. With on-chip bandgap references , a high degree of integration is realized. The measured phase noise variation is about only 2dB with the pn-junction varactors. The phase noise performance is degraded by no more than 3dB with the improved switch. The power consumption of the VCO core is about 3. 78mW when the power supply is 1. 8V and about 3. 15mW when the power supply is 1. 5V. The presented design is suitable for low power applications.

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2 GHz 低功耗差分控制的 CMOS 单片 LC 压控振荡器*

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摘要：设计了工作在 2 GHz，差分控制的单片 LC 压控振荡器，并利用 0.18μm CMOS 工艺实现. 利用模拟和数字(4 位二进制开关电容阵列)调频技术，压控振荡器的调频范围达到 16.15 %(1.8998～2.2335 GHz). 在 2.158 GHz 工作频率下，在 1 MHz 频偏处的相位噪声为 - 118.17 dBc/ Hz. 应用给出的开关设计，相位噪声在不同的数字位控制下变化不超过 3 dB. 由于利用 pn 结二级管作为变容管，在调频范围内，相位噪声仅改变约 2 dB. 压控振荡器在 1.8 V 电源电压下消耗 2.1 mA 电流并能够在 1.5 V 电源电压下正常工作.

关键词：二进制开关电容阵列；互补-MOS 型集成电路；差分控制；相位噪声；压控振荡器
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