Investigations of Key Technologies for 100V HVCMOS Process*

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Abstract: A novel dual gate oxide (DGO) process is proposed to improve the performance of high voltage CMOS (HVCMOS) devices and the compatibility between thick gate oxide devices and thin gate oxide devices. An extra sidewall is added in this DGO process to round off the step formed after etching the thick gate oxide and poly-silicon. The breakdown voltages of high voltage nMOS (HVnMOS) and high voltage pMOS (HVpMOS) are 168 and −158V, respectively. Excellent performances are realized for both HVnMOS and HVpMOS devices. Experimental results demonstrate that the HVCMOS devices work safely at an operation voltage of 100V.

Key words: HVCMOS; DGO; compatibility
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1 Introduction

In recent years, there have been intensive studies of high voltage integrated circuits (HVICs) with improved performance, reduced size, and lower cost in system integration[1]. HVICs can be used in flat panel display drivers, power regulation, telecommunication circuits, automotive and motor control, etc. For these categories of applications, it is usually preferable to perform most of the signal processes at low voltages, while the resulting output is raised to a higher voltage level [2~5].

HVCMOS technology integrates high voltage devices with standard CMOS platforms. One of the most important requirements is to achieve favorable performance of the high voltage devices without changing the standard CMOS device performance. For some applications, the gate oxide of HVpMOS must be thicker than that of HVnMOS, which is as thick as low voltage CMOS (LVCMOS), because the gate electrode of HVpMOS is driven by a high voltage level equal to the high supply voltage. A dual gate oxide (DGO) process, in which both thick and thin gate oxide devices are integrated into the same chip[6~8], is a key challenge of HVCMOS technology. In this paper, a feasible DGO integration approach is presented, and key technologies of the HVCMOS process are investigated. The experimental results show that high performance of HVCMOS is achieved.

2 Device structure

Figure 1 shows a cross-sectional schematic of HVCMOS devices on p-type substrate, in which the lateral double diffused MOSFET (LDMOS) structure is adopted. The high voltage nLDMOS and pLDMOS devices were integrated into standard low voltage CMOS technology by adding a few masks and some process steps. The HVpMOS was fabricated in a lightly doped deep n-well. To increase the breakdown voltage of the devices, Hvpwell and Hvnwell, located between the channel and drain, were designed for lightly doped drift regions of HVpMOS and HVnMOS, respectively. In addition, nwell and pwell were channels for HVpMOS and HVnMOS, respectively. These two wells can affect the threshold voltage and the output current of the devices. In the proposed HVCMOS structure, the thickness of the gate oxide layers of the HVpMOS is 200nm because the maximum applied voltage between the gate and source electrodes is about 100V, while the gate electrodes of the HVnMOS and LVCMOS devices are driven by 0/5V signals, so a thin gate oxide can be used. Here the thin gate oxide is 15nm.

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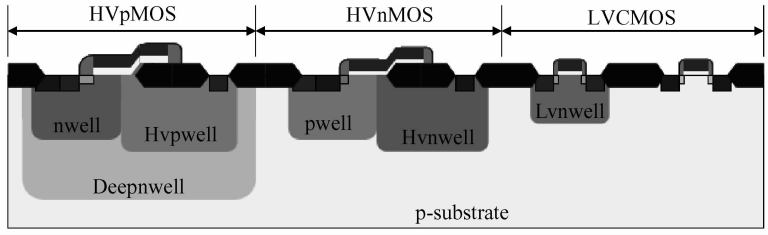

Fig. 1　Cross-sectional schematic of HVCMOS devices

SIVACO TSUPREM-4 and MEDICI TCAD tools were used to simulate the structure parameters and process parameters. Under the condition that its breakdown voltage is larger than 100V, the other parameters (such as driver currents, low power consumption, and high frequency properties) are optimized. The main optimized process and structure parameters are shown in Table 1.

Table 1　Key parameters of HVCMOS devices simulated by TCAD tools

Parameter	Length of drift region $L_d/\mu m$	Length of channel $L_c/\mu m$	Length of field plate $L_g/\mu m$	Drift region dose $/cm^{-2}$	Channel dose $/cm^{-2}$	Deepnwell dose $/cm^{-2}$
HVnMOS	9.5	2	1.0	1.9×10^{12}	5×10^{13}	—
HVpMOS	9.8	2	1.0	1.7×10^{13}	3×10^{13}	6×10^{12}

3　Fabrication process of HVCMOS

The proposed high voltage CMOS process is compatible with a standard 0.8μm single well CMOS process. The key steps of fabrication are shown in Table 2. In this process, high voltage wells are driven before the standard CMOS steps, and the following steps are the same as for a standard CMOS process, except for the thick gate oxide formation of the HVpMOS and the first sidewall formation.

Table 2　Compatible HVCMOS process flow

1. High resistivity (ρ=30～50Ω·cm) p-bulk substrate;
2. Deepnwell (implant dose, $6\times10^{12}cm^{-2}$) for HVpMOS formation;
3. Drift region and channel formation(Hvnwell, Hvpwell, pwell, nwell);
4. Lvnwell for low voltage nMOS formation;
5. 200nm thick gate oxide formation;
6. Poly-gate of HVpMOS formation;
7. LDD implantation for HVpMOS;
8. Sidewall for HVpMOS formation;
9. S/D implantation for HVpMOS;
10. 15nm thin gate oxide poly-gate formation for HVnMOS and LVCMOS devices;
11. Second sidewall formation for HVnMOS and low voltage devices;
12. S/D implantation for HVnMOS and LVCMOS devices;
13. Contact and metallization.

4　Investigation of the key technologies for HVCMOS process

Compatibility is a very important problem for the HVCMOS process. In this paper, a DGO process is adopted, and an extra sidewall is added in the DGO process to improve the compatibility of the HVCMOS.

The main steps of the DGO process are shown in Fig. 2. During this process, the thick gate oxide was removed to 180～190nm by dry etching, followed by poly-silicon etching in order to guarantee the self-alignment between the thick gate oxide and ploy-silicon gate, and a 10～20nm gate oxide was retained to protect the Si-SiO_2 interface from plasma damage. A sidewall was formed after the LDD implantation of the HVpMOS (as shown in steps 5 and 6), which can alleviate the height of the step between the thick gate oxide poly-gate and the following thin gate oxide and deposited poly-silicon, to guarantee that the deposited poly-silicon can be etched completely. S/D implantation was followed by sidewall formation, and then the removal of the SiO_2 by 50∶1 HF. Thin gate oxide and the second poly-silicon were formed subsequently.

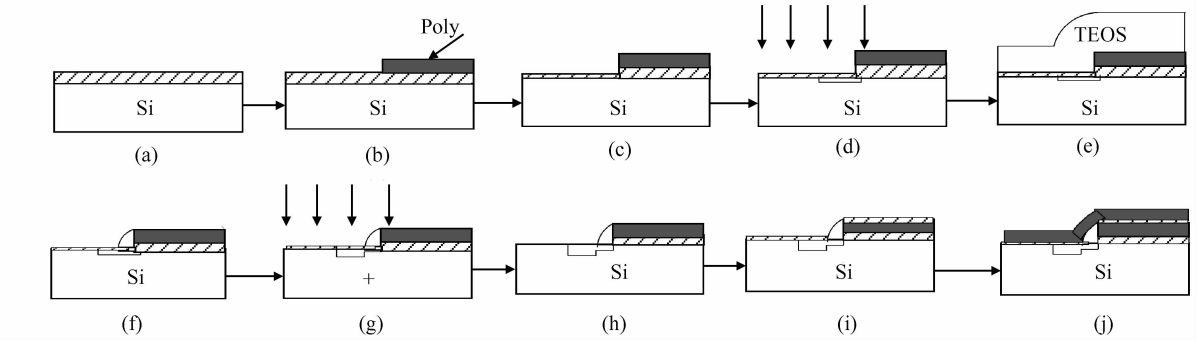

Fig. 2 Schematic of dual gate oxide process (a) 200nm thick gate oxide TEOS; (b) Poly-silicon etched; (c) Dry etch gate-oxide and 10～20nm retained; (d) p-implantation; (e) TEOS deposited; (f) Plasma etching TEOS and 10～20nm TEOS retained; (g) S/D implantation; (h) Wet etching SiO_2 by 50 ∶ 1 HF; (i) 15nm thin gate oxide; (j) Second poly-silicon

Several experiments were carried out to demonstrate the feasibility of the proposed DGO process, both for (1) a normal DGO process without the extra sidewall formation and (2) our novel DGO process with the extra sidewall formation as Figure 2 describes. The experimental characteristics of the HVpMOS fabricated by both of the above processes are similar, which are shown in Figs. 3 (a) and (b). Figure 3 (a) shows the output characteristics of the HVpMOS device. We can see that the device broke down permanently when the gate voltage was set at 40V. The breakdown characteristics of the gate-source junction are shown in Fig. 3(b), and the breakdown voltage of the thick gate oxide is only 32V.

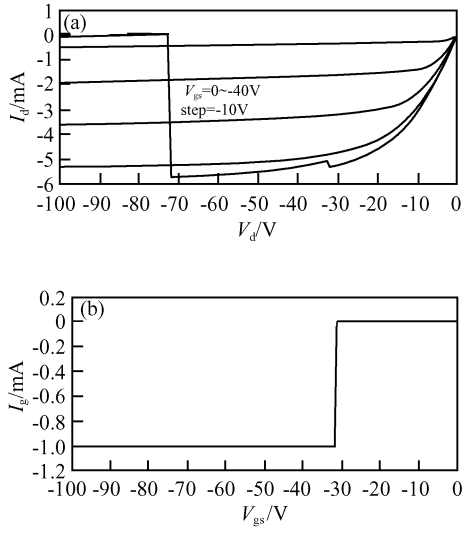

Fig. 3 (a) I_d-V_d curves of HVpMOS; (b) Breakdown characteristics of 200nm thick gate oxide

Catastrophic electrical breakdown will occur in the gate oxide when the maximum electrical field reaches $(5 \sim 8) \times 10^6$ V/cm[9]. From $E_m = V_{gs}/t_{ox}$, we can estimate that the gate-source breakdown voltage of a 200nm gate oxide should be 100～160V.

Figure 4 shows SEM pictures of the HVpMOS fabricated with different DGO processes. The remaining poly-silicon can be seen in Fig. 4 (a) at the corner of the step formed by the thick oxide and poly-silicon of the HVpMOS after the poly-silicon of the HVnMOS was etched. It can be seen that the low breakdown voltage of the gate-source junction is due to the connection between the remaining poly-silicon and thin gate oxide. However, in Fig. 4 (b), no remaining poly-silicon at the step corner can be seen from the image. This is because the sidewall was fabricated before the second poly-silicon was deposited. The sidewall rounds off the thick gate oxide step; therefore, the poly-silicon at the corner of the step was removed completely. The breakdown characteristic between the gate and source electrodes will be improved greatly after the removal of the remaining poly-silicon at the corner of the step. Another merit is that the extra sidewall can become a barrier layer to prevent the thick gate oxide and poly-silicon from wet etching in the following processes. But experimental result shows that there is no obvious improvement in the breakdown characteristics of the gate oxide layer of the HVpMOS fabricated by the second method in Fig. 4, as shown in Fig. 3 (b). From Fig. 4 (b), it can be seen that the shape of the sidewall is undesired, and the sidewall near the poly-silicon disappears. The remaining sidewall (TEOS) was thinner and poorer

quality than the thick gate oxide, resulting in the lower breakdown voltage of the gate-source junction. Over-etching during the wet etching steps after the sidewall formation is the most probable cause of the damaged sidewall.

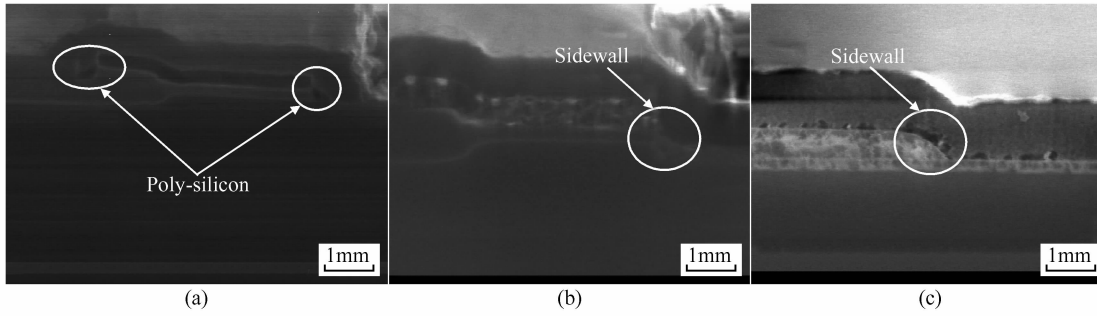

Fig. 4　SEM pictures of HVpMOS device fabricated by different DGO processes　(a) Normal DGO process without extra sidewall for HVpMOS; (b) Novel DGO process described as Fig. 2; (c) Improved DGO process based on that proposed in Fig. 2

To improve the breakdown characteristics of the gate-source junction, an experiment was conducted to study the etching speed of the TEOS and thermo-oxide by using dilute hydrofluoric acid (HF). Table 3 shows the test etching speed of the two materials in different conditions. All wafer types were dipped in the dilute HF for a few minutes. The experimental result shows that the etching speed to TEOS1 is 8 times that of the thermo-oxide. But after annealing for 30min at 800℃ in N_2 atmosphere, the ratio reduced to 3.5. An obvious improvement has been made by this method.

Table 3　Etching speed of TEOS and thermo-oxide in dilute HF　TEOS2 had been annealed for 30min at 800℃ in N_2 atmosphere before being cleaned in HF. The other two wafers were not processed before wet etching.

Parameter	TEOS1	TEOS2	Thermo-oxide 1
Original thickness/nm	457.3	598.8	40.4
Thickness after 2min wet etching in 50∶1 HF/nm	376.3	561.9	30.2
Etching speed/(nm/min)	40.5	18.5	5.1

This result demonstrates that the over-etching of the TEOS in Fig. 2 step 8 is the main reason for the poor shape of the sidewall. According to the test data from Table 3, when the 20nm thermo-oxide was etched, about 150～200nm of the TEOS was lost simultaneously. In addition, there was also a 30～40nm loss of TEOS during the cleaning step before the thin gate oxide formation, and a 200～250nm TEOS loss after the sidewall formation, resulting in the poor gate-source breakdown characteristics. To keep the shape of the sidewall, it is necessary to add an annealing step to decrease the wet etching speed of the TEOS in this process.

We have developed two methods to keep the shape of the sidewall: (1) Change the etch method of the sidewall from fixed-time etch to burst mode etch. Then the wet etching step described in step 8 of Fig. 2 should be cancelled because there is no oxide to be etched. (2) A 30min N_2 annealing at 800℃ step was added before cleaning the wafers to decrease the etching speed of the TEOS. In this case, the wet etching time must be carefully controlled in order to reduce the loss of the sidewall. Experimental results show that both methods are feasible, and characteristics of the resulting HVCMOS devices are excellent. An SEM picture of the HVpMOS fabricated by these two modified processes is shown in Fig. 4(c). An ideal space shape is achieved. The breakdown voltage of the gate-source junction is remarkably improved to 150V, as shown in Fig. 5.

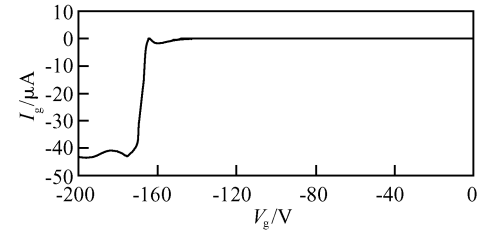

Fig. 5　Breakdown characteristics of gate-source for HVpMOS device fabricated by the modified DGO process

5 Results and discussion

Both HVCMOS and LVCMOS devices fabricated with the aforementioned new DGO process reveal excellent performance. The breakdown characteristics and output characteristics of both the HVpMOS and the HVnMOS are shown in Figs. 6 and 7, respectively.

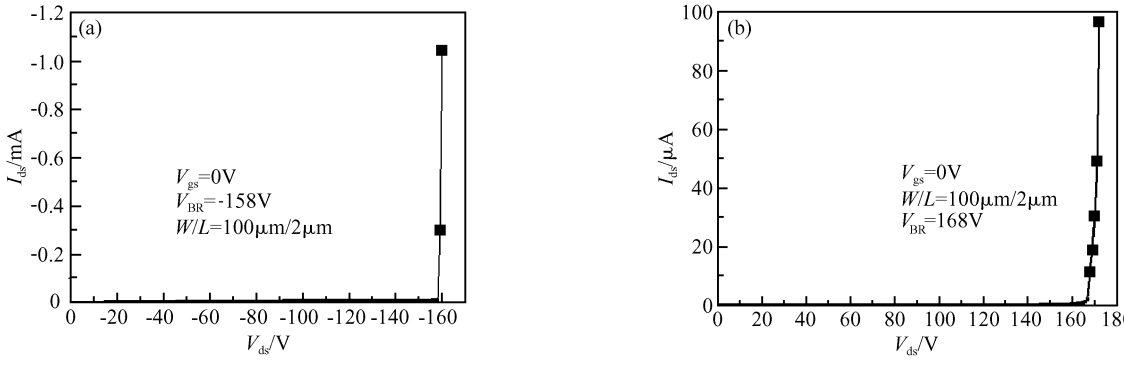

Fig. 6 (a) Breakdown characteristics of HVpMOS; (b) Breakdown characteristics of HVnMOS

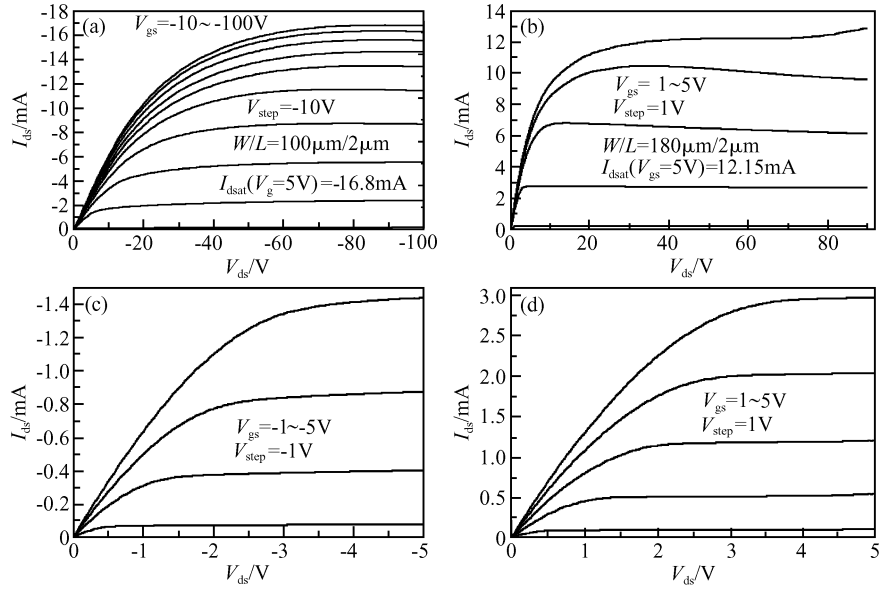

Fig. 7 (a) I_d-V_d curves of HVpMOS; (b) I_d-V_d curves of HVnMOS; (c) I_d-V_d curves of LVpMOS; (d) I_d-V_d curves of LVnMOS

As shown in Fig. 6, the breakdown voltages of the HVnMOS and HVpMOS are 168 and −158V, respectively, when V_{gs} = 0V. A very small leakage current within the sub-threshold region indicates that both high voltage devices have excellent cut-off properties.

Figure 7 (a) shows the output characteristics of the HVpMOS for V_{gs} from −10 to −100V with a step length of −10V. The output current reaches about 16.8mA for a width/length = 50 device. At high gate biases (V_{gs} = −100 V), the device is in a quasi-saturation region, and the main property of this region is that at high gate biases that affect drain current, there is no obvious increase tendency of the drain current along with the increase of the gate bias. Because the presence of the drift region, the drain current tends to be saturated first not because of the pinch-off of the channel at the drain end, but because of the velocity saturation in the drift region for carriers from the channel. The output characteristics of the HVnMOS are shown in Fig. 7 (b) for V_{gs} from 1 to 5V with a step length of 1V, and an output current of about 12.15mA for a W/L = 90 device. A

positive slope of the drain current is shown in this curve when $V_{ds} > 80$V at a gate bias of 5V, and there will be a rapid increase of the output current along with the increase of the drain voltage. This indicates that a hot snapback caused by interaction between electrical and thermal energy generated by self-heating effects will occur. The capability of the device in handling increased power dissipation is limited.

High performance of the LVCMOS devices was also achieved with this HVCMOS technology. Figures 7(c) and (d) show the output characteristics of the LVpMOS and LVnMOS devices, respectively. Good compatibility between the HVCMOS and LVCMOS was demonstrated with this process.

6 Conclusion

Using a novel DGO process, excellent breakdown characteristics of an HVpMOS's gate-source junction was achieved. High performances of both HVpMOS and HVnMOS were realized. The breakdown voltages of HVpMOS and HVnMOS were − 158 and 168V, respectively. The HVCMOS devices can operate safely in the 100V range, and the experimental results demonstrate that the proposed HVCMOS process has good compatibility.

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100V 高压 CMOS 工艺关键技术的研究*

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摘要： 提出了一种新的双栅氧(dual gate oxide, DGO)工艺，有效提高了薄栅氧器件与厚栅氧器件的工艺兼容性，同时提高了高低压器件性能的稳定性. 在中国科学院微电子研究所 0.8μm n 阱标准 CMOS 工艺基础上设计出高低压兼容的 100V 高压工艺流程，并流片成功. 实验结果表明，高压 n 管和高压 p 管的关态击穿电压分别为 168 和 −158V，可以在 100V 高压下安全工作.

关键词： 高压 CMOS 工艺；双栅氧工艺；兼容性

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