A Novel ADC Architecture for Digital Voltage Regulator Module Controllers*

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Abstract: The design and implementation of a novel ADC architecture called ring-ADC for digital voltage regulator module controllers are presented. Based on the principle of voltage-controlled oscillators' transform from voltage to frequency, the A/D conversion of ring-ADC achieves good linearity and precise calibration against process variations compared with the delay-line ADC. A differential pulse counting discriminator also helps decrease the power consumption of the ring-ADC. It is fabricated with a Chartered 0.35μm CMOS process, and the measurement results of the integral and differential nonlinearity performance are 0.92LSB and 1.2LSB respectively. The maximum gain error measured in ten sample chips is $\pm$3.85%. With sampling rate of 500kHz and when the voltage regulator module (VRM) works in steady state, the ring-ADC's average power consumption is 2.56mW. The ring-ADC is verified to meet the requirements for digital VRM controller application.

Key words: voltage regulator module; DC-DC; ring-ADC; delay-line ADC; differential pulse counting discriminator

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1 Introduction

Digital voltage regulator module (VRM) controllers have many advantages over analog VRM controllers, including built-in noise immunity and convenience in applying useful arithmetic to meet the specified static and dynamic voltage regulation[1,2]. A typical digital VRM controller, shown in Fig. 1, consists of an ADC, a digital PID compensator, a digital pulse-width modulator (DPWM), and a programmable voltage reference. ADCs with low power consumption, small gain error, high linearity, and wide quantization range are the key building blocks of digital VRMs in order to achieve good voltage regulator performance. As a result, the research of ADCs in digital VRM controller applications has received more attention recently.

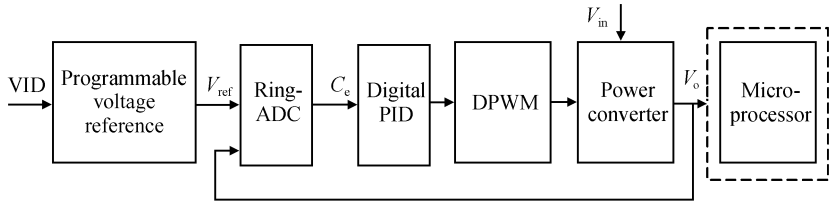

Fig. 1 Block diagram of the digital VRM

A windowed flash ADC has a window of high resolution only around V_{ref}[2]. It has the advantages of small quantization error and small delay. However, these come with the penalties of a complicated analog circuit and relatively high power consumption. Delay-line ADCs have the advantages of built-in noise immunity and low consumption of power and area, but their gain error is up to $\pm$20%[3]. A delay-ring ADC with dual delay-lines is therefore introduced, and the gain error is reduced to $\pm$10%[4]. But the delay-ring's linearity is still poor since its principle of A/D conversion

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is the same as that of the delay-line ADC.

In this paper we propose a novel ADC architecture called ring-ADC whose A/D conversion is based on the principle of voltage-controlled oscillators'（VCO）transform from voltage to frequency. In a ring-ADC, three VCOs are designed to achieve precise calibration against process variations so as to improve the gain error. Furthermore, the differential pulse counting discriminator is designed to decrease the power consumption of the ring-ADC. This ring-ADC not only maintains built-in noise immunity and low power consumption but also achieves much smaller gain error and better linearity than delay-ring ADC.

2 Principle of ring-ADC

2.1 Drawback of delay-line ADC

A CMOS inverter can be used as the delay cell of a delay-line ADC[3]. In the first order analysis, the propagation delay t_p of a stage inverter is a function of its supply voltage V_x[5]

$$t_p = k\tau = kR_{eq}C_{eq} = k\frac{L^2}{\mu(V_x - V_{th})} \quad (1)$$

where k is a constant coefficient that depends on the process technology, τ is a basic propagation delay coefficient, R_{eq} and C_{eq} are the MOS transistor's equivalent resistance and capacitance respectively, V_{th} is the MOS device threshold voltage, L is the channel length, and μ is the channel mobility. When $V_{th} \ll V_x$, t_p is approximately inversely proportional to V_x. The delay-line ADC quantitates V_x by testing t_p. However, this quantization principle has two drawbacks. On one hand, as t_p is inversely proportional to V_x, the quantization of V_x by testing t_p is nonlinear. Furthermore, when V_x is small, the linearity of the quantization will become terrible as the requirement of $V_{th} \ll V_x$ cannot be met fully. On the other hand, V_{th} and μ are process technology dependent constants which result in the gain error of delay-line ADC. Though the process variations can be partially decreased by the dual delay-line architecture in the delay-ring ADC, the nonlinearity is not improved at all[4].

2.2 Architecture of ring-ADC

We propose a novel ADC architecture, ring ADC, to solve the problems of nonlinearity and gain error.

The architecture of ring-ADC is shown in Fig. 2, where Ring-A, Ring-B, and Ring-C are uniform and composed of odd numbers of CMOS converters. They operate at different voltages: V_{ref}, V_o, and V_H, where V_{ref} is the programmable voltage reference, V_o is the output voltage of VRM, and V_H is a high settled voltage reference. A, B, and C are pulse signals, with frequencies of f_A, f_B, and f_C, respectively, produced by these three rings. The differential pulse counting discriminator calculates the frequency difference Δf between f_A and f_B. Its ideal transfer function is given by

$$C_e = \text{int}[(f_A - f_B)T_s] = \text{int}[\Delta f T_s] \quad (2)$$

where the function $y = \text{int}[x]$ indicates that y is the integral of x, C_e is the output of ring-ADC, and T_s is the sample time interval generated by N frequency divider. Thus, $T_s = N/f_C$.

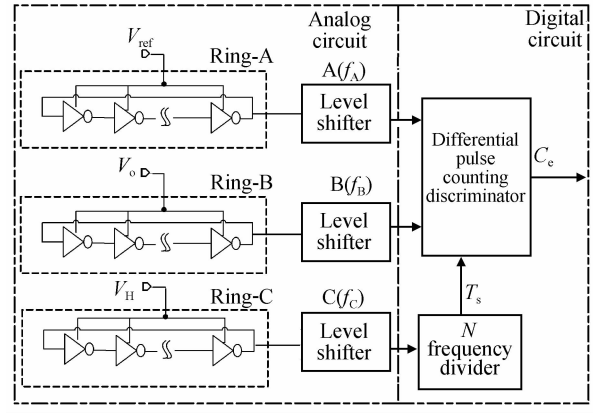

Fig. 2 Architecture of ring-ADC

According to Eq. (1), the frequency of a ring consisting of an M-stage delay cell can be given by

$$f = \frac{1}{T} = \frac{1}{k\tau M} = \frac{\mu(V_x - V_{th})}{kL^2 M} = K_{VCO}(V_x - V_{th}) \quad (3)$$

where $K_{VCO} = \mu/kL^2M$. As K_{VCO} is a constant, f is proportional to V_x. The frequency difference Δf can be expressed as

$$\Delta f = f_A - f_B = K_{VCO}(V_{ref} - V_{th}) - K_{VCO}(V_o - V_{th}) = K_{VCO}\Delta V \quad (4)$$

where $\Delta V = V_{ref} - V_o$. Equation (2) can be rewritten by the substitution of Eq. (4) as

$$\begin{aligned} C_e &= \text{int}[K_{VCO}\Delta V T_s] \\ &= \text{int}\left[K_{VCO}\Delta V \frac{N}{K_{VCO}(V_H - V_{th})}\right] \\ &= \text{int}\left[\frac{N}{V_H - V_{th}}\Delta V\right] \end{aligned} \quad (5)$$

As can be seen from Eq. (5), the high sensitivity to the process technology parameter K_{VCO} is counteracted. It also indicates that the gain of $C_e/\Delta V$ is determined by N and V_H. In our specification, the gain of ring-ADC is $160V^{-1}$, so $C_e/\Delta V = N/(V_H - V_{th}) = 32/200mV = 160V^{-1}$ is required.

In 0.35μm CMOS technology, the process variation of V_{th} is about ± 10%. When V_H = 2.8V, it can be derived from Eq. (5) that the gain error of $C_e/\Delta V$ caused by process variation is about ± 3%. As shown in Fig. 3, the relationship between C_e and V_o is simulated in three different process corners by HSPICE with V_H = 2.8V and V_{ref} = 1.5V. The respective gain errors at the ff and ss corners are +2.8% and −1.5% compared with that at the tt corner. Simulation results verify the theoretical analysis.

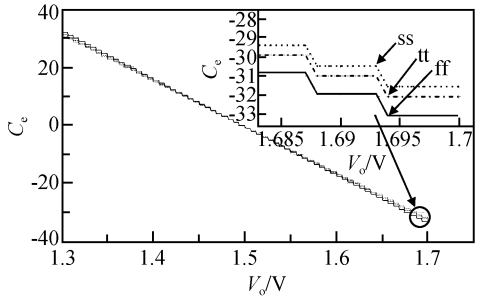

Fig. 3 Relationship between C_e and V_o

3 Realization of ring-ADC

The most important task in the realization of ring-ADC is to design a circuit block to implement the function of Eq. (2). Conventionally, f_A and f_B are evaluated by two accumulator registers. At the end of sample time T_s, C_e equals the difference between these two accumulator registers. However, the configurations of ring-ADC with sampling rate of 500kHz and gain ($C_e/\Delta V$) of $160V^{-1}$ require that f_A or f_B be larger than 80MHz. This will result in high power consumption.

To achieve low power dissipation, a differential pulse counting discriminator is designed. The key idea behind this differential pulse counting discriminator is to use total accumulative phase subtraction to detect the value of Δf, instead of frequency subtraction. The total accumulative phases of A and B during the $n+1$th sample cycle are given by

$$\phi_A^{n+1} = \omega_A T_s + \phi_{A\_begin}^{n+1} \quad (6)$$

$$\phi_B^{n+1} = \omega_B T_s + \phi_{B\_begin}^{n+1} \quad (7)$$

where $\phi_{A\_begin}^{n+1}$, $\phi_{B\_begin}^{n+1}$ are the respective initial phases of A and B at the beginning of the $n+1$th cycle. Then, Δf can be given by

$$\Delta f = f_A - f_B = \frac{\omega_A - \omega_B}{2\pi} = (\omega_A t - \omega_B t)/2\pi t \mid_{t=T_s} = (\phi_A^{n+1} - \phi_B^{n+1} + \phi_{ABR}^{n+1})/2\pi T_s \quad (8)$$

where $\phi_{ABR}^{n+1} = \phi_{A\_begin}^{n+1} - \phi_{B\_begin}^{n+1}$ denotes the initial phase difference between A and B. Hence, Equation (2) can be rewritten as

$$C_e^{n+1} = \mathrm{int}[\Delta f T_s] = \mathrm{int}\left[\frac{\phi_A^{n+1} - \phi_B^{n+1} + \phi_{ABR}^{n+1}}{2\pi}\right] \quad (9)$$

where C_e^{n+1} is the value of C_e in the $n+1$th sample cycle.

Assuming that $C'_e(t) = \mathrm{int}[(\phi_A(t) - \phi_B(t))/2\pi]$ is the integral part of the phase difference between A and B in real time divided by 2π, the value of $C_e'(t)$ in the $n+1$th sample cycle can be expressed as

$$C'^{n+1}_e(t) = \mathrm{int}\left[\frac{\phi_A^{n+1}(t) - \phi_B^{n+1}(t)}{2\pi}\right] \quad (10)$$

where $t \in (nT_s, (n+1)T_s]$. As the value of ϕ_{ABR}^{n+1} is between -2π and $+2\pi$, thus $C_e^{n+1} - C'^{n+1}_e$ may be -1, 0, or $+1$.

Since the sample is continuous, the remaining phase difference between A and B at the end of the nth cycle is set as the initial phase difference between A and B at the beginning of the $n+1$th cycle. Thus, the average error between $\sum_{t=0}^{k} C_e^{n+1+t}$ and $\sum_{t=0}^{k} C'^{n+1+t}_e$ for $k+1$ cycles is given by

$$\lim_{k\to\infty}\left[\left(\sum_{t=0}^{k} C_e^{n+1+t} - \sum_{t=0}^{k} C'^{n+1+t}_e\right)/(k+1)\right] = \lim_{k\to\infty}\frac{\pm 1}{k+1} = 0 \quad (11)$$

C'^{n+1}_e approximates to C_e^{n+1} due to negligible error. As a result, Equation (2) can be implemented by the realization of Eq. (10) instead of the conventional way.

From Eq. (10), $C'^{n+1}_e(t)$ is increased by 1 when $\phi_A^{n+1}(t) - \phi_B^{n+1}(t)$ is increased by 2π. Conversely, $C'^{n+1}_e(t)$ is decreased by 1 when $\phi_A^{n+1}(t) - \phi_B^{n+1}(t)$ is decreased by 2π. A phase/frequency detector (PFD)[6], which is used to detect the phase/frequency difference has the intrinsic capability to carry Eq. (10) out. The operation of a typical PFD is illustrated as follows and shown in Fig. 4. In Fig. 4, the input ports of the PFD are A

and B, and the output ports of the PFD are Q_A and Q_B. When the frequency of input A, f_A, is greater than that of input B, f_B, the PFD produces a positive pulse at Q_A. Q_A is set to 1 by the rising edge transition of A and set to 0 by the rising edge transition of B. An important point in this waveform is that there will be a time interval during which two rising edge transitions of A take place between two rising edge transitions of B. In Fig. 4, these key time intervals occur at the times of $t_1, t_2, t_3 \cdots$. At each of these moments, the accumulative phase difference between A and B is increased by 2π.

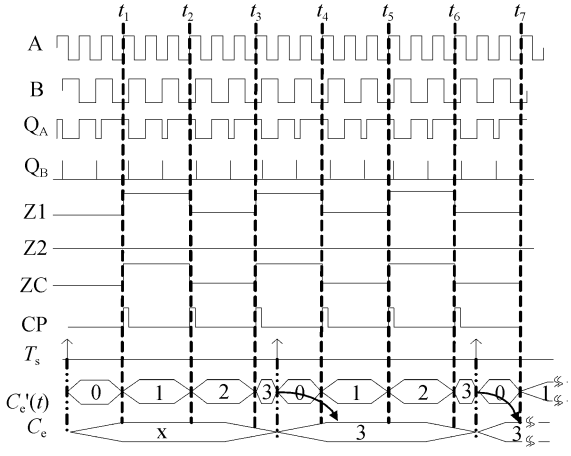

Fig. 4　Waveform of the differential pulse counting discriminator when $f_A > f_B$

The above operation of the PFD can be seen much more clearly from the PFD state diagram shown in Fig. 5. Furthermore, an output function of $C_e'(t)$ is added to the state diagram to record the alteration of $\mathrm{int}[(\phi_A(t) - \phi_B(t))/2\pi]$. In Fig. 5, if the PFD resides in state "I", when the rising edge transition of A occurs, $C_e'(t)$ is increased by 1. In other words, the value of increased phase difference, 2π, is recorded. If the PFD resides in state "II", when the rising edge transition occurs, $C_e'(t)$ is decreased by 1, representing the phase difference between A and B decreased by 2π.

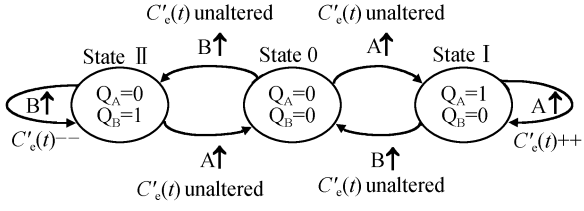

Fig. 5　State diagram of the differential pulse counting discriminator

Thus, Equation (10) can be realized by the state diagram of Fig. 5.

A possible IC implementation of the above state diagram is shown in Fig. 6. It consists of a PFD, a pulse generator (PG), an exclusive or gate (XOR), an edge detector, a pulse counter, and a flip-latch. The state equation of the PG is given by

$$Z^{m+1} = Z^m \oplus Q_X \tag{12}$$

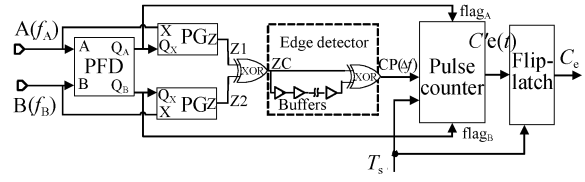

Fig. 6　Block diagram of the differential pulse counting discriminator

The PG is triggered by the rising edge of X. When $Q_X = 1$, then $Z^{m+1} = -Z^m$; when $Q_A = 0$, then $Z^{m+1} = Z^m$. The PG is designed to detect the occurrence of the rising edge transition of A when the PFD is in state "I", and detect the occurrence of the rising edge transition of B when the PFD is in state "II". The edge detector is designed to detect the rising/falling edge transition of ZC. It generates a positive pulse on the CP when a rising/falling edge transition of ZC arrives. When $f_A > f_B$, the waveform of the differential pulse counting discriminator is illustrated in Fig. 4. According to Eq. (8) and the state diagram of Fig. 5, it can be derived that the frequency of CP is equal to $\Delta f = f_A - f_B$. The pulse counter computes the frequency Δf of the signal CP. When the CP is on the rising edge transition and $\mathrm{flag}_A = 1$ ($V_{ref} > V_o$), the value of the pulse counter $C_e'(t)$ is increased by 1. Conversely, when the CP is on the rising edge transition and $\mathrm{flag}_B = 1$ ($V_{ref} < V_o$), the value of the pulse counter $C_e'(t)$ is decreased by 1. As shown in Fig. 4, when the sample time T_s is over, the value of the pulse counter $C_e'(t)$ is put to C_e by the flip-latch. After that, $C_e'(t)$ is reset to zero and counts the frequency of the CP in the next sample cycle. When the VRM works in steady state, the output voltage V_o settles in the range of $|V_o - V_{ref}| < 1\mathrm{LSB}$. That means $\Delta f < 500\mathrm{kHz}$ and the differential pulse counting discriminator will work in a state of very low power consumption.

4 Experimental results

Figure 7 shows a photograph of the digital VRM controller and the layout of the ring-ADC. The DNL and INL, shown in Figs. 8(a) and (b), are 0.92LSB and 1.2LSB, respectively. In a set of 10 sample chips, the maximum integral nonlinearity performance is 1.3LSB and gain error is ±3.85%, which are about the same as the simulation results. A typical output fast Fourier transform (FFT) spectrum is shown in Fig. 8(c). It exhibits that the SFDR is 65.7dB. The relationship between power consumption of the ring-ADC and the value of the differential input voltage is shown in Fig. 8(d). When the VRM works in steady-state ($|V_o - V_{ref}| < 1$LSB), the power consumption of the ring-ADC is 2.56mW. Table 1 summarizes the measured performance of the ring-ADC compared with the delay-ring ADC. Expressed as a percentage of the full scale range, the INL of the ring-ADC is 1.87%, which is much smaller than that of the delay-ring ADC. It also exhibits that the ring-ADC holds the advantages of much smaller gain error and better resolution than the delay-ring ADC.

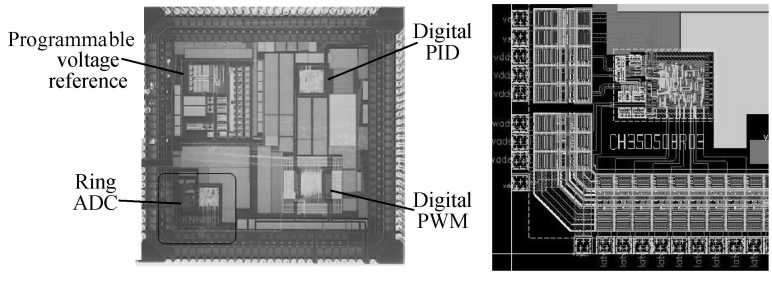

Fig. 7 Photograph of the VRM and layout of ring-ADC

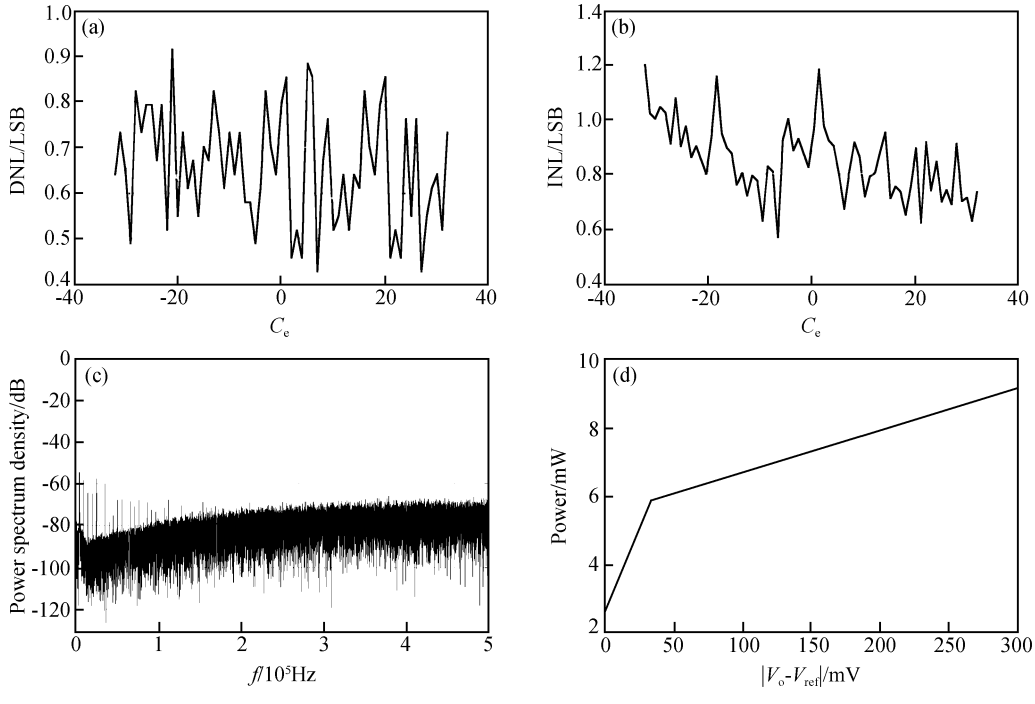

Fig. 8 Analysis of ring-ADC's measurement (a) DNL; (b) INL; (c) Typical FFT spectrum at 5kHz@500kHz; (d) Ring-ADC's power consumption versus differential input voltage

Table 1　Summary of measurement performance

	This work (Ring-ADC)	Delay-ring ADC[4]
Process	0.35μm CMOS	0.35μm CMOS
Resolution/bit, Range/mV, 1LSB/mV	6, ±200 around V_{ref}, 6.25	3, ±120 around V_{ref}, 30
Sampling rate/MHz	0.5	1
DNL, INL, Gain error/%	0.92LSB, 1.2LSB (1.87%), ±3.85	0.5LSB, 1.1LSB (13.75%), ±10
SFDR/dB, SNAD/dB, ENOB/bit 1kHz@500kHz	65.7, 30.1, 4.7	No data
Power consumption@3.3V /mW (When VRM works in steady state)	2.56	1.62
Active area/mm^2	0.075	0.025

5　Conclusion

The design and implementation of a novel architecture of ADC are presented. The proposed ring-ADC has the features of built-in noise immunity, good linearity, and precise calibration against process variations. With the use of a differential pulse counting discriminator, the power consumption of the ring-ADC is reduced to 2.56mW at a 500kHz sampling frequency. As a result, the ring-ADC is suitable for low power applications of a digital VRM controller.

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适用于 VRM 数字控制芯片的新结构 ADC*

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摘要： 提出了一种适用于主板电压调整模块(VRM)数字控制芯片的新结构 ADC——延迟环 ADC 的设计和实现方法. 运用延时环(或称环路压控振荡器)的电压-频率转换原理实现对电压信号的模数转换，提高了线性度，减小了工艺偏差；设计差分脉冲计数式鉴频器，降低了延迟环 ADC 功耗. 在标准 0.35μm CMOS 工艺环境下流片实现，测试结果表明延迟环 ADC 的微分线性误差和积分线性误差分别为 0.92LSB 和 1.2LSB，最大增益误差为 ±3.85%，当 VRM 工作于稳定状态，延迟环 ADC 在采样频率为 500kHz 下工作的平均功耗为 2.56mW. 延迟环 ADC 满足 VRM 数字控制芯片应用要求.

关键词： 主板电压调整模块；直流/直流；延迟环 ADC；延迟线 ADC；差分脉冲计数式鉴频器

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