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New Lateral Super Junction MOSFETs with n$^+$-Floating Layer on High-Resistance Substrate*

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Abstract: A new super junction LDMOST structure that suppresses the substrate-assisted depletion effect is designed with an n$^+$-floating layer embedded in the high-resistance p-type substrate by implanting phosphor or arsenic. This effect results from a charge imbalance between the n-type and p-type pillars when the n-type pillars are depleted by p-type substrate. The high electric field around the drain is reduced by the n$^+$-floating layer due to the REBULF effect, which causes the redistribution of the bulk electric field in the drift region, and thus the substrate supports more biases. The new structure features high breakdown voltage, low on-resistance, and charge balance in the drift region.

Key words: super junction; LDMOST; substrate-assisted depletion; n$^+$-floating layer; breakdown voltage
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1 Introduction

The lateral double diffused MOSFET (LDMOS) structure has been widely used in intelligent power applications because its process is compatible with VLSI processes and it is easy to integrate with other devices. The performance goal in LDMOS is to use the lowest specific on-resistance ($R_{on,sp}$) to minimize conduction loss. Several technologies have been proposed, such as reduced surface field (RESURF) LDMOS[1], new structures based on RESURF technology[2~4], PSOI with a p-type buried layer[5], and the buried oxide double step MOSFET[6]. LDMOS based on the super junction concept[7], in which the n-type drift region of the RESURF LDMOS is replaced by a set of alternating highly doped n- and p-type semiconductor pillars, was recently proposed to further improve the trade-off characteristics between the breakdown voltage (BV) and the specific on-resistance ($R_{on,sp}$), which has always been a major issue in the design of power devices. However, the p-type pillars of the SJ-LDMOST implemented on a p-substrate cannot be depleted completely before the electric field of the silicon reaches its critical breakdown. This results from charge imbalance due to the substrate-assisted depletion effect[8] by depleting n-type pillars to degrade the BV of the device. To eliminate this effect, several structures have been reported[9~11].

In this paper, a novel SJ-LDMOST with n$^+$-floating layer (n$^+$-floating SJ-LDMOS) embedded in the high-resistance substrate (Fig. 1) is proposed for the first time to suppress the charge imbalance effect, and an important REBULF effect[12] is introduced by an n$^+$-floating layer. The high electric field around the drain is reduced by the n$^+$-floating layer, and the bulk electric field is redistributed in the drift region due to the REBULF effect.

2 Device structure and description

Figure 1 shows the proposed n$^+$-floating SJ-LDMOST. The key feature of the structure is the use of an n$^+$-floating layer with a concentration of more than $1\times10^{17}\,cm^{-3}$ in the high-resistance substrate (N_s), and the distance from the n$^+$-floating layer to the bottom of the drift region is W, which must be less than the thickness of the depletion layer (W_p) in the substrate of a conventional SJ-LDMOS. N_D and N_A are the peaks of the concentration of n- and p-type pillars made by ion

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implantation and diffusion, respectively. L_d is the length of the super junction layer. h, W_N and W_P are the height and widths of the n- and p-type pillars, and are 1μm throughout the following discussion. As the drain voltage of the device is increased in the off-state, the n-pillars of the n + -floating SJ-LDMOST are depleted by the neighboring p-pillars, as well as by the p-type substrate above the n^+-floating layer. The p-pillars start to be affected by the n^+-floating layer after the p-type charge above n^+-floating is fully depleted at a high enough drain voltage. In the n^+-floating SJ-LDMOST structure, both pillars are affected by the vertical depletion effect due to the electric field in the y axial direction, which results in the charge balance between the pillars. In the conventional SJ structure, only the n-pillars are affected by the p-type substrate.

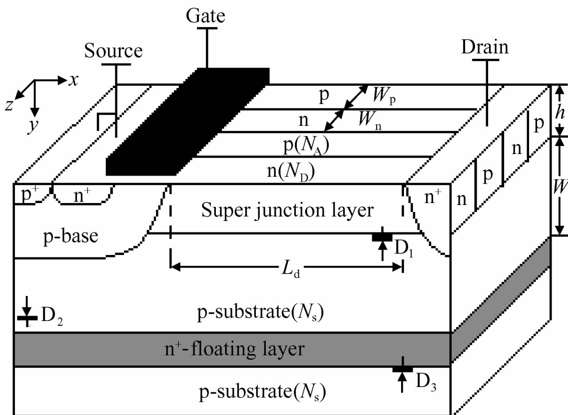

Fig. 1 Three-dimension view of the n^+-floating SJ-LDMOST

The potential of the n^+ layer is floated up when the depletion layer spreads into its region, and thus the high electric field around the drain is reduced by the redistribution of the bulk electric field in the drift region, and the high-resistance substrate supports more biases due to the parallel plane D_3 junction. This instance is different from Ref. [13] in which the n^+-floating layer is embedded into p^+ substrate. A high breakdown voltage could not be obtained in Ref. [13] due to the absence of the parallel plane junction D_3.

3 Simulation results

Figure 2 shows the simulated potential contours at the breakdown using simulation software ISE[14] for the proposed n^+-floating SJ-LDMOST and the conventional SJ-LDMOST. It is clear that the breakdown occurs at the surface of the conventional SJ-LDMOST (Fig. 2(a)) due to electric field crowding and the p-type pillars cannot be depleted completely for charge imbalance effect. Thus the breakdown voltage is limited to 147V. However, compared with a conventional SJ-LDMOST, there are two significant differences for the proposed n^+-floating SJ-LDMOST (Fig. 2 (b)). First, both p- and n-type pillars are depleted completely at breakdown due to the fact that charge balance is obtained in the proposed structure. Second, a significant part of the potential contours gets pulled out toward the source region due to the presence of the n^+-floating layer, by which the electric field around the drain is reduced due to the REBULF effect (shown in Fig. 3 (a)), thus the potential across the D_1 junction has been reduced significantly, and the breakdown of the n^+-floating SJ-LDMOST occurs at the D_1 and D_2 junctions simultaneously in the best case, which allows the breakdown voltage to reach 263V.

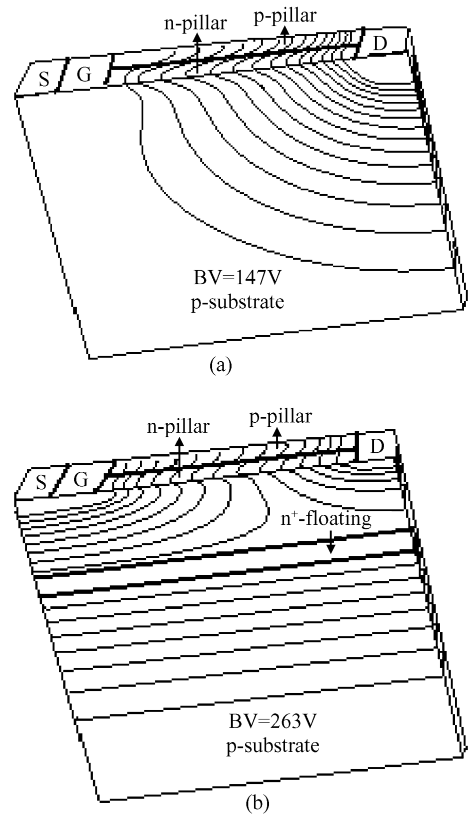

Fig. 2 Potential distributions of the conventional (a) and n^+-floating SJ-LDMOS (b) L_d = 15μm, N_D = N_A = 5.0 × 10^{16} cm^{-3}, N_s = 1.2 × 10^{14} cm^{-3}, W = 18μm, W_p = 22μm

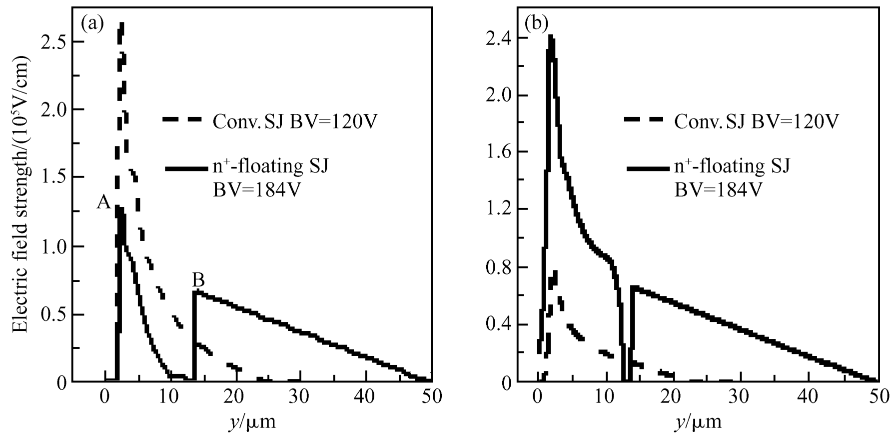

Fig.3 Vertical electric field profiles around the drain (a) and the source (b) for the conventional and n^+-floating SJ-LDMOS $L_d = 10\mu m$, $W = 16\mu m$, $N_D = N_A = 5.0 \times 10^{16} cm^{-3}$, $N_s = 1.2 \times 10^{14} cm^{-3}$

The vertical electric field distributions around the drain and source are shown in Fig.3. Under reverse bias, the electric field around the drain of the n^+-floating SJ-LDMOST (Fig.3(a)) is divided into two parts (their peaks are denoted by A and B), which were produced by junctions D_1 and D_2. In this way, the maximal electric field around the drain becomes lower than that of the conventional SJ-LDMOST. It can be seen from Fig.3(b) that the strength and area of electric field distribution near the source in the n^+-floating SJ-LDMOST are larger than that of the conventional SJ-LDMOST. This is a result of the depletion layer spreading into source region.

The effect of the doping imbalance on the BV for the n^+-floating SJ-LDMOST and conventional SJ-LDMOST are compared in Fig.4. The maximum breakdown voltage V_A in the n^+-floating SJ-LDMOST is increased drastically by ΔV_1 compared with V_B in the conventional SJ-LDMOS due to suppression of the imbalance charge ΔQ, and increased by ΔV_2 compared with V_C in the lateral unbalanced SJ-LDMOS[10] due to the REBULF effect.

The optimum W is applied in accordance with Fig.5 that shows the relation of the breakdown voltage and W in the n^+-floating SJ-LDMOS. It is clear that the breakdown voltage peaks when the REBULF condition is satisfied. This indicates that the optimum REBULF condition is achieved as the height of the electric field at points A and B (shown in Fig.3(a)) is equal, which causes the breakdown to occur at junctions D_1 and D_2, simultaneously.

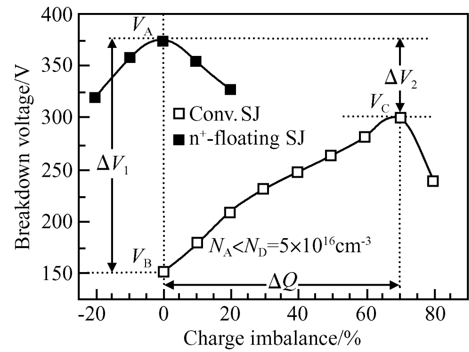

Fig.4 Breakdown voltage versus doping imbalance for the conventional and n^+-floating SJ-LDMOS $L_d = 30\mu m$, $W = 22\mu m$, $N_s = 1.2 \times 10^{14} cm^{-3}$

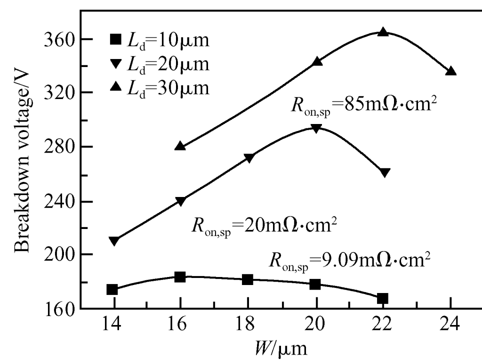

Fig.5 Breakdown voltage versus W for the n^+-floating SJ-LDMOS $N_D = N_A = 5.0 \times 10^{16} cm^{-3}$, $N_s = 1.2 \times 10^{14} cm^{-3}$

In practical implementation of the n^+-floating SJ-LDMOST, the additional steps needed to implement the device involve implanting phosphor or arsenic into the p-substrate to form the n^+-floating layer and the substrate above the n^+-

floating layer generated by epitaxy. Although the n^+-floating layer will diffuse out due to the thermal cycle, its total dose could be kept from changing, which would not affect the REBULF condition to suppress the substrate-assisted depletion effect.

Figure 6 shows the on-state I_{DS}-V_{DS} characteristics of the n^+-floating SJ-LDMOST with the breakdown voltage of 117V and the RESURF LDMOS based on RESURF technology[1] with the breakdown voltage of 103V. It indicates that the on-resistance of the n^+-floating SJ-LDMOST is much lower than that of the RESURF LDMOST due to highly doped n-type semiconductor pillars, which can be explained in Ref. [15].

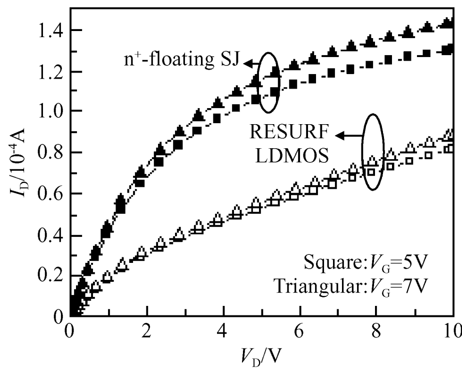

Fig. 6　On-state characteristics of the RESURF LDMOS and n^+-floating SJ-LDMOS　$L_d = 10\mu m$, $W = 16\mu m$, $N_D = N_A = 5.0\times10^{16} cm^{-3}$, $N_s = 1.2\times10^{14} cm^{-3}$

In general, the longer the drift region is, the higher the breakdown voltage will be. However, it should be noted that the breakdown voltage of the device will also saturate due to the saturation of the vertical breakdown voltage. In the n^+-floating SJ-LDMOST structure, the saturated length of the drift region is larger than that of the conventional SJ-LDMOST since the vertical breakdown voltage of the n^+-floating SJ-LDMOST is higher than that of the conventional SJ-LDMOST due to the REBULF effect. The maximum breakdown voltage of the n^+-floating SJ-LDMOST reaches 440V, compared with that of 150V in the conventional SJ-LDMOST.

The $R_{on,sp}$ of the n^+-floating SJ-LDMOS and the RESURF LDMOS versus BV with various L_d are compared in Fig. 8 with an applied gate voltage V_g of 6V and gate oxide thickness G_{ox} of 40nm. The comparison clearly demonstrates that the $R_{on,sp}$ of the n^+-floating SJ-LDMOS is almost

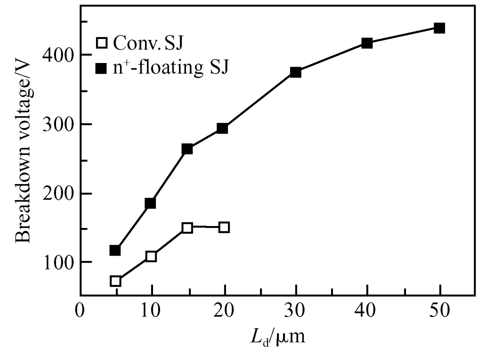

Fig. 7　Breakdown voltage versus the length of drift region for the conventional and n^+-floating SJ-LDMOS　$h = 1\mu m$, $N_s = 1.2\times10^{14} cm^{-3}$

the same as that of RESURF LDMOS at the low breakdown voltage compared with the high-voltage because the whole on-resistance of a low voltage LDMOS is dominated by the resistance in the channel region[16], compared to the high-voltage LDMOS dominated by the resistance of the drift region. In the n^+-floating SJ-LDMOS, a set of alternating and highly doped n- and p-type semiconductor pillars replace the n-type drift region of the RESURF LDMOS, which causes the on-resistance to decrease especially with the high breakdown voltage.

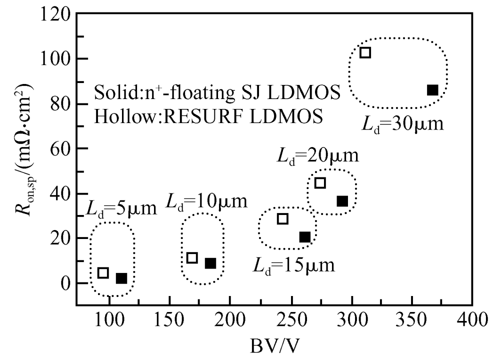

Fig. 8　$R_{on,sp}$ versus BV for the RESURF LDMOS and n^+-floating SJ-LDMOS　$G_{ox} = 40nm$, $V_g = 6V$

4　Conclusions

A new SJ-LDMOS structure that employs an n^+-floating layer embedded in high-resistance substrate was analyzed. This structure eliminates charge imbalance by suppressing the substrate-assisted depletion effect to achieve high breakdown voltage while maintaining low on-resistance resulting from the effect on the n- and p-type pillars of the p-type substrate and n^+-floating, which causes

the charge balance between the pillars. In addition, the vertical electric field distributions around the drain are reduced due to the REBULF effect, improving the saturated breakdown voltage in the n^+-floating SJ-LDMOST compared to that in the SJ-LDMOS without n^+-floating layer. The reduced specific on-resistance is obtained in the n^+-floating SJ-LDMOS compared with the RESURF LDMOS with the high breakdown voltage due to highly doped n-type semiconductor pillars.

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高阻衬底上具有n^+浮空层的横向 Super Junction MOSFETs*

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摘要： 提出了一种具有n^+浮空层的横向 super junction 结构，此结构通过磷或砷离子注入在高阻衬底上形成n^+浮空层来消除传统横向 super junction 结构中的衬底辅助耗尽效应.这种效应来源于 p 型的衬底辅助耗尽了 super junction 区的 n 型层，使 p 与 n 之间的电荷不能平衡.n^+层的 REBULF 效应通过使漏端电场减小，体电场重新分布而使新结构中的衬底承担了更多的电压.结果表明这种结构具有高的击穿电压、低的导通电阻和漂移区中电荷平衡的特点.

关键词： super junction；LDMOST；衬底辅助耗尽；n^+-浮空层；击穿电压

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