Two-Stage Driving Circuit for One-Chip TFT-LCD Driver IC*

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Abstract: A two-stage driving circuit of a one-chip TFT-LCD driver IC for portable electronic devices is proposed. The driving buffers of the new circuit are built in the γ-correction circuit rather than in the source driver. The power consumption, die area, and driving capability of the driving circuit are discussed in detail. For a two-stage driving circuit with 13 driving buffers, the settling time of the driving voltage within 0.2% error is about 19.2μs when 396 pixel-loads are driven by the same grayscale voltage. The quiescent current of the whole driving circuit is 518μA, and the power consumption can be reduced by 77%. The proposed driving circuit is successfully applied in a 132RGB×176-dot, 260k color one-chip driver IC developed by us for the TFT-LCD of mobile phone, and it can also be used in other portable electronic devices, such as PDAs and digital cameras.

Key words: TFT-LCD; source driver; γ-correction; grayscale voltage
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1 Introduction

With the rapid development of VLSI and mobile communication technologies, portable electronic devices, such as cell phones and PDAs have been widely used in people's daily life. Because TFT-LCD has many advantages such as high luminance, high image quality, fast response time, and low power consumption, it is widely applied in all kinds of portable electronic devices. The TFT-LCD driver IC is one of the key parts in LCM (LCD module), which directly affects the image quality and power dissipation of LCM.

Currently, TFT-LCD driver ICs can be classified into two kinds. One is the multi-chip solution applied for large TFT-LCD panels, which consists of a source driver IC, gate driver IC, TCON IC, etc, and in which driving buffers are connected to the outputs of the source driver[1]. The other is the one-chip solution applied for portable electronic devices that use a battery power supply[2~5], for which all functional blocks used for large TFT-LCD driver ICs are integrated in a one-chip driver IC in order to reduce die area and power consumption. Small die area can decrease the chip cost, and low power dissipation can lengthen battery's working life.

The settling time of the source driver output voltage is an important factor for a one-chip driver IC. A large driving ability can yield better image quality. Currently, for 260k color TFT-LCD one-chip driving ICs, the power consumption is under 5mW in the module; the die area is about 20.69mm × 2.47mm; and the settling time is less than 35μs[3~4]. However, the circuits of driver ICs must be optimized further in order to achieve lower power consumption and chip cost.

In this paper, we proposed a two-stage driving circuit for one-chip TFT-LCD driver IC. The driving buffers are placed in the part outputs of γ-correction circuit rather than in the every outputs of it, and thus the number of driving buffers is reduced greatly as compared with the conventional driving circuit. Considering the trade-off for the power consumption, the die area and the driving capability, a typical two-stage driving circuit with 13 driving buffers is designed which is satisfying the requirement of driving circuit with 13 driving buffers is designed which is satisfying the requirement of driving capability. The designed driving circuit is successfully applied in 132RGB × 176-dot, 260k color one-chip driver IC developed by us for TFT-LCD of mobile phone.

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2 Driving circuits of one-chip driver IC

A block diagram of an LCM using a one-chip driver IC[2~5] is shown in Fig. 1. The driving buffer of a one-chip driver IC is usually connected to the output of the γ-correction circuit while the source driver block is only used as a digital-to-analog converter.

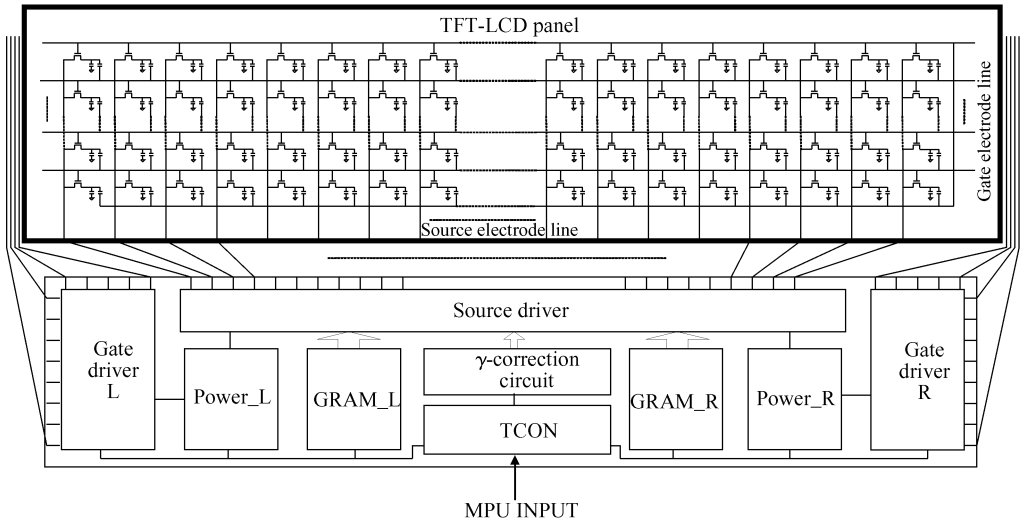

Fig. 1 Block diagram of LCM using one-chip driver IC

The timing controller (TCON), gate driver, source driver, γ-correction circuit, DC-DC converters, and graphic RAM are typical circuit blocks for a one-chip driver IC. TCON generates controlling signals and timing clocks for the whole driver IC. The gate driver and source driver generate line driving voltages and column driving voltages, respectively. The γ-correction circuit generates grayscale voltages corresponding to input digital display data. The DC-DC converters generate operational voltages of all blocks and driving voltages for the panel. Graphic RAM is used to store one frame of digital display data.

In the one-chip driver IC, the γ-correction circuit generates full-scale grayscale voltages appended with driving buffers at the outputs, and the source driver selects the proper grayscale voltages by D/A converter according to input digital display data and then outputs to the LCD panel to display the color images. Figure 2 shows the conventional driver architecture of a one-chip driver IC for a small TFT-LCD.

In Fig. 2, the driving voltage buffers are included in the γ-correction circuit and the source driver is only used to select the grayscale voltages. This is different from the source driver IC for a large TFT-LCD panel where the driving voltage buffers are included in every source driver[6]. The number of driving buffers in Fig. 2 is smaller than that of the source driver IC for a large TFT-LCD panel so that the die area and power dissipation of the driver IC can be reduced greatly.

3 Load analysis of TFT-LCD panel and driving capability requirement

3.1 Load analysis of TFT-LCD

The equivalent load of one pixel in a TFT-LCD panel can be modeled by a five-stage serial RC circuit or a one-stage RC circuit[7], as shown in Figs. 3 (a) and (b). A one-stage RC equivalent circuit is suitable for a small TFT-LCD panel because the area of sub-pixels is small and the length of ITO and metal (Cr/Al) line is short as compared with large TFT-LCD. R_t is the equivalent resistance when the TFT is on, and C_{total} is the equivalent capacitance of the sub-pixel. The values of R_t and C_{total} are different for all sizes of TFT-LCD panels, but for a 50mm TFT-LCD panel, the equivalent RC loads of one sub-pixel are about $R_t = 10k\Omega$ and $C_{total} = 20pF$.

In Fig. 2, the load impedances of the driving voltage buffers are different from each other depending on the input digital display data. For the best situation, the digital display data are different from each other so that every grayscale voltage

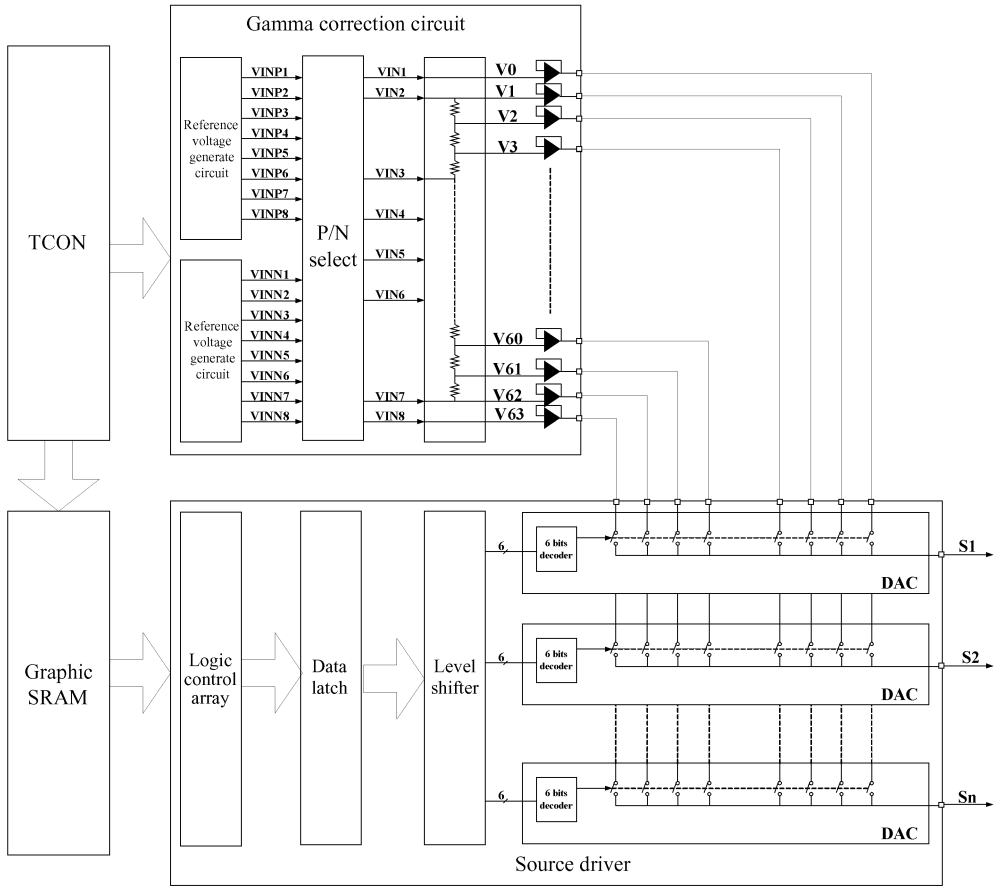

Fig. 2　Conventional driver architecture of one-chip driver IC for small TFT-LCD

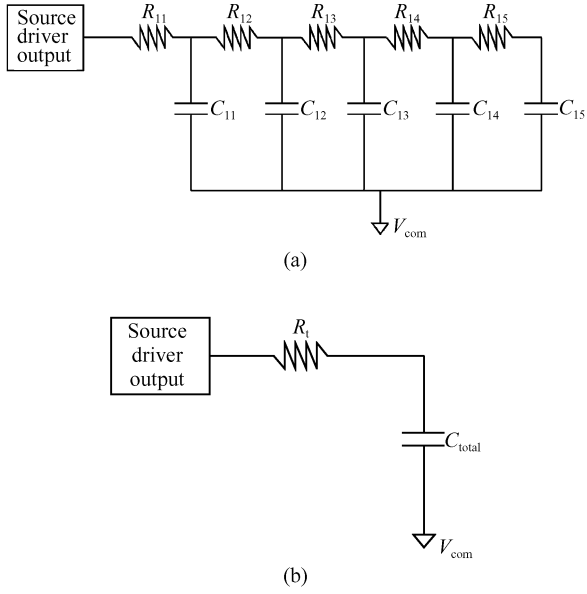

Fig. 3　Load models of TFT-LCD panel　(a) Five-stage serial RC circuit; (b) One-stage RC circuit

(also every driving buffer) drives only one sub-pixel, and the load impedance of every driving buffer is R_t and C_{total}. However, in the worst situation, the digital display data all have the same value so that the whole line of sub-pixels are driven by one grayscale voltage (also by one driving buffer). If there are N sub-pixels in a line, then N sub-pixels are paralleled for a driving buffer, so that the total load impedance of one driving buffer is $R_t^N = \dfrac{R_t}{N}$ and $C_{total}^N = NC_{total}$.

3.2　Driving capability requirement

The settling time of the grayscale voltage is the sum of the SR limiting settling time (T_{SR}) and the small signal settling time (T_{SS})[6]. In this paper, the settling time of the driving voltage is defined as the time that the output voltage of the driving buffer takes to rise from zero to the grayscale voltage V_g within $\pm 0.2\%$ error at the worst load condition (R_t^N and C_{total}^N).

For a one-chip TFT-LCD driver IC, T_S is determined by the minimum row period $T_{row,min}$ and maximum charge sharing time $T_{charge\_share,max}$; their relationship is as follows[4,5]:

$$T_s < T_{row,min} - T_{charge\_share,max} \quad (1)$$

This relationship ensures that the liquid pixels and storage capacitor can be charged to grayscale voltage in a row period.

For a 132RGB×176-dot, 260k color one-chip driver IC of a TFT-LCD used for a mobile phone, $T_{row,min} - T_{charge\_share,max} = 40\mu s$, We need $T_s < 30\mu s$ ($10\mu s$ for margin), and $T_{SR} < 20\mu s$, $T_{SS} < 10\mu s$.

4 Driving architecture with buffers built into the γ-correction circuit

4.1 One-stage driving architecture with 8 driving buffers

In order to further reduce the power consumption and the die area, the circuit shown in Fig. 2 can be simplified to the one-stage architecture shown in Fig. 4 with 8 built-in buffers in the γ-correction circuit, where the driving buffers are moved from the outputs of the γ-correction circuit to the outputs of 8 reference voltages circuit, and the number of driving buffers is reduced from 64 to 8.

4.2 Load analysis of one-stage driving architecture

In this architecture, 8 reference voltages (VIN0～VIN7) are driven by 8 OPAMP buffers and are then applied to the resistance-string circuit to generate 64 level grayscale voltages. The loads of buffers consist of three parts: the equivalent loads of the TFT-LCD panel, the on-resistance of the 6-bit DAC, and the resistance in resistance-string of the γ-correction circuit. The loads of the buffers are different when digital display data from the MPU is changed.

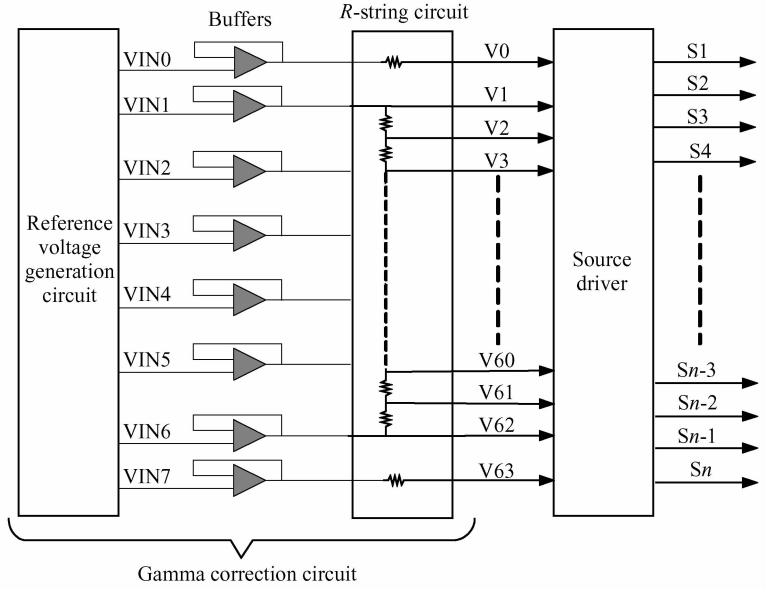

Fig. 4 One-stage driving architecture with 8 built-in driving buffers

In the worst load situation, the loads for whole lines of pixels are driven by one grayscale voltage V_{gm+1}, as shown in Fig. 5. VINn and VIN $n+1$ are two adjacent reference voltages, and R_{g1} and R_{g2} are the equivalent resistances in the resistance-string. For BUF1, the circuit shown in Fig. 5 can be equivalently simplified to the circuit shown in Fig. 6(a).

If the on-resistance of the analog switch in the source driver is R_s, the output impedance of BUF1 is

$$Z_L = \frac{(NR_{g1} + R_s + R_t)R_{g2}C_{total}s + R_{g2}}{[N(R_{g1} + R_{g2}) + R_s + R_t]C_{total}s + 1} = R_{eq} + \frac{1}{C_{eq}s} \quad (2)$$

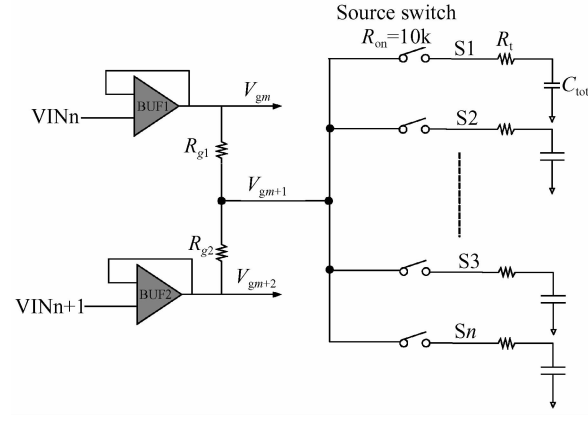

Fig. 5 Equivalent load model of one-stage driving architecture in the worst situation

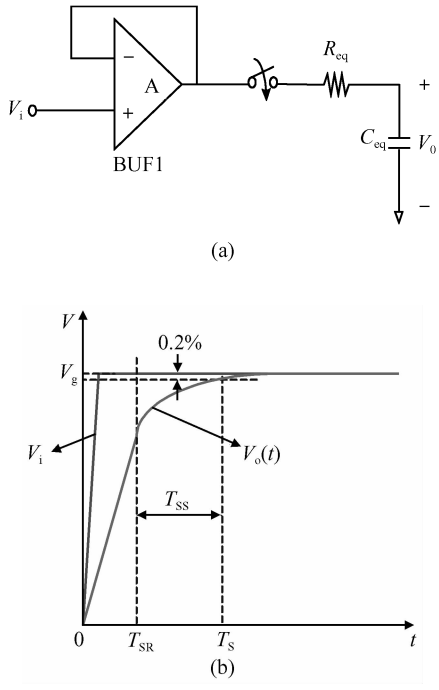

Fig. 6　Load equivalent circuit of BUF1 and its step voltage response　(a) Equivalent circuit; (b) Step voltage response

When R_{g2} is large enough, the quiescent current of R_{g2} is very little as compared with the charging current of loads, and so R_{g2} can be ignored, thus we have,

$$R_{eq} = R_{g1} + \frac{R_s + R_t}{N} \tag{3}$$

$$C_{eq} = NC_{total} \tag{4}$$

Thus the time constant τ for the output load of BUF1 is

$$\tau = R_{eq}C_{eq} = (NR_{g1} + R_s + R_t)C_{total} \tag{5}$$

4.3 Settling time analysis

For the circuit shown in Fig. 6 (a), C_{eq} is charged by the output voltage of the buffer through the resistance R_{eq} when the switch is ON. The capacitor charging process when the input is applied by a step voltage can be considered as follows. From start to T_{SR}, the driving buffer experiences a slew rate process, and the voltage of C_{eq} rises with a constant slope of SR. When $t > T_{SR}$, BUF1 operates under a linear small signal process, the voltage of C_{eq} rises exponentially until the output voltage V_o equals the input voltage V_i, as shown in Fig. 6 (b).

Assuming the driving buffers are two-stage OPAMPs with bias current I_{bias} and open loop gain A, and a Miller capacitor C_c is used to improve the phase margin, then the slew rate can be written as[8,9]

$$SR = \frac{dV_o}{dt} = \frac{I_{bias}}{C_c + C_{eq}} \tag{6}$$

Because the slew rate process is over at T_{SR}, the output voltage of BUF1 at this time is

$$V_{o1} = SR \times T_{SR} \tag{7}$$

When $t > T_{SR}$, the driving buffer is assumed to be in a linear small signal process, and we have

$$\frac{V_o(s)}{V_i(s)} = \frac{A}{1+A} \times \frac{1}{1+\tau s} \tag{8}$$

Thus the step voltage response can be obtained by inverse Laplace transform as

$$V_o = V_i \frac{A}{1+A}(1 - e^{-\frac{t}{\tau}})U(t) \tag{9}$$

Then the voltage of capacitor C_{eq} can be obtained as

$$V_o(t) = \begin{cases} SR \times t, & 0 < t \leqslant T_{SR} \\ V_{o1} + (V_g - V_{o1})\dfrac{A}{1+A}(1 - e^{-\frac{t-T_{SR}}{\tau}}), & t > T_{SR} \end{cases} \tag{10}$$

At time T_S

$$\frac{|V_o(t) - V_g|}{V_g} \times 100\% \leqslant 0.2\% \tag{11}$$

We have

$$T_S = T_{SR} + \tau \ln\left\{\frac{\left(1 - \frac{V_{o1}}{V_g}\right)\frac{A}{1+A}}{\left(1 - \frac{V_{o1}}{V_g}\right)\frac{A}{1+A} - 0.998 + \frac{V_{o1}}{V_g}}\right\} \tag{12}$$

From Eq. (12), it is observed that T_S depends on A, SR, τ and V_g. When A is large enough, we have

$$T_S = T_{SR} + \tau\left[\ln\left(1 - \frac{V_{o1}}{V_g}\right) + 6\right] \tag{13}$$

According to Eq. (13), T_S is determined mainly by T_{SR}, τ, and V_{o1}/V_g, and T_S is larger when T_{SR} and τ are larger or V_{o1}/V_g is less. For fixed V_{o1}/V_g, T_{SR} is the main factor of T_S, so we can increase the SR of the driving buffer to reduce T_s. Further, τ is another important factor for reducing T_s. Since C_{total} and R_t are the load of the TFT-LCD panel and cannot be changed, reducing the values of R_s and R_{g1} is the only way to reduce τ according to Eq. (4).

An analog switch with a 6bit decoder circuit can be used in the source driver so as to obtain a low R_s. However, there are two methods to reduce R_{g1}: one is reducing the value of unit resistance in the grayscale voltage generating circuit (resist-

ance-string), and the other is changing the topology of the driving circuit. However, if the value of unit resistance is reduced, the quiescent current of the resistance-string circuit will be increased, which is not desirable for a TFT-LCD driver IC. Consequently, it is necessary to change the driving buffers' architecture to increase T_s but without increasing the power dissipation.

The driving buffers' architecture can be changed by adding additional driving buffers into the γ-correction circuit at the proper place of the resistance-string circuit. For example, in the circuit shown in Fig. 5, another voltage driving buffer can be added between BUF1 and BUF2. Its input (or output) voltage is between VINn and VIN$n+1$, and as a result, the load conditions of the driving buffers are changed and R_{g1} is reduced.

4.4 Two-stage driving circuit with 13 driving buffers

The properties of the driving architecture shown in Fig. 4 can be improved by increasing the number of driving buffers. As shown in Fig. 7, five additional buffers are added into the γ-correction circuit, which is called a two-stage driving architecture. In this new driving architecture, the number of reference voltages appended with driving buffers at the outputs is increased from 8 to 13, so the R_{g1} of each buffer is reduced, and also T_s can be expected to decrease.

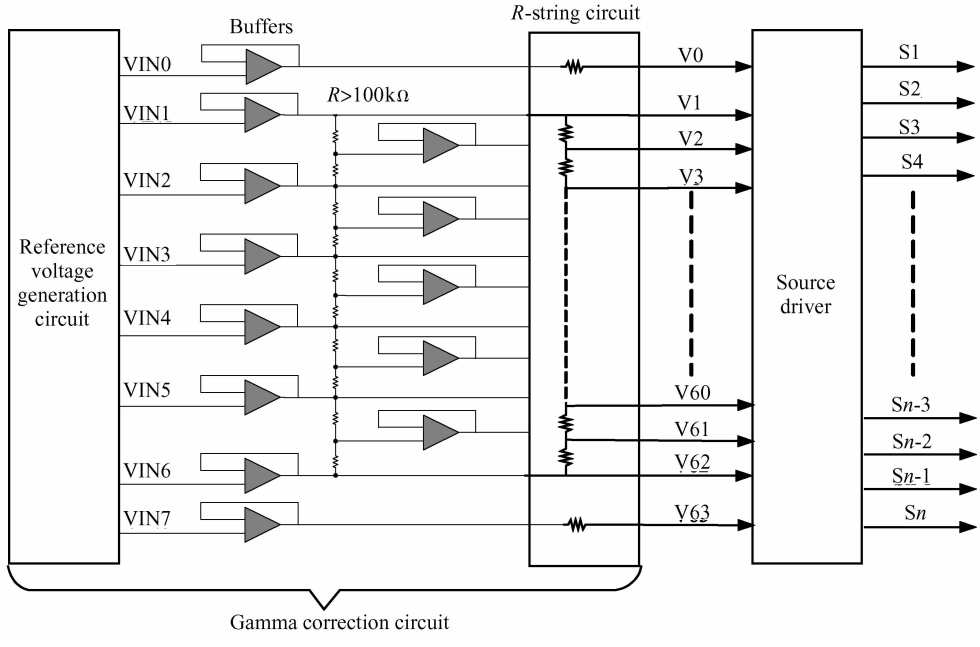

Fig. 7 Two-stage driving architecture with 13 driving buffers

The two-stage driving architecture is formed as follows. The 8 first-stage driving buffers are added at each of the outputs of the 8 reference voltages (VIN0 ~ VIN7), two large resistances (larger than 100kΩ) for voltage division are connected between outputs of two adjacent buffers for the middle reference voltages (VIN1 ~ VIN6), and then the 5 second-stage driving buffers are added between the division resistances and grayscale voltage generating circuit (resistance-string). Then the outputs of the second-stage buffers are connected to the resistance-string circuit accordingly without changing the grayscale voltages division ratio. With the increase of the unit resistance in the grayscale voltage generating circuit (resistance-string), the quiescent current will be reduced, but the circuit area will increase, and the resistance load of the buffers will increase so that the settling time will be affected. A tradeoff between the unit resistance value (power consumption and die area) and the settling time needs to be made.

5 Simulation and measurement results

The driving circuits using the two-stage driv-

ing architecture proposed in this paper are designed and simulated by HSPICE using a 0.25μm CMOS process. The parameters of R_t and C_{total} in the load model are 10kΩ and 20pF, respectively. The simulation results for 3 kinds of driving architectures in the worst load situation are shown in Table 1.

Table 1　Simulation results for 3 kinds of driving architecture

Simulation condition worst load situation $T=27$℃			Simulation results					
			8 buffers		13 buffers		64 buffers	
R_s+R_t /kΩ	C_{total} /pF	R_g /Ω	T_s /μs	I_s /μA	T_s /μs	I_s /μA	T_s /μs	I_s /μA
10+5	20	135/4	13.4	764.2	9.4	922.1	6.6	2707
		135/3	16.3	629.1	11.3	787.6	6.6	2674
		135/2	22.1	494.1	15.0	653.1	6.5	2404
		135	30.0	359.0	26.0	518.6	6.6	2269

Note: $R_{\square}=135\Omega$, R_g is the unit resistance of R-string circuit, T_s is the settling time, and I_s is the quiescent current.

From the simulation results shown in Table 1, we can draw the following conclusions.

First, for a given driving architecture, the settling time and quiescent current consumption are affected by the value of unit resistance of the R-string circuit. With the decrease of the value of unit resistance, the settling time decreases but the quiescent current consumption is increases.

Second, for the given value of unit resistance, the settling time and quiescent current consumption are different for different driving architectures. With the increase of the number of driving buffers, the settling time decreases but the quiescent current consumption increases.

Third, for a two-stage driving architecture with 13 buffers, the settling time and power dissipation are the tradeoff of the values for the architecture with 8 buffers and 64 buffers. When $R_g=135\Omega$, we have $T_s=26\mu$s and $I_s=518.6\mu$A, T_s satisfies our design specifications, and the power dissipation can be reduced by 77% as compared with the conventional architecture with 64 buffers.

The two-stage driving architecture proposed in this paper has already been successfully applied in a 132RGB×176-dot, 260k color one-chip driver IC (named as "Longtium-T1") developed by us for the TFT-LCD of mobile phone.

The measured waveform of the source driver output voltage of the driver IC using 13 driving buffers and $R_g=135\Omega$ is shown in Fig. 8. The settling time of the grayscale voltage from 0.8 to 5.0V is about 19.2μs, which satisfies the design requirement. It can be seen that the measured settling time is less than the simulated one ($T_s=26\mu$s) shown in Table 1. This is because the loading parameters of the TFT-LCD panel such as R_t and C_{total} used in the simulation are larger than the real parameters.

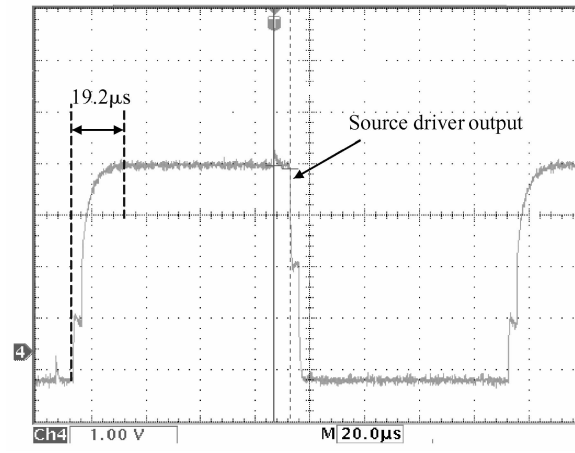

Fig. 8　Measured waveform of source driver output

The test results of the LCM using this driver IC ("Longtium-T1") are shown in Fig. 9. It is shown that high quality display images are achieved, in which the two-stage driving circuit proposed is used.

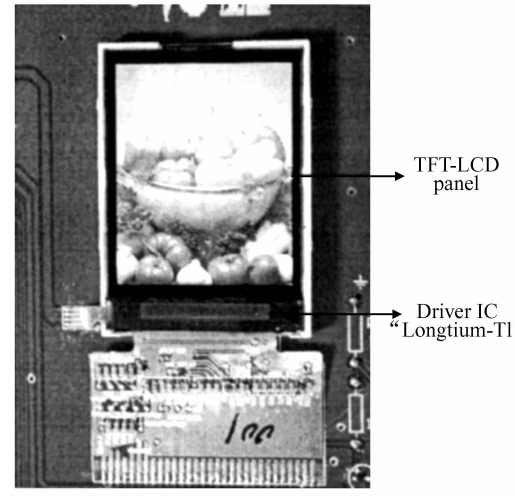

Fig. 9　Photo of LCM using longtium-T1 driver IC

6　Conclusions

A two-stage driving buffer architecture of a one-chip TFT-LCD driver IC for portable elec-

tronic devices has been proposed. For this new architecture, the power dissipation and the die area of the driver IC has been greatly reduced by reducing the number of driving buffers.

Optimization of the two-stage driving architecture can be carried out in order to drive different sizes of TFT-LCD panels and to reduce the power dissipation and the die area further, and even three-stage or multi-stage driving architectures can be considered.

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TFT-LCD 驱动芯片的二级驱动电路*

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摘要: 针对单芯片集成的 TFT-LCD 驱动芯片的特性, 提出了在 γ 校正电路中加入两级驱动 Buffer 的驱动电路结构, 以及提高其驱动能力的有效措施. 对于具有 13 个驱动 buffer 的二级驱动电路, 当由一个灰度电压驱动全部 396 个像素单元时, 驱动电压的最大安定时间约为 19.2μs; 静态消耗电流为 518μA, 与传统的 64 个驱动 buffer 电路相比, 其功耗减小了 77%. 本文的设计结果已成功应用于 132RGB×176 分辨率、26 万色彩色显示手机用 TFT-LCD 驱动芯片中, 其也可用于 PDA、数码相机等其他便携电子设备的显示驱动.

关键词: TFT-LCD; 驱动电路; γ 校正; 灰度电压

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