Current Share Control IC Design for Paralleled DC/DC Converters*

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Abstract: To keep even current distribution among DC/DC converters in a paralleled power system, an automatic master-slave control (AMSC) current sharing scheme is presented, which was implemented by a current share control IC. A current feedback loop for output voltage adjustment is proposed for low signal distortion. Moreover, a special startup control logic is designed to improve startup timing and to speed up the initial current sharing. It was completed in 1.5μm bipolar-CMOS-DMOS (BCD) technology with an area of 3.6mm^2. Using it, a paralleled power system of two DC/DC converters capable of outputting 12V/3A was built. Experimental results show that the current sharing error at full load is kept within 1%.

Key words: current sharing; IC; paralleled power system; automatic master-slave control
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1 Introduction

Paralleled DC/DC converters provide some outstanding advantages such as increased power rates and enhanced availability from the fault tolerance possible with $N+1$ converters. In such cases, output current sharing among the paralleled converters is desirable to distribute uniform stress and prevent one or more of them from operating in current limit mode[1~4]. Since DC/DC converters usually have good output voltage regulation, even modest differences in their output voltages can cause the output currents to be quite different. Thus, paralleled DC/DC converters require an explicit current sharing scheme to ensure proper operation.

Many schemes have been used to achieve current sharing, among which the automatic master-slave control (AMSC) has been the most frequently adopted one recently[1,3]. In an AMSC, the converter with the highest output current automatically becomes the master and the others are regulated to output currents almost the same as that of the master.

The AMSC current sharing scheme is described in this paper, along with the current feedback loop for converter output voltage adjustment. Through the control scheme, a system of paralleled DC/DC converters with proposed current sharing ICs is designed, and circuit details are described. Experimental results of a prototype design are provided to prove the functionality and performance.

2 Automatic master-slave control

The most popular current sharing schemes are the droop method and active current sharing schemes. The droop method relies on the high output impedance of each converter, with lower current deviation at higher output impedance. It is simple to implement. In addition, no communication between the converters is needed. However, it has a poor load regulation, making it unsuitable for high performance applications. By applying a closed loop negative feedback system, the active current sharing scheme provides better output voltage regulation and accuracy than the droop method. According to different approaches to generate the average output current information, it can be categorized into three modes: dedicated master-slave scheme, democratic scheme, and AMSC. In the dedicated master-slave scheme, a con-

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verter is designed as master and its output current provides the average output current information. In the democratic scheme, the average output current information is determined by "voting". And in AMSC, the master is dynamically determined: the converter with the highest output current automatically becomes the master, and its current acts as the average output current. While the dedicated master-slave scheme and democratic scheme provide perfect balance for currents during normal operation, they fail to provide fault tolerance. When the master converter in a dedicated master-slave scheme or one converter in a democratic scheme fails, the system will not work properly. Compared with these two schemes, AMSC is more flexible and helpful for improving system redundancy.

Figure 1 shows a diagram of the AMSC current sharing scheme for converters in parallel, with only the first and Nth converters shown. R_o is the output resistance of the converter. Each converter provides a measurement of its output current, I_o, and the diode-connect structure allows only one converter to communicate on the current share bus. It is the one with the highest output current, and is referred to as the master converter. In the slave converter, the output current is compared to that of the master converter to get a current-error signal, I_{adj}. The current-error signal flows through an adjust resistor, R_{adj}, to change the feedback voltage at the input node of the voltage loop of the converter, V_f, which drives the output current approximately to that of the master.

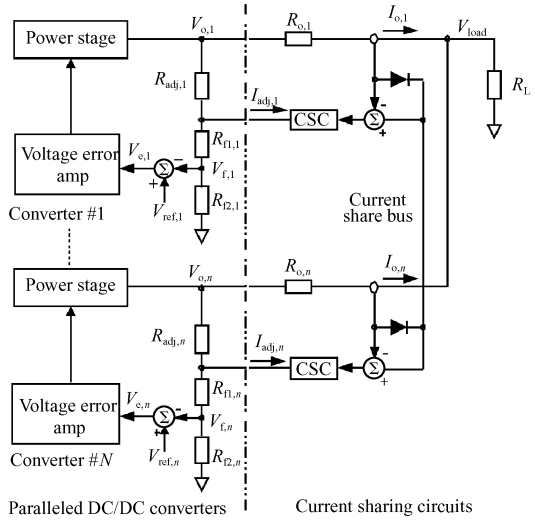

Fig. 1 Diagram of the automatic master-slave control

As described, the current feedback loop uses a current signal to communicate between the converters and the current sharing circuits. Compared with the traditional voltage-error signal feedback scheme, it reduces the signal distortion produced by parasitic parameters like wire resistors of PCB while a voltage signal passes through them.

At the steady state, supposing ideal current sharing has been achieved, the output current of an individual converter could be expressed as

$$I_{o,j} = \frac{V_{ref,i}(R_{f1,i} + R_{f2,i} + R_{adj,i})}{R_{f2,i}(R_{o,i} + nR_L)}, \quad j = 1 \sim n \tag{1}$$

Here n is the number of the paralleled converters, i represents the number of the master one, R_{f1} and R_{f2} are the feedback resisters of the voltage loop of the converter, and R_L is the load. Note that the shared output current is dependent on the load, the number of converters paralleled, and the parameters of the master converter.

The adjust currents of the converters required for current sharing are

$$I_{adj,j} = \frac{R_{f2,j}(R_{o,j} + nR_L)I_{o,j} - V_{ref,j}(R_{f1,j} + R_{f2,j})}{R_{adj,j}R_{f2,j}} - \frac{V_{ref,j}}{R_{f2,j}}, \quad j = 1 \sim n \tag{2}$$

It can be seen that for a given parallel power system, the adjust current is generated for current sharing according to the load.

3 Paralleled DC/DC converters and current share control IC

3.1 Paralleled DC/DC converters

The remote sensing and output current sourcing only capability is necessary to DC/DC converters connected in parallel. Remote sensing enables the output voltage to be adjusted by the feedback signal, and an output stage capable of sourcing current only is necessary for ensuring that one converter does not pull current from the other one. In the parallel system design, it is implemented by an OR-ing diode with an ultra-low forward voltage drop. In addition, the OR-ing diodes improve the system reliability when one converter is short-circuited.

3.2 Current share control IC

To implement good current sharing of a par-

allel DC/DC converter system, a current share control IC based on the AMSC current sharing scheme is proposed. The diagram of a converter with a current sharing control IC is shown in Fig. 2. R_{sense} is the output current sensing resistor and R_L is the load. The circuit in the dashed line was integrated onto a chip and acts as a current sharing control IC.

The main blocks in the current sharing control IC include: a current sensor amplifier that measures the output current of the converter through a low-value current sensor resistor; a current sharing bus driver, which is configured as the diode-connect structure between the current sharing bus and the current sensor amplifier; a current sharing receiver that monitors the current sharing bus voltage; an error amplifier that produces an error signal according to the difference between the currents of the converters; a *V-I* converter that converts the error signal to an adjust current applied to the converter; and a startup control circuit for startup timing improvement.

The details of the IC are described in Ref. [5].

3.3 Control loop design

The current sharing control IC introduces additional complexity into the dynamic characteristics of the parallel power system and may give rise to instability unless a proper current share loop is constituted. System stability requires that unity gain crossover frequency of the current sharing circuit be well before the unity gain crossover frequency of the converter. This can be achieved by adding a zero to the error amplifier at least one decade before the crossover frequency of the converter[1].

The compensation is realized by connecting C_{EAO} and R_{EAO} in series at the EAO pin as shown in Fig. 2. The values of C_{EAO} and R_{EAO} are determined by

$$C_{EAO} = \frac{G_M}{2\pi f_{zero}} A_{CSA} A_V A_{ADJ} A_{PWR(fCO)} \quad (3)$$

$$R_{EAO} = \frac{1}{2\pi C_{EAO} f_{zero}} \quad (4)$$

where G_M is the transconductance of the error amplifier, f_{zero} is the zero added, A_{CSA} is the gain of the current sensor amplifier, A_V is the voltage gain and is equal to R_{sense}/R_L, A_{ADJ} is the gain associated with the V/I converter and is equal to $R_{adj}/500\Omega$, and $A_{PWR(fCO)}$ is the measured gain of the converter at the desired zero frequency.

Figure 3 shows the Bode plots for the converter, the open loop current share loop and the total combined loop gain. By proper design of the compensation network, a stable parallel system can be obtained.

4 Experimental results

The current share control IC was designed and fabricated in 1.5μm double-metal, single-poly

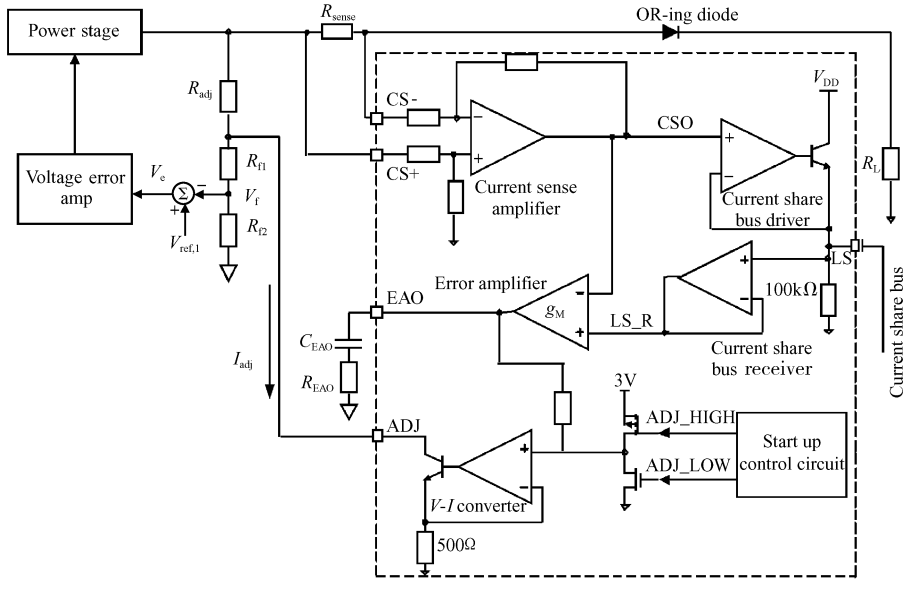

Fig. 2　Building blocks of the current sharing IC

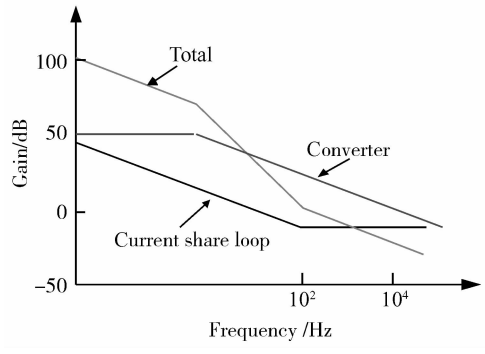

Fig. 3 Bode plots of the parallel power system

BCD technology. The chip area including test pads is 2047μm × 1776μm. Figure 4 shows a photo of the chip. By designing a demo board of a parallel power system, paralleled DC/DC converters, the functionality and performances of the IC were verified.

In the system, two LM25005 buck converters were paralleled with the current sharing control ICs. The converter supplied a 12V/1.5A output from the DC power source of 18V and operated at switching frequency of 300kHz. Each converter had a loop bandwidth of about 10kHz with a phase margin of 60°[6]. In the system, resistors of 50mΩ with high accuracy (±1%) were used as the output current sensing resistors.

4.1 Dynamic response

In the control loop design, the zero of the error amplifier was placed at 100Hz. The system stability was verified in the time domain. The dynamic response of the system to load steps between 50% and 100% is plotted in Fig. 5. CSO1 and CSO2 are the output signals of the current

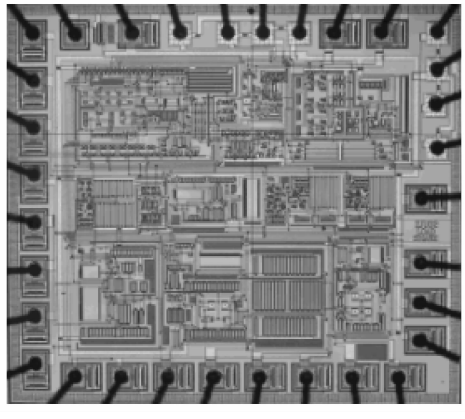

Fig. 4 Chip photo

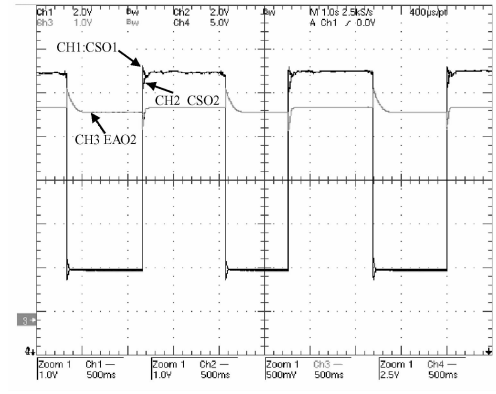

Fig. 5 System response to a load step from 50% to 100%

sensing amplifiers, which represent the output currents of the two converters, respectively. And EAO2 is the error signal of the error amplifier. It shows that the system settles to a new stable state quickly without oscillation, which implies the success of the control loop design. Meanwhile, the adjust current of the slave converter changes with load as was discussed in Section 2.

4.2 Startup timing

Figures 6 and 7 show the experimental results of the startup timing of parallel systems with and without startup control circuit, respectively. 80FLAG2 is the output flag signal of the startup comparator corresponding to the slave converter #2. When the output current of the slave converter is lower than 80% of that of the master one, 80FLAG2 is set to "1" and the *V-I* converter will be forced to sink a maximum current as high as

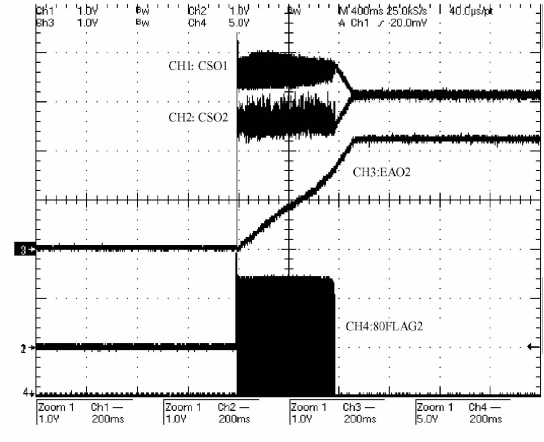

Fig. 6 Start-up timing of the parallel system with start-up control logic

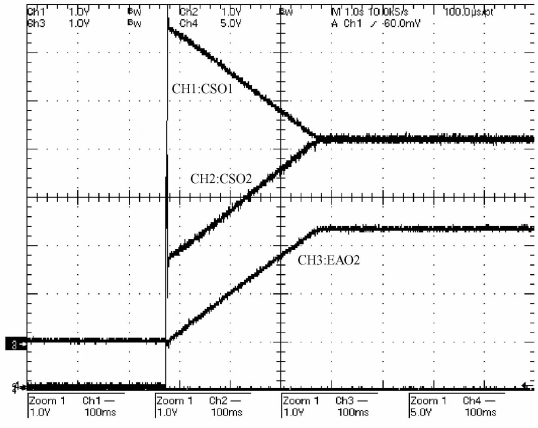

Fig. 7　Start-up timing of the parallel system without start-up control logic

6mA, which results in a fast adjustment. The results of Figs. 7 and 6 show that the startup control circuit held the output current of the slave converter at around 80% of that of the master one till the error signal at the EAO2 rose to a high level to start current sharing.

When the error signal at the EAO2 pin reaches a high enough level, the output voltage will be quickly adjusted to the expected value, and the startup procedure will be finished and then the system will enter into and maintain its normal operation status. Figure 6 shows that at 480ms the two converters completed adjustment finally and achieved the current sharing.

Note that here the value of 80% is a good tradeoff between system stability and current sharing errors during startup. The smaller the value, the larger the current difference between the converters, which results in bad startup timing improving. On the other hand, if it is too large, the system is more likely to switch between two modes, open loop control and closed loop control, repeatedly during ultra low load operation, which results in system instability. The value of 80% is proved to be an optimum value.

As analyzed above, the startup control circuit speeded up the current sharing during its starting up and improved its startup timing.

4.3　Load current sharing error

The load current sharing error is defined as

$$\eta_i = \left(\frac{2I_i}{I_L} - 1\right) \times 100\%, \quad i = 1,2 \qquad (5)$$

where I_1, I_2, and I_L are the currents of converters

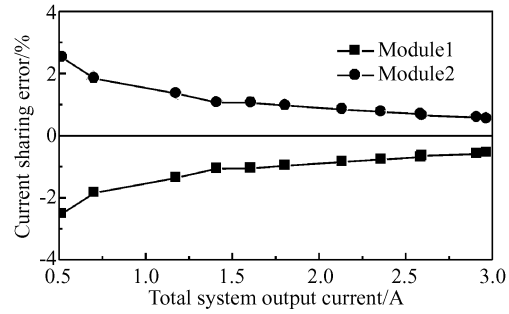

Fig. 8　Relationship between load current sharing error and output current

#1, #2, and the load, respectively. Figure 8 gives the curves of load current sharing error versus load current, and shows that the minimum value of 0.5% was reached at full load. It should be pointed out that at light load, besides small signal measurement error, inner offset voltages of the current sensing amplifier and the error amplifier as well as the *V-I* converter are summed into current distribution error, which results in a larger sharing error than at full load. However, since in this case, the current and thermal stresses of the converters are much less than at heavy load, the results are acceptable.

5　Conclusion

Using a current sharing control IC designed by the authors, a parallel power system with 12V/3A output capability was built based on the AMSC scheme. Experiments show that current sharing accuracy within 1% at full load was achieved. In addition, a startup control circuit was introduced to improve the system startup timing and speed up the start current sharing.

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应用于并行直流转换电源的均流控制芯片设计*

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摘要: 为实现并行直流转换电源系统中转换器电流的均衡分布,降低转换器承受的电、热应力,提高系统可靠性,给出一种采用自动主从控制策略的均流方案,并给出了方案实现的关键部件——均流控制芯片的设计.设计中采用电流反馈环路对输出电压进行调整,降低了 PCB 板级寄生效应对调整信号的影响;并提出一种启动控制电路用以改善系统的启动时序,加速了启动阶段的电流均衡过程.芯片采用 1.5μm BCD(Bipolar-CMOS-DMOS)工艺设计实现,面积为 3.6mm^2.应用该芯片构成了一个由两个直流转换器组成,具有 12V/3A 输出能力的并行电源系统.测试结果表明,该并行电源系统满负载时均流误差小于 1%.

关键词: 电流均分; 集成电路; 并行电源系统; 自动主从控制
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