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Effect of Snapback Stress on Gate Oxide Integrity of nMOSFET in 90nm Technology*

Zhu Zhiwei†, Hao Yue, and Ma Xiaohua

(*Key Laboratory of the Ministry of Education for Wide-Band Gap Semiconductor Materials and Devices, Microelectronics School, Xidian University, Xi'an* 710071, *China*)

Abstract: By measurement, we investigate the characteristics and location of gate oxide damage induced by snapback stress. The damage incurred during stress causes device degradation that follows an approximate power law with stress time. Oxide traps generated by stress will cause the increase of stress-induced leakage current and the decrease of Q_{bd} (charge to breakdown), and it may also cause the degradation of off-state drain leakage current. Stress-induced gate oxide damage is located not only in the drain side but also in the source side. The tertiary electrons generated by hot holes move toward Si-SiO_2 interface under the electrical field toward the substrate, which explains the source side gate oxide damage.

Key words: snapback breakdown; tertiary electron; SILC; charge to breakdown; oxide trap
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1 Introduction

Many I/O circuits are subjected to high current stress only on the drain terminal during electrostatic discharge (ESD) or electrical overstress (EOS) events. This may cause gate oxide reliability problems, especially for single gate oxide devices (same gate oxide for core and IO device). It has been suggested that hot holes can be injected into the oxide for a grounded gate MOSFET biased into snapback. Hole injection will have a great effect on gate oxide reliability when a large snapback current flows through the oxide of the deep-submicron nMOSFETs. Chen *et al*.[1] reported that gate oxide breakdown was accelerated when hot holes were injected into the oxide. Nishioka *et al*.[2] also observed gate oxide breakdown in small n-channel MOSFETs during drain-current-induced hot-hole injection. Krakauer *et al*.[3] found that snapback stress can result in both hole trapping and significant interface state leading, respectively, to a net negative or net positive threshold voltage shift.

With the improvement of the process technology of VLSI, the size and gate oxide thickness of MOSFETs are decreasing continually. Under the same bias conditions, the thinner the gate oxide of the MOSFET is, the higher the oxide electrical field becomes. I/O MOS devices become more and more sensitive to EOS/ESD from the outside world. CMOS device scaling is opening some new questions about the impact of EOS/ESD events on ultra-thin gate oxide integrity of MOS devices[2,3]. So far, few works have been devoted to the effect of non-destructive snapback stress on gate oxide integrity of the ultra-thin gate oxide MOSFET. In this paper, we analyze the generation of the defects and their impact on characteristics of 90nm nMOSFETs during DC snapback stress, and then the position of the generated defects is identified by S parameter measurement. Finally, it is explained that the generated defects extend from the drain to the source of the MOSFET by the theory of the tertiary hot electrons.

2 Devices and experiment

The device used in this paper is silicided LDD nMOSFET fabricated in 90nm CMOS technology. The oxide is about 1.4nm, formed with a decoupled plasma nitridation (DPN) process. The LDD

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† Corresponding author. Email: zwzhu@xidian.edu.cn
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nMOSFET is a surface device with an n+ poly-Si gate. By measurement, we can see that the first breakdown current of these devices is about 119μA, and the second breakdown current is about 110mA. To analyze the degradation of a non-destructive snapback stressed nMOSFET, these samples are stressed and biased into snapback. The snapback stress condition is as follows: $V_s = V_{sub} = V_g = 0$, where the drain is given I_d stress. When the stress increases gradually, the following events occur in sequence (Fig. 1):

(1) When the n+ drain to the p substrate bias reaches about 4.3V (trigger voltage V_{t1}), the n+ drain to the p substrate junction breaks down.

(2) When the drain current reaches 119μA (I_{t1}), the source to p substrate junction turns on.

(3) As the current increases further, the parasitic lateral npn transistor turns on, and the nMOSFET is pulled into snapback condition. Once the npn transistor turns on, the drain voltage will decrease from its maximum value (V_{t1}) to a minimum value (hold voltage V_h).

(4) If the current increases excessively, the self-heating effects will cause thermal (second) breakdown. The breakdown current is about 110mA.

The snapback *I-V* characteristic is shown in Fig. 1. The snapback stress (119μA $< I_d <$ 110mA) cannot generate destructive damage to the device, but can cause the device characteristics to degrade. In this paper, the stress is paused periodically during the DC snapback stress, and then the characteristics of the transistor are measured at that time. All the measurements are carried out under light-tight and electrically-shielded conditions at room temperature using a HP4156B precision semiconductor parameter analyzer.

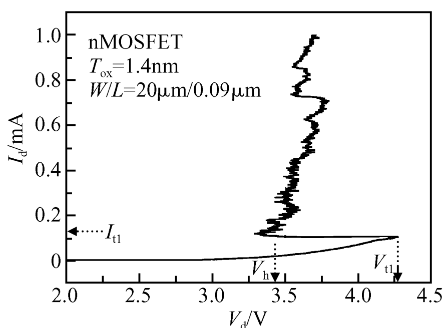

Fig. 1 nMOSFET DC snapback *I-V* characteristics The I_d is measured at $V_g = V_s = V_b = 0$.

3 Results and discussion

It is widely accepted that hot holes generated by the drain avalanche effect can be injected into the oxide near the drain of a grounded gate MOSFET biased into snapback[2,4]. The oxide traps (N_{ot}) and interface states (N_{it}) can be created by the injected holes in this process. In Fig. 2, the degradation of I_{dsat} is plotted versus the snapback stress time for an nMOSFET under different oxide thicknesses. As shown in Fig. 2, the thinner the oxide is, the more degradation of I_{dsat} it has. This is because thinner-oxide MOSFETs have a greater oxide electrical field in the gate oxide and the electrical field in the overlap of the gate and the drain during the same stress[5], so more oxide traps and interface states will be generated during the stress. From the figure we can see that the degradation approximately follows a power law versus snapback stress time, which is similar to the HCI degradation of a MOSFET. The power law expressions are depicted in Fig. 2. The two expressions have the same power exponent and different coefficients. The thinner the oxide is, the bigger coefficient the expression has. A bigger coefficient means more degradation.

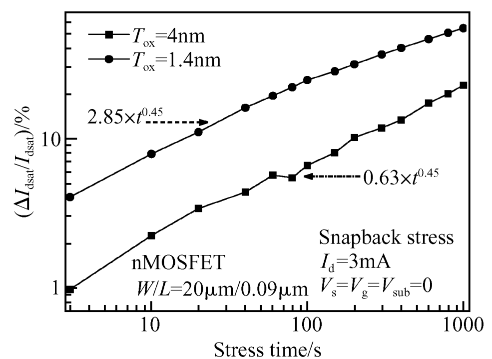

Fig. 2 Degradation of drain saturation current I_{dsat} under snapback stress I_{dsat} is measured at $V_d = V_g = 1$V.

In order to understand the physical mechanism of the oxide degradation under snapback stress, the generation of N_{it} and N_{ot} during snapback stress and their effect on the oxide integrity need to be identified. For this purpose, voltage ramp dielectric breakdown (VRDB) tests were performed on fresh and snapback-stressed nMOS-

FETs. In Fig. 3, the Q_{bd} is shown for an nMOSFET versus different I_{dsat} degradation ($\Delta I_{dsat}/I_{dsat0}$) after snapback stress. It shows no obvious change of Q_{bd} in low I_{dsat} degradation, but rapid decrease of Q_{bd} after large I_{dsat} degradation (about 36% $\Delta I_{dsat}/I_{dsat0}$). It also shows that the SILC degradation ($\Delta I_g/I_{g0}$) versus the I_{dsat} degradation has the inverse trend with the Q_{bd}. A two stage change process of normalized SILC ($\Delta I_g/I_{g0}$) with $\Delta I_{dsat}/I_{dsat0}$ is shown in Fig. 3. The $\Delta I_g/I_{g0}$ rapidly increases as the Q_{bd} rapidly decreases.

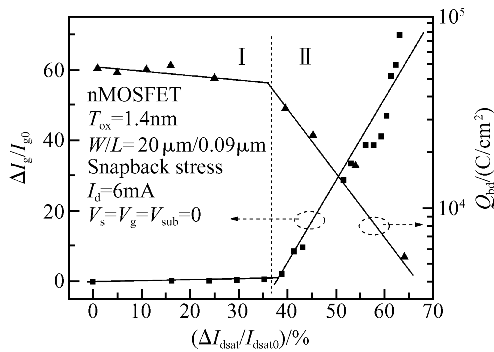

Fig. 3 Normalized SILC ($\Delta I_g/I_{g0}$) and charge to breakdown (Q_{bd}) versus I_{dsat} degradation during the snapback stress SILC is measured at $V_g = 1V$, $V_d = V_s = V_{sub} = 0$; Q_{bd} at $V_d = V_s = V_{sub} = 0$, ramp V_g from 0 to $-8V$.

It is known that oxide neutral electron traps are created in ultra-thin oxide layers during high field stress[1,2,4]. SILC can be explained by electrons tunneling via the generated neutral electron traps in Fig. 4, which is a two step tunneling process of electrons via oxide traps: Firstly, electrons will tunnel into the traps inside the oxide, and then electrons will tunnel out of the traps to either the conduction band of the oxide or to the

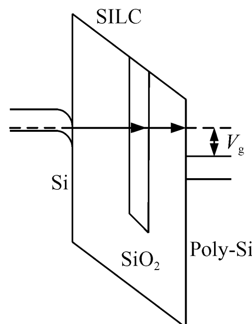

Fig. 4 Energy band diagram of the MOSFET with the trap assisted tunneling process for the SILC

anode directly. The SILC is the total of the trap-assisted tunnel current of all the oxide traps[6,7]. Up to now, many groups have proposed that SILC is directly linked to the oxide trap density of a MOSFET. Buchanan *et al*.[8] also proposed that SILC normalized to the initial leakage current before stress is proportional to the oxide trap density. The relationship of SILC varied with the traps generated by the snapback stress can be expressed as[6]:

$$\frac{I_{SILC}}{I_g(0)} = \frac{I_g(t) - I_g(0)}{I_g(0)} \approx A \times \Delta N_{ot} \quad (1)$$

where I_{SILC} is the SILC through the gate oxide, $I_g(t)$ is the gate leakage current after snapback stress, and $I_g(0)$ is the initial, unstressed gate leakage current. A is a constant, which has an experiential value[6] of $8 \times 10^{-9} cm^2$. ΔN_{ot} is the increase in oxide trap density. In the first stage of the SILC varied with $\Delta I_{dsat}/I_{dsat0}$, the SILC has little change, which means that the increase of gate oxide traps generated by snapback stress is not significant in this stage according to Eq. (1), so the degradation from N_{it} is dominant. The increase of N_{it} causes the degradation of I_{dsat} (Fig. 2) in the initial stage of snapback stress. In the second stage, SILC rapidly increases with $\Delta I_{dsat}/I_{dsat0}$, which shows that lots of oxide traps N_{ot} are generated by snapback stress. It is also observed that the transition point of the first stage to second stage for the $\Delta I_g/I_{g0}$ corresponds to the point in which the Q_{bd} begin to rapidly decrease, which shows that the increase of N_{ot} begins to become a significant factor for the degradation of gate oxide of a snapback-stressed nMOSFET in the second stage. From the above discussion, it can be determined that the oxide traps generated by snapback stress may degrade gate oxide breakdown characteristics significantly, but the interface states N_{it} do not.

The oxide traps generated by snapback stress may also significantly impact the off-state drain leakage current I_d. The off-state mode current measurement result is shown in Fig. 5. In the initial stage of snapback stress, drain leakage current I_d is approximately equivalent to source current I_s (The I_s is the sub-threshold current of the nMOSFET, $I_s \gg I_g$). The I_s decreases with stress time because the oxide trapping electrons and the interface states increase the surface potential in the channel. With the increase of stress time, the gate

current I_g gradually increases because many oxide traps are generated by the snapback stress. Finally, I_g would exceed I_s and become the dominant component of I_d. This implies that the off-state drain leakage current is mainly caused by gate current I_g after a long stress time. However, previous study shows that the degradation of off-state drain leakage current is mainly induced by interface-states assisted tunneling and oxide-traps-induced surface barrier lowering[5] for the thick gate oxide MOSFET, which is different from the characteristics of MOSFETs in 90nm technology.

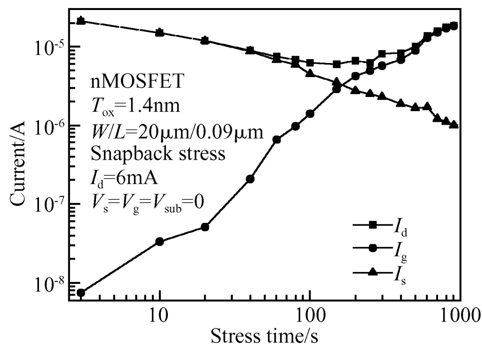

Fig.5 Off-state mode drain current I_d, gate current I_g, and source current I_s during snapback stress They are measured at $V_d = 1V$, $V_s = V_g = V_{sub} = 0$.

For the purpose of evaluating the damage location, it is necessary to take accumulation mode of the carrier-separation measurement[9~11] after snapback stress. Degraeve *et al*.[9] proposed that non-uniform oxide degradation along the channel length of the MOSFET can be revealed via a comparison of the drain and source currents biased in the accumulation region, which are composed of electrons that tunnel from the gate ($V_g<0$). The position of damage along the channel can be evaluated by the parameter

$$S = \frac{I_d}{I_d + I_s} \tag{2}$$

where I_d and I_s are the drain and the source currents of the MOSFET biased in the accumulation region after the snapback stress. These currents mainly consist of two components: one due to the tunneling current through the unbroken oxide region, and the other due to the current through the damage region. The mechanism of the tunneling current through the unbroken oxide region coincides with the current measured before the damage occurred. The parameter S provides an indication of the location of the most severe oxide damage along the channel where a substantial increase in tunneling leakage is expected to occur. If S comes close to 1, the most severe oxide damage is on the verge of the drain. If S comes close to 0, the most severe oxide damage is on the verge of the source. For other values of S, the most severe oxide damage is located in channel region.

Figure 6 shows the distribution of the ratio S taken at negative gate voltage $V_g = -1V$ before and after snapback stress ($I_d = 6mA$). Fresh devices exhibit identical I_d and I_s, and a tight S distribution centered around 0.5, indicating a uniform tunneling gate leakage along the channel. After stress, the value of parameter S is distributed over the whole region of 0 to 1. The inset depicts the cumulative distribution of the S parameter for the same device population after stress.

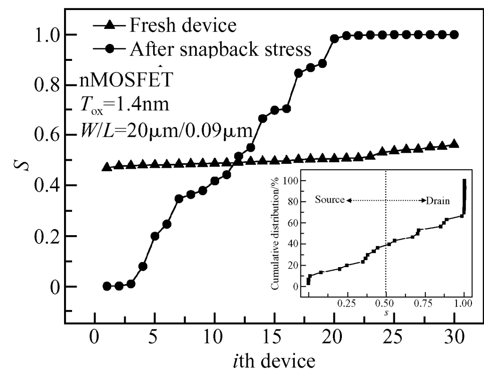

Fig.6 Damage location parameter S of a large number of nMOSFET before and after 1000s snapback stress Parameter S is measured at $V_g = -1V$, $V_d = V_s = V_{sub} = 0$.

The left side of the dashed line denotes that the most severe oxide damage is located at the source side of the device, and the right side of the dashed line denotes that the most severe oxide damage is located at the drain side of the device. Salman *et al*.[12] proposed that the injection of the hot holes is localized at the drain side under drain stress, which can result in drain side gate oxide damage to the MOSFET. Figure 6 also shows that a significant percentage (about 60% in the inset) of the population exhibits higher drain side than source side oxide leakage. In these devices, this substantial drain side oxide damage was observed to lead to drain side oxide breakdown[13]. However, it is necessary to see that the 40% of the population of the samples (inset of Fig.6) that exhibited higher

source side damage is comparable to the population of the samples exhibiting higher drain side oxide damage after snapback stress, which is different from the previous study[4,12]. This indicates that the source side gate oxide damage is becoming a new reliability problem for the nMOSFET in 90nm technology, whose physical mechanism may be explained by Fig. 7.

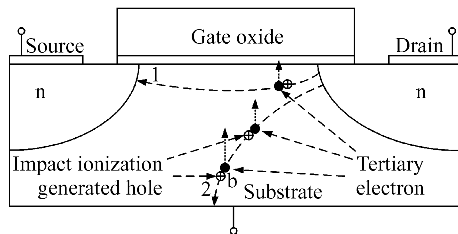

Fig. 7 Cross section of an nMOSFET

The schematic cross section of an nMOSFET biased to snapback is shown in Fig. 7. Under the snapback condition, the electron-hole pairs are generated by the avalanche effect near the junction of the drain and substrate, and then whole electrons are collected by the drain electrode and most holes are collected by the substrate electrode. The substrate potential is necessary to keep the parasitical bipolar transistor turned on due to the substrate resistance when the hole current flows through the substrate region under the snapback condition. As a result, an electrical field is set up direct from the Si-SiO_2 surface to the substrate. For the short channel nMOSFET, some holes may also arrive at the source diffusion region under the snapback condition. Thus there are two general trajectories of hot holes in Fig. 7, viz. 1 and 2. The previous study[14,15] proposed that the heating of the hot holes can result in the generation of energetic tertiary electrons when the avalanche-effect-generated holes move away from the drain under the large drain bias, which is ascribed to the impact ionization feedback mechanism represented in Fig. 7. These tertiary hot electrons can be injected into the oxide and cause gate oxide damage. During the snapback stress, generated tertiary hot electrons (filled circles) would inject gate oxide under the electrical field toward the substrate when the hot holes move from the drain to the substrate or the source. The injection of tertiary hot electrons toward the oxide may induce oxide damage. Moreover, as these hot holes traverse deeper into the substrate [e. g. location (b)] and further from the drain, the resultant tertiary electrons that are injected into the gate oxide from this location tend to be "hotter". First, the initial energy of these deeper tertiary electrons and further tertiary electrons away from the drain are likely to be higher since the holes tend to become more energetic at greater depth and further distance away from drain. Second, deeper tertiary electrons will tend to gain more energy in their motion due to a longer distance traveled across the bulk region. On the verge of the drain, the damage is mainly owing to the drain avalanche hot carrier injection. In the channel region and the region near the source, the damage is due to the injection of the tertiary electrons toward the oxide. Because the tertiary electrons can be generated on the whole motion trajectory of the hot holes, the injection of the tertiary electrons may cause the location of the oxide traps to extend from the drain to the source of the nMOSFET. Finally, the oxide damage location is not only in the drain side, but also in the source side. This may explain why the S parameter is distributed over the whole region of 0 to 1.

4 Conclusion

This paper reports the investigation of snapback-stress-induced gate oxide damage and damage location in the oxide of nMOSFETs. The snapback stress is non-destructive, which causes the device degradation with stress time, which is similar to the HCI degradation of nMOSFET. The measurement shows that the increase of oxide traps is the main reason for the degradation of the gate oxide integrity of the 90nm nMOSFET, and the oxide damage location is distributed over the whole the gate oxide along the channel.

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Snapback应力对90nm nMOSFET栅氧化层完整性的影响*

朱志炜† 郝 跃 马晓华

（西安电子科技大学微电子学院 宽禁带半导体材料与器件教育部重点实验室，西安 710071）

摘要： 基于测试对snapback应力引起的栅氧化层损伤特性和损伤位置进行了研究.研究发现应力期间产生的损伤引起器件特性随应力时间以近似幂指数的关系退化.应力产生的氧化层陷阱将会引起应力引起的泄漏电流增加,击穿电荷减少,也会造成关态漏泄漏电流的退化.栅氧化层损伤不仅在漏区一侧产生,而且也会在源区一侧产生.热空穴产生的三代电子在指向衬底的电场作用下向 $Si\text{-}SiO_2$ 界面移动,这解释了源区一侧栅氧化层损伤的产生原因.

关键词： 突发击穿；三代电子；应力引起的泄漏电流；击穿电荷；氧化层陷阱

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† 通信作者.Email:zwzhu@xidian.edu.cn

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