Key Techniques of Frequency Synthesizer for WLAN Receivers

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Abstract: Several key techniques for a PLL-type frequency synthesizer for WLAN receivers are studied. Its structure is analyzed and the main parameters are proposed. A monolithic LC-tuned voltage controlled oscillator (LC-VCO) with low phase noise is fabricated with TSMC 0.18μm RF (radio frequency) CMOS technology. The measured phase noise is -117dBc/Hz at 4MHz off the center frequency of 4.189GHz. A down-scaling circuit with low power dissipation was fabricated in a TSMC 0.18μm mixed-signal CMOS process. The measured results show that the IC can work well under a 1.8V power supply. Its total power dissipation is only 13mW.

Key words: PLL; WLAN; VCO; down scaling
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1 Introduction

The growing popularity of portable wireless devices has resulted in a high demand for high data-rate wireless LAN (WLAN) systems. The PLL-type frequency synthesizer is shared between the transmitter and the receiver and is one of the most important parts in WLAN transceiver systems.

This paper focuses on key techniques in the design of the PLL frequency synthesizer in a WLAN transceiver system. A linear model of the PLL frequency synthesizer is proposed, and the main parameters of the PLL are acquired through behavior simulation based on the model. A VCO based on an on-chip symmetrical spiral inductor is fabricated in TSMC 0.18μm RF CMOS technology. A down-scaling circuit with a programmable swallow divider directly synthesized by means of Verilog-HDL is fabricated in a TSMC 0.18μm mixed-signal CMOS process. Measurement shows that the phase noise of the VCO and the power dissipation of the down-scaling circuit are very low. These ICs work very well. All of these techniques prove very important for the design of WLAN receivers.

2 PLL for frequency synthesizer

According to the WLAN standard of IEEE 802.11a[1], three bands are defined: 5.15 $\sim$ 5.25GHz, 5.25$\sim$5.35GHz, and 5.75$\sim$5.85GHz. The operation frequency of the proposed transceiver in this paper covers the first two bands, i.e. 5.15$\sim$5.35GHz.

A dual-conversion transceiver is adopted. The RF signal is mixed with the first local oscillator (f_{LO1}) at 4GHz and thus is converted from 5 to 1GHz. Then, the 1GHz RF signal is mixed with the second local oscillator (f_{LO2}) as in a Zero IF transceiver. Figure 1 shows a block diagram of the frequency synthesizer, which is made up of a phase frequency detector (PFD), a charge pump (CP), a low pass filter (LPF), a VCO, and a down-scaling circuit. The frequency band at 4GHz

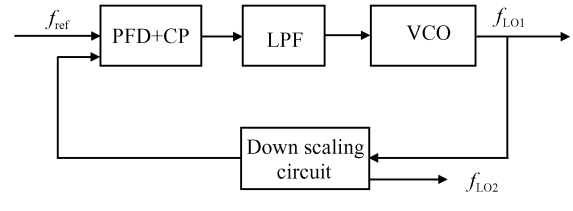

Fig. 1 Block diagram of the PLL-type frequency synthesizer

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is generated by the VCO, and the frequency band at 1GHz is obtained by the frequency divider working at divided-by-4 in the down-scaling circuit.

3 Behavior simulation strategy

The proposed PLL-type frequency synthesizer can be modeled as a linear system[2~4]. As shown in Fig. 2, the VCO is modeled as an integrator with a gain of K_V. K_d is the gain of the PFD (about $1/2\pi$), the current of the charge pump is I_P, and the transfer function of the LPF is defined as $Z(s)$. The number of poles of the LPF plus the fundamental pole of the VCO defines the order of the PLL.

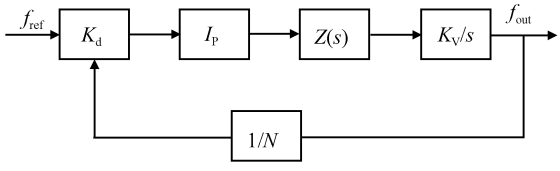

Fig. 2　Block diagram of the simplified PLL-type frequency synthesizer model

In order to reduce the chip area, the LPF of the PLL-type frequency synthesizer is realized by off-chip components. Figure 3 shows the circuit implementation of the LPF. This is a 3rd-order LPF. Along with the charge pump, a 4th-order PLL is also constructed.

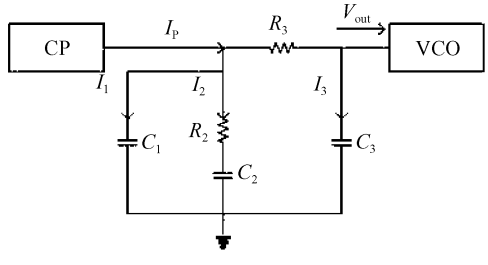

Fig. 3　Schematic of the LPF

The transfer function of the LPF is

$$Z(s) = \frac{(1 + s\tau_2)}{s[s^2 C_1\tau_2\tau_3 + s(C_1\tau_2 + C_1\tau_3 + C_3\tau_2 + C_2\tau_3) + C_1 + C_2 + C_3]} \quad (1)$$

where $\tau_2 = R_2 C_2$, $\tau_3 = R_3 C_3$. The loop transmission of the PLL (open loop transfer function) is

$$L(s) = \frac{I_P K_V (1 + s\tau_2)}{2\pi N s^2 [s^2 C_1\tau_2\tau_3 + s(C_1\tau_2 + C_1\tau_3 + C_3\tau_2 + C_2\tau_3) + C_1 + C_2 + C_3]} \quad (2)$$

The phase margin of the loop is

$$\mathrm{PM} \approx \tan^{-1}(\tau_2\omega_c) - \tan^{-1}\left(\frac{A\tau_2\omega_c}{1 - B(\tau_2\omega_c)^2}\right) \quad (3)$$

where ω_c is the loop bandwidth of the PLL, and

$$A = \frac{\frac{C_1}{C_2} + \frac{C_3}{C_2} + \frac{\tau_3}{\tau_2}\left(1 + \frac{C_1}{C_2}\right)}{1 + \frac{C_1}{C_2} + \frac{C_3}{C_2}}, B = \frac{\frac{C_1\tau_3}{C_2\tau_2}}{1 + \frac{C_1}{C_2} + \frac{C_3}{C_2}} \quad (4)$$

The closed loop transfer function of the PLL is

$$G(s) = \frac{NL(s)}{s + L(s)} \quad (5)$$

In order to keep the stability of the loop, the PM must be larger than 45°. The loop bandwidth of the PLL can increase to constrain the phase noise. However, the stability of the loop will decrease if the bandwidth is too large. A compromise must be made when the parameters of the components in the LPF and the other important parameters in the loop are considered. Some important loop parameters are listed in Table 1.

Table 1　Loop parameter of the frequency synthesizer

Parameter	Value	Parameter	Value
Reference clock	4MHz	C_1	277.5pF
Loop bandwidth	89kHz	C_2	8.065nF
Phase margin	54°	C_3	72.94pF
Current of CP	1mA	R_2	1.061kΩ
VCO gain	580MHz/V	R_3	5.708kΩ

A linear model as shown in Fig. 2 can be established with the help of ADS. With this model, the simulation of the loop response, the transient response, and the phase noise can be executed with less time, compared with the simulation at the transistor level. Figure 4 (a) shows the transient response of the VCO output frequency in closed loop state. It can be seen that the stability time of the PLL is about 27.3μs.

To simplify the simulation, the PFD, CP, and LPF are combined into one block and the noise data are taken from transistor-level simulation. The noise data of the VCO, the down-scaling circuit (frequency dividers), and the reference signal are obtained from measurement results. The phase noise of the PLL is shown in Fig. 4 (b). The total phase noise is −108.49 dBc at 1MHz off the carrier.

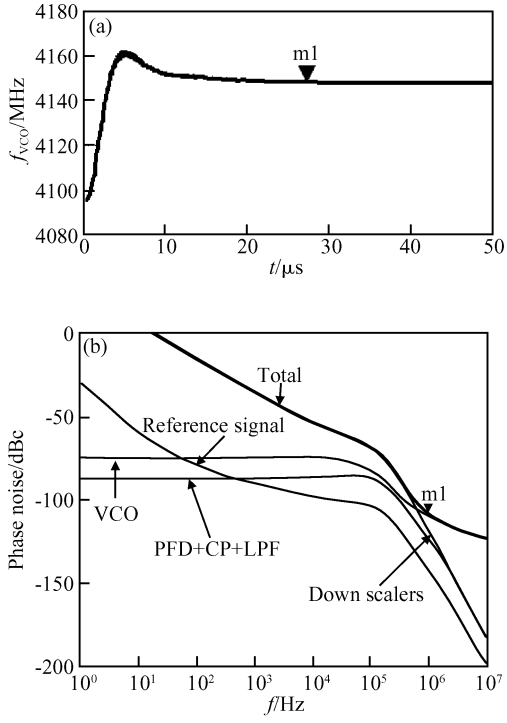

Fig. 4 (a) Simulation results of the transient response of the VCO frequency; (b) Simulation results of the phase noise of the PLL

4 VCO design

The VCO is the key component of the frequency synthesizer. Since $f_{VCO} = 4/5f_t$, the output signal of the VCO should cover the frequency band of 4.1～4.3GHz.

A schematic of the LC VCO[5] is shown in Fig. 5. It is a cross-coupled difference VCO with two cross-couple amplifiers in stack. Two tuning terminals are connected to two different control voltages. Four MIM (metal-insulator-metal) capacitors, two MOS (metal-oxide-semiconductor) varactors, and one on-chip spiral inductor make up the LC resonant tank. Two crossed-coupled amplifiers provide negative resistance to compensate the loss in the LC resonator. One is made of two nMOS, and the other is of two pMOS. The total negative resistance is the sum of the negative resistances of transistor pair M1/M2 and transistor pair M3/M4.

The phase noise is primarily dependent on the Q-factor of the inductor. The higher Q is, the lower the phase noise is. In order to get a high-Q inductor, an on-chip spiral[6] was designed by means of momentum, Agilent's electromagnetic

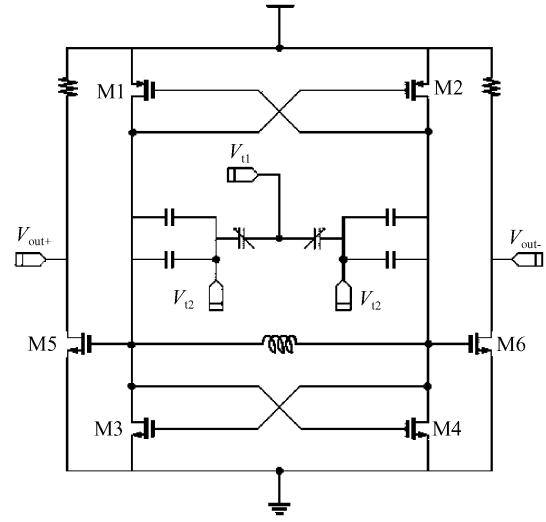

Fig. 5 Circuit schematic of the VCO

analysis program. Metal 6, i. e. the thickest top metal, was selected to form the spiral winding. Such an on-chip inductor has an inductance of 1.9nH and a Q-factor of $\geqslant$10 between 3.0 and 5.0GHz.

The VCO circuit was fabricated in a TSMC 0.18μm RF CMOS process. Figure 6 shows a microphotograph of the VCO.

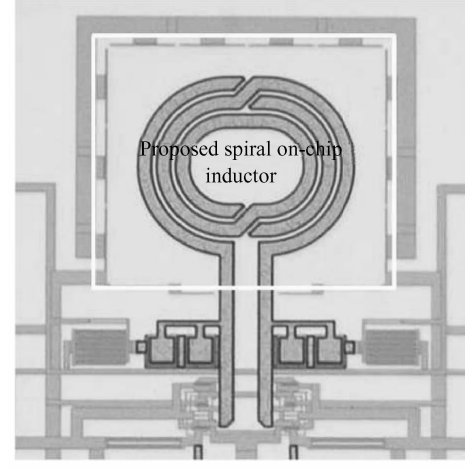

Fig. 6 Microphotograph of the VCO

Figure 7 shows the measured spectrum of the output signal at 4.18871GHz. From the figure it can be seen that the center frequency is 4.1887GHz, the output power is -8.68dBm, and the phase noise is -106dBc at 500kHz off the center frequency.

When the control voltage V_{t1} is fixed, the frequency tuning range can be measured by changing

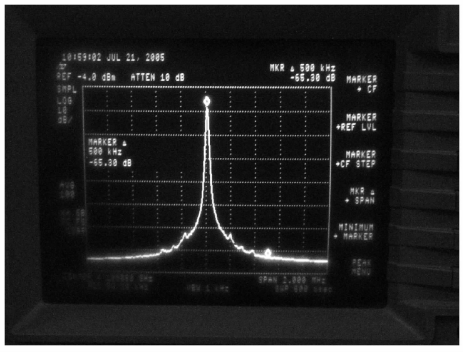

Fig. 7　Measured phase noise (SPAN 2MHz; VBW 1kHz; RBW 10kHz; Centre 4.189GHz; Frequency offset 500kHz)

the value of the control voltage V_{t2}. Different tuning ranges were obtained at different values of the control voltage V_{t1}, as listed in Table 2.

Under the control voltage V_{t2} = 0.8V, the measured tuning curve of the VCO is shown in Fig. 8. It is noticed that the frequency band of 4.1 ~ 4.3GHz is in the linear region of the curve and the slope of the linear region is not too large, which makes this circuit a good choice for integration into a frequency synthesizer in a WLAN transceiver.

The output jitter is shown in Fig. 9. It can be seen that jitter time is 4.423ps at the frequency of 4.22GHz.

Table 2　Tuning ranges of VCO at different values of control voltage V_{t1}

V_{t1}/V	0	0.2	0.4	0.6	0.8	1.0	1.2	1.4	1.6	1.8
f_{low}/GHz	4.1573	4.0801	4.0480	4.040	4.0354	4.0329	4.0329	4.0310	4.0327	4.0316
f_{high}/GHz	4.6392	4.6359	4.6242	4.6024	4.5504	4.5292	4.4767	4.3964	4.2803	4.1540

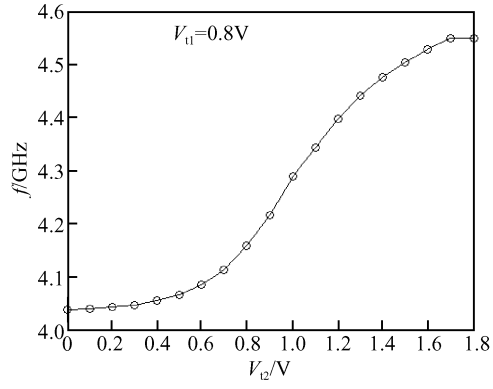

Fig. 8　Measured tuning characteristic of the VCO

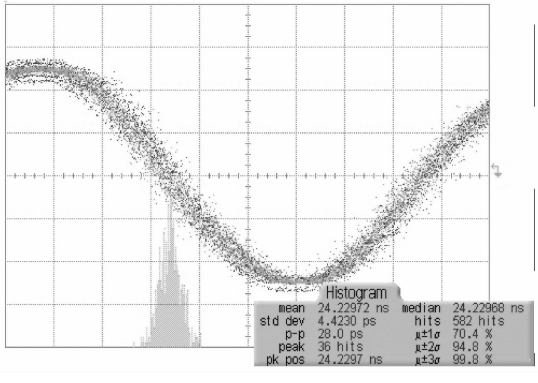

Fig. 9　Output jitter

5　Down-scaling circuit

In a PLL-type frequency synthesizer, the frequency of the VCO's output signal is divided by a down-scaling circuit into a lower one. In this PLL system, the down-scaling circuit consists of three parts: an asynchronous frequency divider working in the divide-by-4 mode, a dual modulus prescaler[7] (DMP), and a programmable & plus swallow divider made up of counter-M and counter-A. A block diagram of the down-scaling circuit is shown in Fig. 10. The DMP divides the output by $P+1$ until counter-A counts up to A. At this point it switches over and divides by P until counter-M counts up to M. Then the two counters are reset, and DMP switches back to divide-by-$(P+1)$ at the same time. The total division ratio of the down-scaling circuit is

$$N = 4(PM + A) \tag{6}$$

In the proposed frequency synthesizer, $P = 8$, $M = 32$, and A can be set between 0 and 16 in the programmable & plus swallow divider.

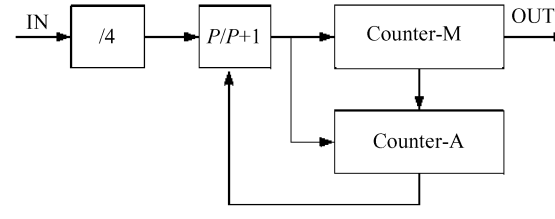

Fig. 10　Block diagram of down scaling circuit

The asynchronous frequency divider working in the mode of divided-by-4 is made up of two D-

flip-flops (DFF) as shown in Fig. 11

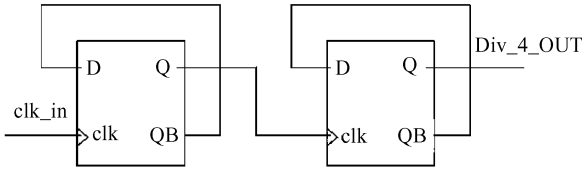

Fig. 11 Block diagram of asynchronous frequency divider working in the state of divided-by-4

The DMP, which consists of three parts, the divide-by-4/5 counter, the asynchronous counter, and the control logic, is shown in Fig. 12. When the control signal MC is at logic high (MC = 1), the division ratio of the divide-by-4/5 counter is 5 and the total division ratio of the DMP is 9. Otherwise, the division ratio of the divide-by-4/5 counter is 4, and the total division ratio of the DMP is 8.

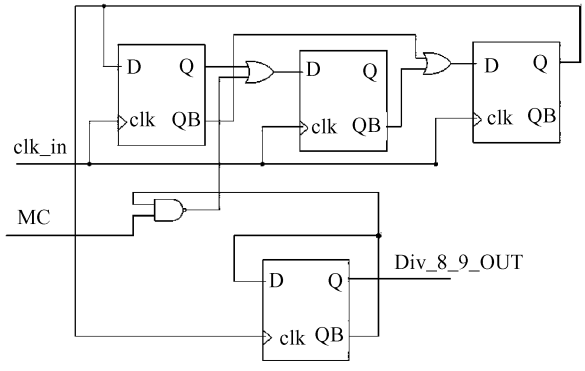

Fig. 12 Block diagram of the DMP

The master/slave D-flip-flop in the frequency divider working at the mode of divided-by-4 and DMP is made up of an improved D-latch as shown in Fig. 13. Complementary cross-couple pairs are used in the output part of the latch. The load of the output part is lowered in order to increase the speed. M5 (M6) is used to turn off the discharge path when Q (QB) changes from logic 0 to logic 1. Although the output logic 1 decreases from V_{DD} and a static current path exists if the input data changes in the evaluation phase (CLK = logic '1'), proper logic operation can be ensured by carefully selecting the dimensions of the transistors. Moreover, in high-speed applications, due to the continuous switching at high frequencies, the dynamic power dissipation dominates and the added static power dissipation is not significant. Thus the improved high-speed flip-flop is very attractive for RF applications, and the output voltage can directly drive the following block without any post amplifier. Thus, the complexity of the circuit is decreased.

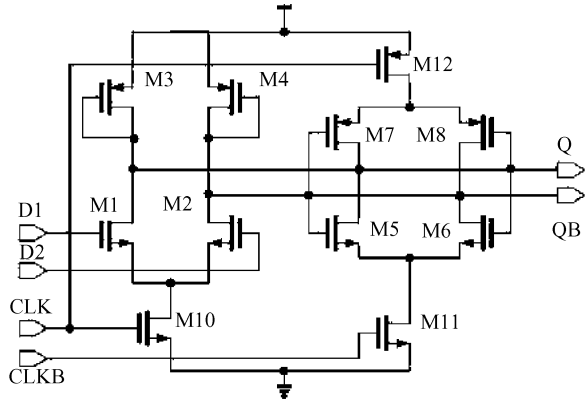

Fig. 13 Schematic diagram of the improved D-latch

The programmable & plus swallow divider was designed by means of Verilog-HDL and synthesized by Apollo, Synopsys' VLSI implementation program. It was finally fabricated with Artisan's TSMC 0.18μm CMOS standard library[8].

The down-scaling circuit was realized in a TSMC 0.18μm mixed-signal CMOS process. Figure 14 shows its microphotograph.

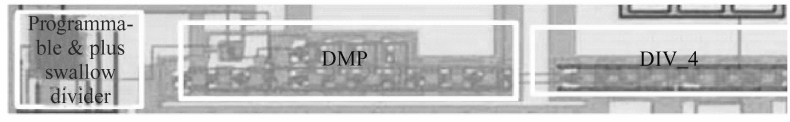

Fig. 14 Microphotograph of the down scaling circuit

The measured 133MHz output signal of the DMP is shown in Fig. 15 (a). The measured output signal of the programmable & plus swallow divider, compared with the output signal of the DMP, is shown in Fig. 15 (b). Its frequency is 4.078MHz. The amplitudes of both the DMP and

the programmable & plus swallow divider are 1V. The DC current of the down scaling circuit including an output buffer is only 7mA. The relationship between total division ration of the down scaling circuit and the frequency of output signal of the programmable & plus swallow divider is shown in Table 3.

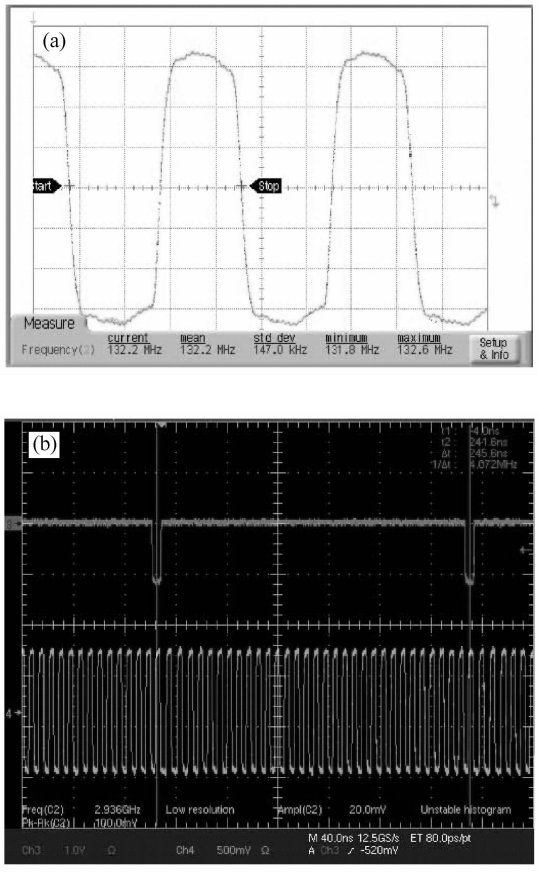

Fig. 15　(a) Output waveform of DMP; (b) Output waveform of the measured output signal of the programmable & plus swallow divider, compared with the output signal of the DMP

Table 3　Relationship between total division ratio of the down-scaling circuit and f_{out}, the frequency of output signal of the programmable & plus swallow divider, with f_{in} = 4.22GHz

A	A (in bit)	$PM + A$	f_{out}/MHz
3	011	259	4.078
4	100	260	4.062
5	101	261	4.047
6	110	262	4.032
7	111	263	4.016
8	1000	264	4.001
9	1001	265	3.987
10	1010	266	3.972

6　Conclusion

The key techniques of a frequency synthesizer for WLAN receivers were presented. The structure of the synthesizer was analyzed. Its main parameters are proposed through behavior simulation. A VCO with phase noise of −117dBc/Hz at 4MHz off the center frequency of 4.189GHz was realized in a TSMC 0.18μm RF CMOS process. The down-scaling circuit with a power dissipation of 13mW was fabricated in TSMC 0.18μm mixed-signal CMOS process. These ICs are good choices for realizing WLAN receivers.

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无线局域网接收机用频率综合器的关键技术

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摘要：对无线局域网接收机用锁相环型频率综合器的几项关键技术进行了研究.首先分析了锁相环型频率综合器的结构并提出了系统的主要参数.采用 TSMC 0.18μm 射频 CMOS 工艺设计了一个具有低相位噪声的单片 LC 调谐型压控振荡器.其在 4.189GHz 频点上 4MHz 频偏处所测得的相位噪声为 -117dBc/Hz.采用 TSMC 0.18μm 混合信号 CMOS 工艺实现了具有低功耗的下变频模块电路.该电路在 1.8V 电源供电下可正常工作,功耗为 13mW.

关键词：锁相环；无线局域网；压控振荡器；下变频模块
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中图分类号：TN432 **文献标识码**：A **文章编号**：0253-4177(2007)04-0542-07

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