2.5Gb/s/ch 0.18μm CMOS Data Recovery Circuit

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Abstract: A 2.5Gb/s/ch data recovery (DR) circuit is designed for an SFI-5 interface. To make the parallel data bit-synchronization and reduce the bit error rate (BER), a delay locked loop (DLL) is used to place the center of the data eye exactly at the rising edge of the data-sampling clock. A single channel DR circuit was fabricated in TSMC's standard 0.18μm CMOS process. The chip area is 0.46mm^2. With a $2^{31}-1$ pseudorandom bit sequence (PRBS) input, the RMS jitter of the recovered 2.5Gb/s data is 3.3ps. The sensitivity of the single channel DR is less than 20mV with 10^{-12} BER.

Key words: data recovery; delay locked loop; bit-synchronization
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1 Introduction

A 40Gb/s optical-link communication system requires electrical interface technology with bit rates of 2.488 ~ 3.125Gb/s/ch and 17 parallel channels between the SerDes device and the framer IC[1]. The manifestation of this technology is called SFI-5 (SerDes framer interface level 5)[1]. One of the technical challenges posed by SFI-5 is how to recover the 17-channel parallel data. Some approaches to developing a data recovery (DR) circuit have been proposed for such a multi-bit interface[2,3]. To reduce the bit error rate (BER), these circuits adjust the rising edge of the 2.5GHz clock to the data eye center by selecting a right clock-phase[2] or interpolating two quad-phase clocks[3].

For multi-channel data recovery applications, a problem exists for the conventional data recovery approaches. Corrupted by low-frequency wander and high-frequency jitter, the input parallel data of the multi-channel DR circuit may not be bit-synchronous. In the conventional way, each channel adjusts a local clock to its data eye center so that the recovered data are not bit-synchronous. This means that each channel should have its individual clock output so that an alignment circuit is needed in the following digital system. The alignment circuit would transfer all 17 data lanes, which have individual clocks to a common clock domain[2].

To synchronize the parallel recovered data so that the following alignment circuit is unnecessary, we design a 2.5Gb/s/ch DR circuit. In contrast to the conventional approaches, a voltage controlled delay line (VCDL) is used to adjust the data eye center to the rising edge of the 2.5GHz reference clock. For multi-channel data recovery application, the recovered data of each channel is synchronized with the global reference clock so that all the recovered data are bit-synchronous. Used in an SFI-5 interface, all the 17-channel recovered data share a global clock output so that the alignment circuit in the following digital system[2] can be avoided.

2 Circuit techniques

As shown in Fig. 1, the DR circuit consists of a delay-locked loop (DLL) and a D-flip-flop (DFF). To synchronize the input data with the reference clock, a VCDL is used in the DLL to adjust the data eye center to the rising edge of the reference clock. For parallel data recovery, the DR circuits of each channel share a common reference clock, so that the clock is called a global reference clock. The clock should be provided at the system level by some specific devices[2,3]. The DFF is used to regenerate the synchronized data.

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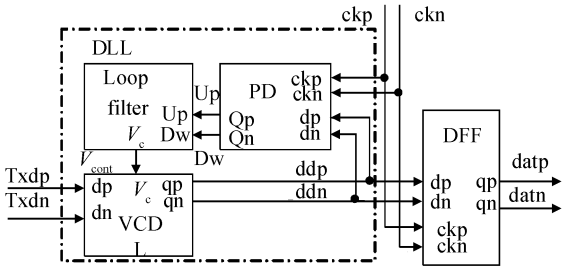


Fig.1　Block schematic of the DR circuit

2.1　Delay locked loop

The DLL is used to synchronize the input data with a reference clock. As shown in Fig. 1, the DLL consists of a VCDL, a phase detector (PD), and a loop filter. The delayed data (ddp, ddn) and the reference clock (ckp, ckn) are connected to the input terminals of the phase detector (PD). When the data eye center leads the rising edge of the clock, the PD output 'Up' will be high and 'Dw' will be low, so that the capacitor in the loop filter will be charged to a higher level. For a higher loop filter output, the delay of the VCDL will be larger. On the other hand, when the data eye center lags the rising edge of the clock, the PD output 'Up' will be low and 'Dw' will be high, so that the capacitor in the loop filter will be discharged to a lower level. Then the delay of the VCDL will be smaller. When the loop is in-lock, the data eye center will be located exactly at the rising edge of the clock.

2.1.1　Dynamic bang-bang PD

To compare random data transitions to the clock to provide a signal that represents the phase error, a phase detector (PD) is needed in the DLL. As shown in Fig. 2, the PD is a double-edge-triggered D-flip-flop (DFF), which consists of two latches and a multiplexer. The reference clock (ckp, ckn) is sampled alternately by two latches. The multiplexer will alternatively select the regenerated signal of the two latches for the PD's output. Assuming a gain of 1 for the multiplexer, the output of the PD will be equal to one of the regenerated signals of the two latches, and the output will change only when a data transition occurrs.

At every transition of the input data, the reference clock is sampled by the input NRZ data. When the data eye center leads the rising edge of the clock, the PD output (Qp, Qn) will be high. On the other hand, when the data eye center lags the rising edge of the clock, the PD output (Qp, Qn) will be low. The output of the PD indicates a clear DC component driving the loop towards lock.

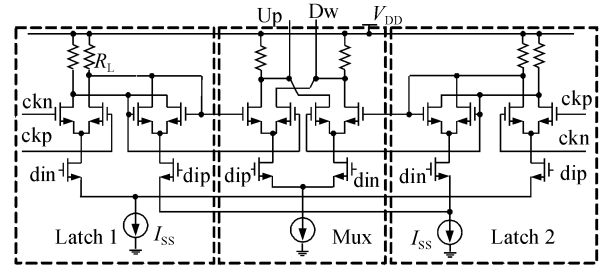


Fig.2　Circuit diagram of the dynamic PD

2.1.2　Loop filter

As shown in Fig. 3, the PD outputs (Qp, Qp) are used to control a current source. The loop filter is charged or discharged according to the polarity of the PD output. The DC component of the loop filter's output drives the loop towards lock. All the components are fully integrated on chip.

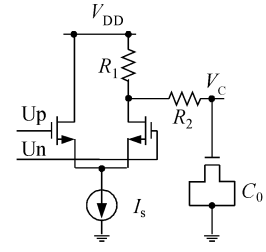


Fig.3　Circuit diagram of the loop filter

2.1.3　Voltage controlled delay line (VCDL)

For continuous delay adjustment, an analog VCDL is used in the DLL. As shown in Fig. 4, the VCDL consists of six delay stages. The bandwidth of the delay cell is designed to be larger than the data rate to avoid serious signal distortion.

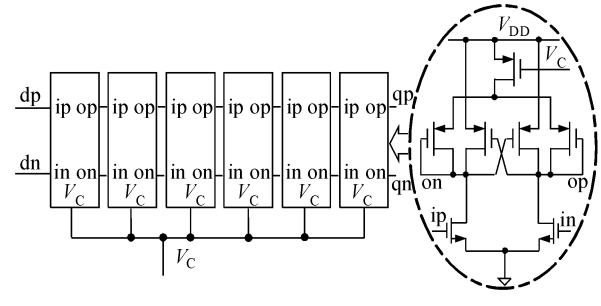


Fig.4　Circuit diagram of the VCDL

2.2 Data decision circuit

The synchronized data is sampled by the reference clock in the data decision circuit. The circuit is implemented with a conventional D-flip-flop that consists of master-slave latches. Figure 5 shows a schematic of one latch. It is a modified source-coupled FET logic (SCFL) latch where the conventional two source followers are removed to save power.

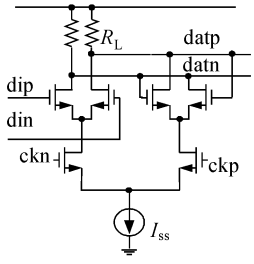


Fig. 5 Circuit diagram of the latch

3 Application: used in SFI-5

There are 16 parallel data channels and a 17th deskew channel between the SerDes device and the framer IC in SFI-5. A parallel DR circuit is needed to recover the 17-channel parallel data. The DR circuit in this design could be conveniently used for SFI-5. As shown in Fig. 6, seventeen identical 2.5Gb/s/ch DR circuits are integrated together to realize the parallel data recovery. For parallel data recovery, a reference clock is provided at the system level, so that the clock is called a global reference clock. In each channel, the input data is synchronized with the global reference clock. Figure 7 shows the simulation waveform of the global clock output and the 17-channel recovered data. Compared with the conventional approaches[2,3], the parallel recovered data of this parallel DR circuit are bit-synchronous so that the following alignment circuit[2] can be avoided.

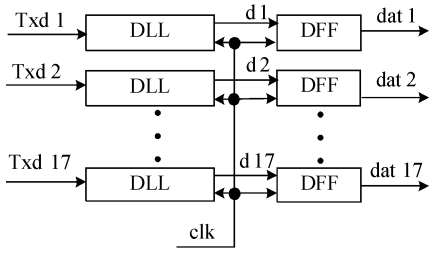


Fig. 6 Block diagram of the 17-channel DR

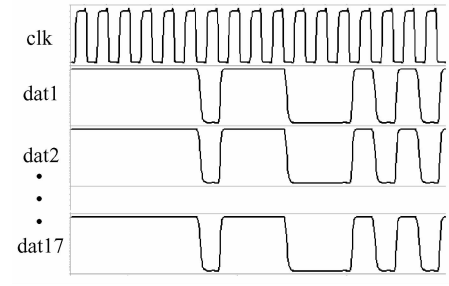


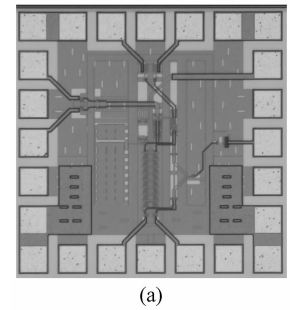
Fig. 7 Simulation waveform of the 17-channel DR

4 Measurement results of the single channel 2.5Gb/s/ch DR IC

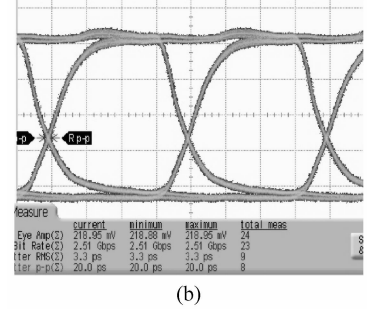
A single channel 2.5Gb/s/ch DR IC was fabricated in TSMC 0.18μm CMOS technology. Figure 8(a) shows a photograph of the IC. The chip area is 675μm×675μm.

The circuit was measured on chip. The main testing instruments include an Advantest D3186 pulse pattern generator, an Advantest D3286 error detector, and an Agilent 86100A oscilloscope.

With a 1.8V supply, the power consumption is about 60mW. With input bit rates of 2.3 ~ 2.8Gb/s, the DLL can lock and the DR circuit can recover the input data with low RMS jitter. With $2^{31}-1$ PRBS input data and a 2.5GHz reference clock, the eye diagram of the recovered 2.5Gb/s



(a)



(b)

Fig. 8 Photograph of the IC (a) and eye diagram of the recovered 2.5Gb/s data (b)

data is shown in Fig. 8 (b). The RMS jitter of the recovered 2.5Gb/s data is 3.3ps and the peak-to-peak (p-p) jitter is 20ps. Using an Advantest D3186 and D3286 for BER testing, the sensitivity of the single channel DR was found to be less than 20mV with 10^{-12} BER. The BER performance is guaranteed by the inherited DLL in the DR.

Compared with the DR circuits reported in previous papers, the jitter performance of this design is better. In Ref. [5], the p-p jitter was 60ps with 2.3Gb/s input data. In Ref. [6], the RMS jitter of the recovered 2.5Gb/s data was 10ps. In Ref. [7], a simulated eye diagram of the 2.5Gb/s CDR indicated that the jitter was larger than this design. The better jitter performance is achieved in this design because a reference clock is used and the center of the input data eye is aligned to the rising edge of the reference clock by the DLL.

5 Conclusions

A 2.5Gb/s/ch data recovery circuit was designed for an SFI-5 interface. A DLL was used to place the center of the data eye exactly at the rising edge of the data-sampling clock. For parallel data recovery applications, all the parallel recovered data are synchronized with the global reference clock so that they are bit-synchronous. Simulation and test results indicate that this design is suitable for parallel data recovery application in an SFI-5 interface.

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2.5Gb/s/ch 0.18μm CMOS 数据恢复电路

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摘要：设计了一个应用于 SFI-5 接口的 2.5Gb/s/ch 数据恢复电路. 应用一个延迟锁相环，将数据的眼图中心调整为与参考时钟的上升沿对准，因而同步了并行恢复数据，并降低了误码率. 采用 TSMC 标准的 0.18μm CMOS 工艺制作了一个单通道的 2.5Gb/s/ch 数据恢复电路，其面积为 0.46mm^2. 输入 $2^{31}-1$ 伪随机序列，恢复出 2.5Gb/s 数据的均方抖动为 3.3ps. 在误码率为 10^{-12} 的条件下，电路的灵敏度小于 20mV.

关键词：数据恢复；延迟锁相环；位同步

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