A Novel Digital Transceiver for CT0 Standard*

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Abstract: This paper introduces a novel digital transceiver for the cordless telephone zero (CT0) standard, which uses a digital modulation and demodulation technique to handle the signal instead of the traditional analog method. In the transmitter, a fractional-N phase locked loop (PLL) is utilized to realize the continuous phase frequency shift key (CPFSK) modulation, and a 2 Ts raised cosine (2RC) shaping technique is used to reduce the occupied bandwidth. In the receiver, a novel digital method is proposed to demodulate the 2RC CPFSK signal. This chip is fabricated using an SMIC 0.35μm mixed signal CMOS process with a die size of 2mm×2mm. With an external low noise amplifier (LNA), the sensitivity of the chip is better than −103dBm.

Key words: RF transceiver; fractional-N PLL; CPFSK; modulator; demodulator
PACC: 7850G
CLC number: TN432 **Document code**: A **Article ID**: 0253-4177(2007)06-0833-09

1 Introduction

The first generation cordless telephone standard, cordless telephone zero (CT0), uses an analog modulation and demodulation (MODEM) technique to transfer voice signals, but it has very bad performance with respect to security and anti-interference. In order to utilize the frequency band of the CT0 standard and improve its performance, a new digital MODEM is proposed in this paper.

A block diagram of the proposed system is shown in Fig. 1. First, the transmitted 24kbps ADPCM data stream is sent into the burst mode controller (BMC) to form packets. Then the signal enters the 2RC shaping block to reduce the bandwidth. Finally, the signal is modulated directly to the desired frequency band through a sigma delta fractional-N PLL.

A dual conversion super-heterodyne RF receiver is used in this chip. The received signal is first down-converted into a 10.7MHz intermediate frequency (IF) by mixing with a variable on-chip local oscillator (LO) and then down-converted into a 455kHz IF by mixing with an external crystal. The second IF signal is sub-sampled by a 256kHz clock and digitized by an internal successive-approximation-register analog to digital converter (SAR ADC). All the following operations, including demodulation, automatic frequency control (AFC), clock and data recovery (CDR), and packet handling, are performed digitally.

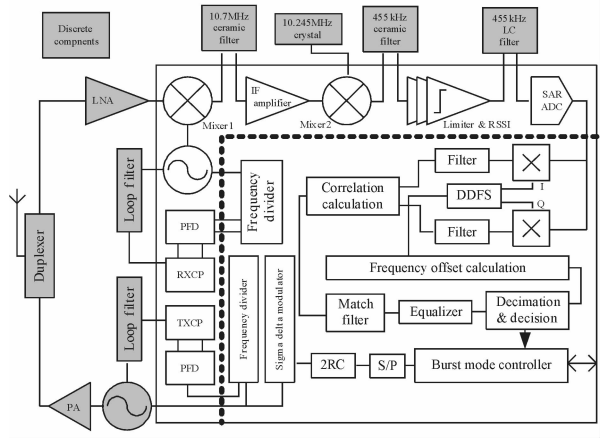

Fig. 1 Block diagram of the proposed system

* Project supported by the Key Project of the National Natural Science Foundation of China (No. 60437030) and the Natural Science Foundation of Tianjin (No. 05YFJMJC01400)
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Received 18 October 2006, revised manuscript received 30 January 2007

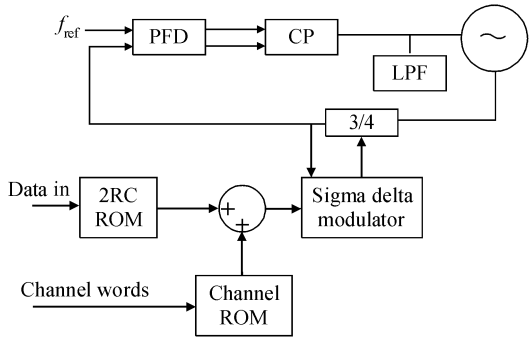

Fig. 2 Detailed block diagram of the modulator

2 System design

2.1 Modulator

For cordless telephone applications, both voice and signaling must be transmitted. In this scheme, the voice is transferred through 4FSK modulation in order to compress its bandwidth, while the signaling is transmitted using 2FSK modulation for the purpose of anti-interference.

A detailed block diagram of the modulator is shown in Fig. 2. According to the regulation of the authority[1], the occupied bandwidth of the modulated signal cannot be greater than 16kHz. In order to meet this requirement and at the same time keep the quality of the voice, a 24kbps ADPCM data stream is chosen as the input signal, and a 2RC 4FSK technique is used to further reduce the bandwidth. The frame format for both the voice and signaling are listed in Table 1. For voice, the baud rate is 12.8kBaud with ±1.6kHz and ±4.8kHz frequency deviation. For signaling, the bit rate is 12.8kHz with ±3.2kHz frequency deviation.

The n RC signal is a kind of partial response signal[2]. The bandwidth of the CPFSK signal using the n RC technique is narrower than that of the pulse amplitude modulation (PAM) method. Thus, the n RC technique is often used in band-limited wireless communication systems.

Table 1 Frame format of the packet

FS (16bits)	ADPCM (240bits)	
PR (48bits)	FS (16)	Signaling (64)

Typical 2RC pulse shaping for 2FSK and 4FSK signals is shown in Fig. 3. For a random PAM data sequence, the 2RC shaping principle is that the current waveform is the sum of the latter half of the former symbol and the former half of the current symbol.

The PLL-based direct modulation technique is a popular method in RF transmitters because of its simplicity and low power consumption. Considering its advantages of fast locking, low noise, and high resolution, a sigma delta fractional-N PLL is chosen in this design. In order to get a fast transient response time, a 12.8MHz crystal oscillator is selected as the reference, and the loop bandwidth is set to 38.4kHz.

A block diagram of the digital sigma delta modulator is shown in Fig. 4. According to Ref. [3], the frequency resolution is determined by f_{ref}/M, where f_{ref} is the reference frequency of the PLL, i.e., 12.8MHz. In this design, the value of M is set to 141111, so the frequency resolution can reach about 45.35Hz.

The DC value of the input signal for the sigma delta modulator will determine the carrier frequency of the transmitter. For a base station the transmitted carrier frequencies are between 48.000 and 48.475MHz with 25kHz space, and for handset these frequencies are from 45.000 to 45.475MHz. Because a 3/4 divider is used in this design, it is easy to obtain the ROM value for different channels by

$$\text{round}[D_{CHi}] = \frac{f_{CHi} - 3f_{ref}}{f_{ref}} \times 2M - M \quad (1)$$

where f_{CHi} is the transmitted carrier frequency of the ith channel, and D_{CHi} represents for the corresponding ROM value. All these values are calculated beforehand and stored in the channel ROM and controlled by the channel words.

The 2RC ROM stores the typical 2RC waveform of different symbols for 2FSK and 4FSK, as shown in Figs. 3 (a)～(d). Figure 3 (e) shows a simple implementation of the 2RC shaping block. Note that the data stored in the 2RC ROM are not the waveform itself but the amplified version. According to the value of M and the corresponding frequency deviation, the gain can be expressed as

$$G = \frac{\text{FD}}{f_{ref}} \times 2M \quad (2)$$

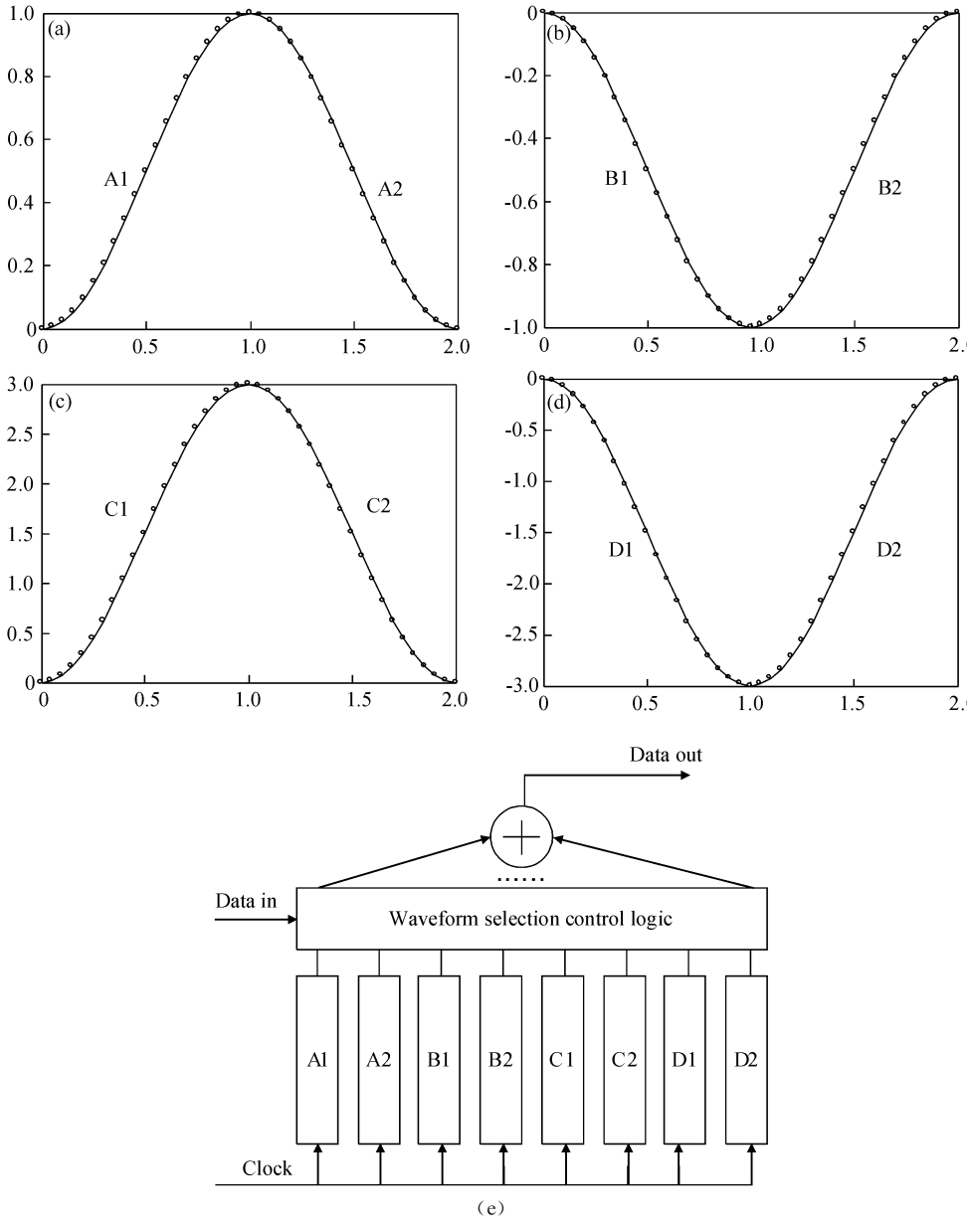

Fig. 3　Typical pulse waveform for 2RC signal ((a)～(d)) and the realization block diagram (e)

where FD is the frequency deviation information for a different symbol. As shown in Fig. 3, after being amplified, the typical data are calculated beforehand and stored in the 2RC ROM.

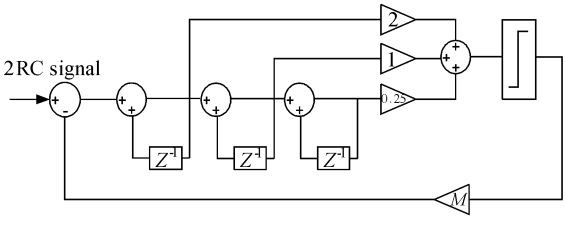

Fig. 4　Block diagram of the 3rd order sigma delta modulator

2.2　Demodulator

The traditional analog demodulation method for 2RC shaping FM signal is to use a frequency discriminator. The shortcoming of this method is that the nonlinearity of the frequency discriminator itself and the frequency error between the base station and the handset will cause a variation in the DC level and the non-symmetric eye diagram. Therefore, an extra AGC, AFC and some nonlinear compensation circuits must be added,

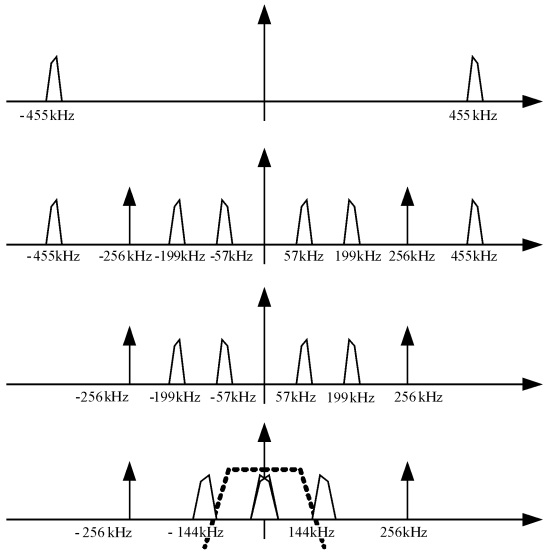

Fig. 5 Sketch map of the frequency conversion for sub-sampling

thus increasing the complexity of the demodulator.

In this paper, a novel digital method is proposed to improve the performance of the traditional analog demodulator. A block diagram of the proposed method is shown in Fig. 1, and its principle is explained in the following.

In this scheme, after two steps of down-conversion, the received signal is shifted from RF to a 455kHz IF. This 455kHz IF signal is then sub-sampled by a 256kHz sampling frequency. As shown in Fig. 5, after sub-sampling, the digital IF signal is located at 57kHz.

Then, the digitized 57kHz IF signal mixes with the quadrature signals $I(n)$ and $Q(n)$ generated by the direct digital frequency synthesizer (DDFS) to convert the IF signal to base-band.

The frequency control words (FCW) of the DDFS are designed to be 12bits long in order to get adequate frequency resolution. The output frequency of the DDFS can be expressed as

$$f_{\mathrm{NCO}} = \frac{f_s \times \mathrm{FCW}}{2^{12}} \tag{3}$$

where f_s is the system clock of the DDFS, which is the same as the sampling frequency, i.e., 256kHz. To generate a 57kHz digital LO signal, the FCW should be equal to 912. The generated quadrature LO signal can be expressed as

$$I_{\mathrm{LO}}(n) = \cos\left(2\pi \times \frac{57n}{256}\right) \tag{4}$$

$$Q_{\mathrm{LO}}(n) = \sin\left(2\pi \times \frac{57n}{256}\right) \tag{5}$$

After digital down conversion, the 57kHz IF signal is converted to base-band. However, some unwanted signals such as those located at -114 and 142kHz are also down-converted, making the demodulator unable to distinguish the desired signal from all these frequency components. Thus, filters must be added after the digital down converter. In order to simplify the design, a filter with the following transfer function is selected:

$$H_{\mathrm{Filter}} = (1 + z^{-1})^5 \tag{6}$$

Simulation results show that the attenuation at 114 and 142kHz is more than 40dB.

Remember that a 2RC technique is used in the modulator in order to reduce the occupied bandwidth. That is to say, the inter-symbol-interference (ISI) has already been introduced factitiously. Thus, in the demodulator an equalizer should be used to eliminate the unwanted ISI. However, what the equalizer needs to deal with is not the received symbol itself but the phase error between successive symbols. Thus, before the equalization, the phase error information must be obtained first. In this design, the coordinate rotation digital computer (CORDIC) algorithm[4] is used to get the phase error information. According to the CORDIC algorithm, there is a relationship:

$$\Delta\phi(n) = \mathrm{tg}^{-1}\frac{\sin(\Delta\phi(n))}{\cos(\Delta\phi(n))} \tag{7}$$

where $\Delta\phi(n)$ represents the phase error information between the nth and the $(n-1)$th symbol. It can be seen that in order to get $\Delta\phi(n)$, $\sin(\Delta\phi(n))$ and $\cos(\Delta\phi(n))$ must be calculated in advance. A convenient technique to calculate these values was proposed in Ref. 5. Letting $I(n)$ and $Q(n)$ represent the I and Q channel outputs, respectively, for the nth symbol, then the dot and cross products can be defined as

$$\mathrm{Dot}(n) = I(n)I(n-1) + Q(n)Q(n-1) \tag{8}$$

$$\mathrm{Cross}(n) = Q(n)I(n-1) - I(n)Q(n-1) \tag{9}$$

If the complex signals are rewritten in polar coordinates, then the dot and cross products can also be expressed as

$$\mathrm{Dot}(n) = A(n)A(n-1)\cos(\Delta\phi(n)) \tag{10}$$

$$\mathrm{Cross}(n) = A(n)A(n-1)\sin(\Delta\phi(n)) \tag{11}$$

where $A(n)$ represents the modulus of the nth

complex signal. From Eqs. (7)～(11), the following equation can be obtained:

$$\Delta\phi(n) = \mathrm{tg}^{-1}\frac{\mathrm{Cross}(n)}{\mathrm{Dot}(n)} \tag{12}$$

Thus the phase error information can be calculated using the CORDIC algorithm.

Following the phase error calculator, a match filter is used to get the optimized receiver performance. Among all the filters in the receiver path, the bandwidth of the match filter is the narrowest. This filter is realized digitally, so its performance will not vary with the process and environment, and thus a fixed coefficient equalizer can be used to compensate for the unwanted ISI introduced by the 2RC modulator and matched filter. The transfer functions of the match filter and the equalizer can be expressed in the following equations[6]:

$$H_{\mathrm{MF}}(z) = 0.5 + z^{-5} + z^{-10} + z^{-15} + 0.5z^{-20} \tag{13}$$

$$H_{\mathrm{EQ}}(z) = 0.0063 - 0.259z^{-10} + 0.62z^{-20} - 0.369z^{-30} + 0.0073z^{-40} \tag{14}$$

The signal is then sent into the decision block to recover the clock and the data. There are two output signals from the decision block, as shown in Fig. 1. One is the data signal after the decision, and the other is sent to a frequency error extraction block to modify the frequency of the DDFS. After automatic frequency correction, the frequency error between the digital LO and the third IF is limited to a reasonable range. Equation (15) is the transfer function of the frequency error extraction filter:

$$H_{\mathrm{Error}}(z) = 0.5 + \frac{0.125}{1 - z^{-1}} \tag{15}$$

The coefficients of this filter can be changed according to the settling and precision requirements of the system.

3 Circuit design

3.1 RF receiver

On the receiver end, the transmitted RF signal is first received by a high performance CMOS super-heterodyne type RF receiver[7]. A block diagram of the RF receiver can be found in Fig. 1. It consists of two mixers, a limiter and received signal strength indicator (RSSI) circuit, a fully differential SAR ADC, and a bias current generator. In the mixer, the speed of the switching transistors must be as fast as possible in order to increase its conversion gain and lower its flicker noise[8]. There are two methods to increase the switching speed. One is to increase the aspect ratios of the switch transistors, but it will increase the load of the LO buffer and thus increase the power consumption. The other method is to decrease the current flowing through the switch transistors. In the simple fully balanced mixer, this current is the same as the bias current of the input stages. Decreasing the bias current will lower the transconductance of the RF input stages, which is not beneficial to the conversion gain and noise performance.

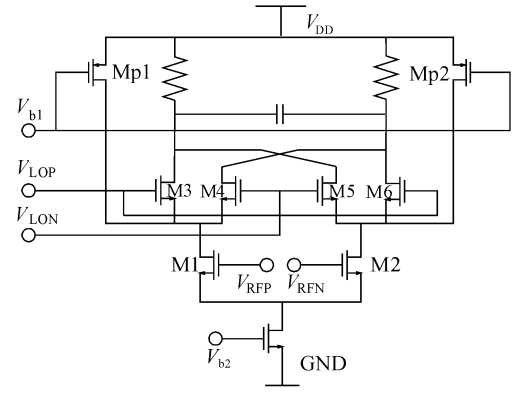

Fig. 6　Schematic of the designed mixer

In this design, two more transistors, Mp1 and Mp2, are added to shunt the current flowing through input transistors as shown in Fig. 6. Without decreasing the bias current, the currents through the switching transistors are greatly reduced. Thus, the switching speed is increased, and then the noise performance is improved without degrading any other performance. In this design, only 20% of the bias current flows through the switching transistors and all of the residual current is absorbed by Mp1 and Mp2.

The limiter is used to amplify the received signal to an acceptable level. The advantages of the limiter over an automatic gain control (AGC) circuit are its simplicity and high speed. The schematic of the designed limiter is shown in Fig. 7. The resistor R_{C} is used to set the output common mode level, and the output swing is determined by IBR_{L}. In this design, the gain of the limiter is about 80dB. Because of the process variation, a

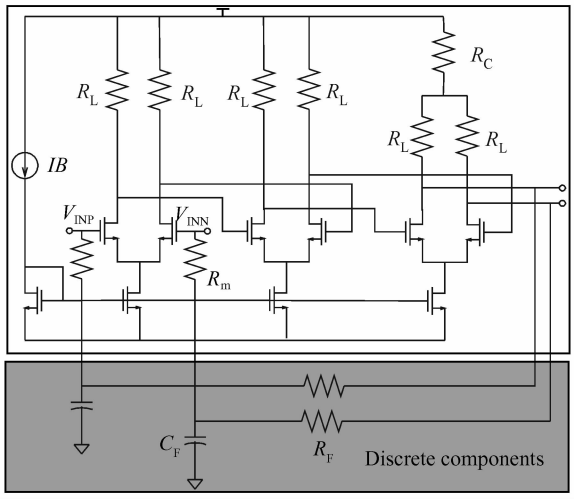

Fig. 7 Schematic of the limiter

DC offset will occur at the input of the limiter, and its value is usually on the order of several mV. Such big a DC offset will also be amplified by the limiter and will bury all desired signal at the output. Thus, a DC offset cancellation circuit must be added in the limiter.

In this design, a DC feedback technique[9,10] is used to solve the problem as shown in Fig. 7. The on-chip resistors and the off-chip capacitors form a low-pass filter in the feedback path. The DC value of the output signal is picked up by this low-pass filter and then fed back to the input port of the limiter. In this way, only DC feedback is effective, and the desired AC signal can be amplified without any degradation.

The simple RSSI is realized by drawing out the outputs of every stage and converting them into current and then adding them together. The ripples are filtered out by an external resistor and capacitor.

Following the limiter is a 6bit SAR ADC. There are two major structures to realize an SAR ADC, i.e., the charge redistribution structure and the resistor-capacitor hybrid structure. From the view of cost, the resistor-capacitor hybrid structure is better than the charge redistribution structure, but from the view of complexity and power consumption, the charge redistribution structure is more suitable for this application. The operation principle and the block diagram of the charge redistribution SAR ADC can be found in the literatures[11~13] and will not be described in this article. Only some critical parts need to be pointed out.

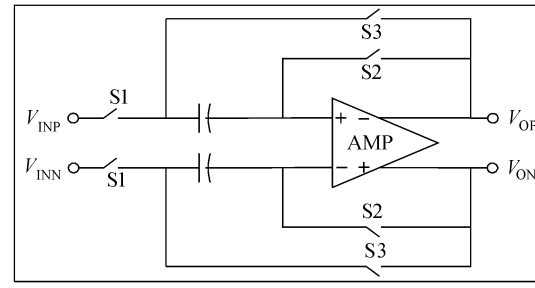

Fig. 8 Block diagram of the sample and hold circuits

The first critical part in the SAR ADC is the sample and hold (S/H) circuit. Although the occupied bandwidth of the received signal is only 16kHz, for band-pass sampling, the bandwidth of the S/H circuit must be large enough to pass all IF signals. In this design, the bandwidth of the S/H circuit is more than 500kHz. The block diagram of the S/H circuits is shown in Fig. 8. Note that a DC offset in the amplifier can be eliminated using this structure[14,15].

The second critical part in the SAR ADC is the comparator with DC offset cancellation as shown in Fig. 9. The comparator used here is a dynamic latch with a pre-amplifier. This configuration can reduce the kick-back noise greatly. In fact, both the pre-amplifier and the latch have DC offset, and they must be cancelled out before normal operation. In this design, an output offset storage technique is used to eliminate the DC offset[15].

The third critical part in the SAR ADC is the reference buffer. For fully differential operation, three reference voltages need to be generated, i.e., V_{refp}, V_{refn} and V_{cm}. The traditional method is to use a series of resistors to generate these voltages. In order to get enough reference precision,

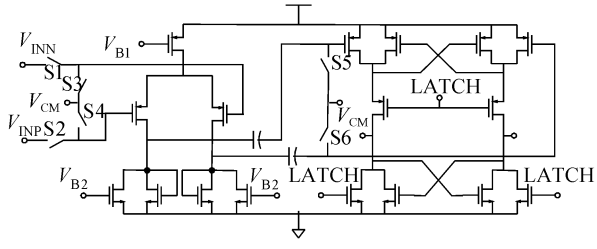

Fig. 9 Schematic of the comparator with DC offset cancellation

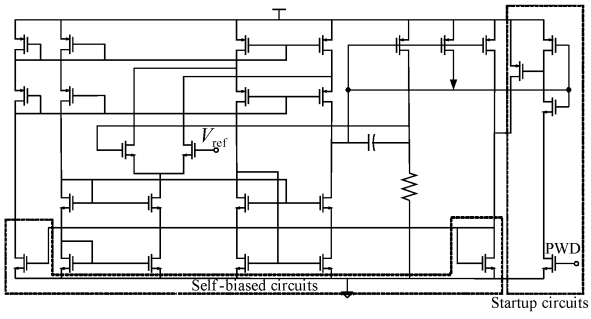

Fig. 10　Schematic of the bias current circuit with startup circuit

the value of the resistors must be relative large, but it will limit the driving capability. In this design, some buffers are added to increase the driving capability. However, the DC offsets in these buffers will also affect the performance of the ADC, so they must be cancelled out. The technique used here is the same as that used in the S/H circuits shown in Fig. 8[15].

A schematic of the bias current generator circuits is shown in Fig. 10. In the schematic, V_{ref} is an external signal produced by an off-chip high precision voltage reference. Because of the high gain property of the amplifier, the voltage at node A should be equal to V_{ref}, so the current flow through the resistor should be equal to V_{ref}/R, where R is placed off-chip. This technique is very popular in products because the precision of the off-chip resistor is much better than that of an on-chip resistor. In this design, the produced bias currents are fed back to the amplifier as its bias current. Thus the whole circuit forms a self-biased loop, and the power consumption of this loop will not vary with the process and environment. In order to make the circuit work properly, a startup circuit must be added as shown in Fig. 10.

3.2　Transmitter

In order to prevent frequency pulling effects[18] in the FDD system, the voltage-controlled oscillators (VCO) of the transmitter and the power amplifier (PA) are placed off-chip, and other circuits such as the phase frequency detector (PFD), charge pump (CP) and digital circuits are integrated on-chip. The PFD and CP, which are similar to those used in the receiver frequency synthesizer, will be described in the following section.

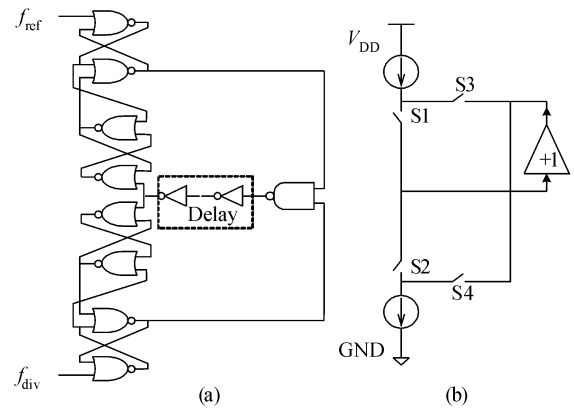

Fig. 11　Block diagram of the PFD (a) and charge pump (b) of receiver PLL

3.3　Receiver frequency synthesizer

The receiver frequency synthesizer is an integer-N PLL. Because the channel space is 25kHz, the reference of the PLL is set to 25kHz.

A block diagram of the PFD is shown in Fig. 11(a), and the delay cell in the reset path is used to eliminate the dead zone. A schematic of the charge pump is shown in Fig. 11 (b). A unit gain buffer is used to eliminate the charge sharing effects[15].

In order to keep the phase noise contributed by the VCO as low as possible; an LC oscillator is used as shown in Fig. 12 (a). Considering the high Q factor characteristic of discrete components, a part of the LC tank is placed off-chip and only the varactor is integrated on-chip. The varactor used here is an I-MOS[16]. The relationship between the control voltage and value of the MOS

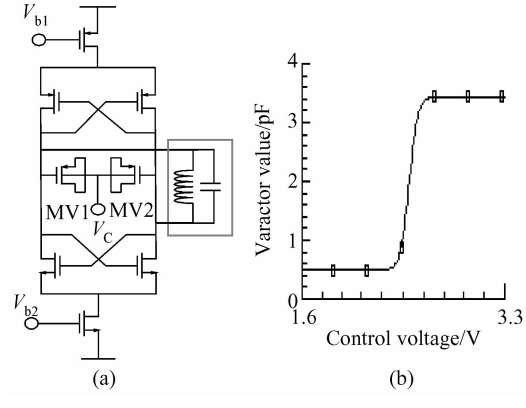

Fig. 12　Schematic of the receiver VCO (a) and the characteristic of the varactor (b)

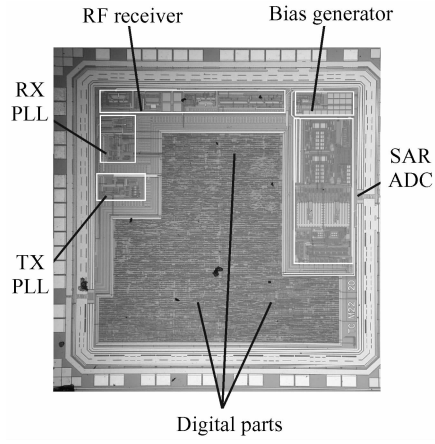

Fig. 13 Chip photograph of the designed RF transceiver

varactor is shown in Fig. 12 (b). For large signal operation, the actual value of the varactor is the average of the maximum and the minimum values[17].

4 Experiment results

This chip is fabricated using an SMIC 0.35μm mixed signal CMOS process. A photograph is shown in Fig. 13. The die size of the whole chip is 2mm×2mm, including PADs.

The power supply and ground connection are very important for a mixed signal SoC. To prevent crosstalk between different building blocks on the same substrate, guard rings are used between the analog and digital parts. At the same time, four separate power supply and ground groups are utilized in the chip, one for RF building blocks such as the LNA and mixer, one for base band analog circuits such as the limiter & RSSI, SAR ADC and bias current generator, one for PLLs, and one for digital circuits.

Because the generator cannot generate a 2RC signal, the limiter output amplitude versus the input signal was measured as a rough estimate of the receiver sensitivity[9]. It can be seen from Fig. 14 that at node A, the limiter reaches its −3dB saturation point. Thus the sensitivity of the receiver is found to be about −103dBm at 50Ω.

The transmitted spectrum is also measured using an Agilent HP4396B as shown in Fig. 15. Because this type of instrument is too old to measure the occupied bandwidth directly, we have to compare this figure with the theoretical results, which are also shown in Fig. 15. The dark line represents

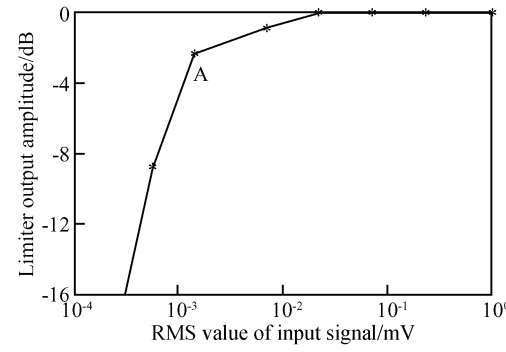

Fig. 14 Limiter output amplitude versus input signal

the measured result, while the other represents the theoretical results. After comparing and calculating using Matlab, it is found that the bandwidth is less than 16kHz.

In normal operating conditions, the whole chip draws 12mA total current from a 3.3V power supply.

5 Conclusion

In this article, a novel digital transceiver is introduced for use in digital cordless telephone

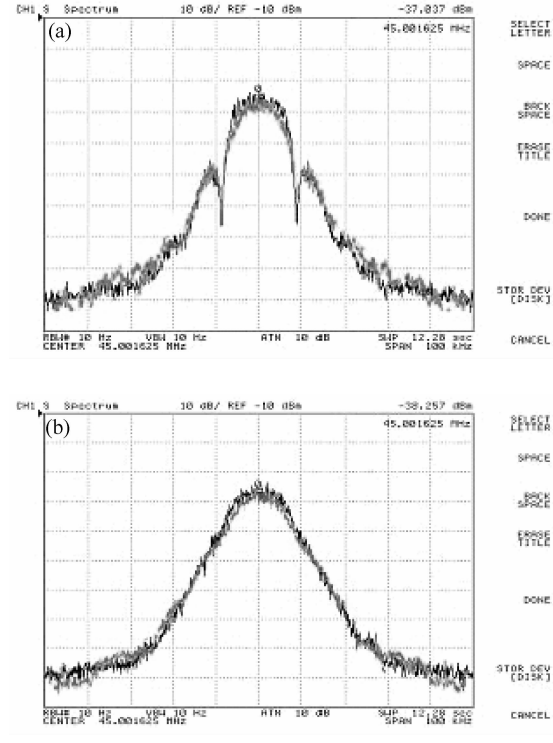

Fig. 15 PSD of transmitted 2FSK (a) and 4FSK (b) signal

applications. The whole chip has been fabricated using an SMIC 0.35um mixed signal CMOS technology. A sigma delta fractional-N PLL is used in the transmitter, and a double conversion superheterodyne structure is used in the receiver. A novel 2RC CPFSK demodulation technique is also proposed in this article. This chip integrates most circuits used in RF applications, including an RF transmitter, RF receiver, ADC, frequency synthesizer, digital demodulator, AFC, and BMC, and is a powerful SoC (system-on-a-chip).

Experimental results show that the sensitivity of the transceiver can reach −103dBm, the power consumption is less than 40mW with a 3.3V power supply, and the occupied bandwidth of the transmitted signal is less than 16kHz.

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一个新颖的用于 CT0 标准的数字收发器*

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摘要: 介绍了一种新颖的用于 CT0 无绳电话标准的数字收发器. 该收发器采用数字调制和解调技术来进行数据传输, 取代了传统的模拟调制解调方式. 在发射机中, 使用小数分频锁相环实现了 CPFSK 调制; 为了减小占用带宽, 使用了 2RC 整形技术. 在接收机中, 使用了一种新颖的数字解调方法实现 2RC CPFSK 信号的解调. 该芯片采用 SMIC 0.35μm 混合信号工艺实现, 芯片尺寸为 2mm×2mm. 使用片外的低噪声放大器, 该芯片的接收灵敏度可达 −103dBm.

关键词: 射频收发器; 小数分频锁相环; 连续相位频移键控; 调制器; 解调器
PACC: 7850G
中图分类号: TN432　　**文献标识码:** A　　**文章编号:** 0253-4177(2007)06-0833-09

* 国家自然科学基金重点项目(批准号:60437030)和天津市自然科学基金(批准号:05YFJMJC01400)资助项目

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2006-10-18 收到, 2007-01-30 定稿