Bandgap Reference Design by Means of Multiple Point Curvature Compensation

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Abstract: A new method, namely multiple point curvature compensation (MPCC), is proposed for the design of a bandgap reference, and its design principles, theoretical derivation, and one feasible circuitry implementation are presented. Being different from traditional techniques, this idea focuses on finding multiple temperatures in the whole range at which the first order derivatives of the output reference voltage equal zero. In this way, the curve of the output reference voltage is flattened and a better effect of curvature compensation is achieved. The circuitry is simulated in ST Microelectronics 0.18μm CMOS technology, and the simulated result shows that the average temperature coefficient is only 1ppm/℃ in the range from −40 to 125℃.

Key words: bandgap reference; curvature compensation; sub-threshold circuit
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1 Introduction

Bandgap voltage references (BGR) have wide applications in various analogue and digital systems, such as analogue-to-digital (ADC) and digital-to-analogue converters (DAC), voltage regulators, and phase-locked loops. The performance and accuracy of these circuits depends directly on the BGR characteristics, i.e. nominal voltage reference value (V_{REF}), temperature coefficient (TC), and temperature range (TR). Generally, first-order compensated BGR can achieve a TC of about 20 ~ 60ppm/℃, while in some high-performance applications, such as high-resolution ADC and DAC, the curvature-compensation technique is required to further reduce the TC of the BGR. Traditionally, such techniques include quadratic temperature compensation[1], exponential temperature compensation[2], linearization of VBE[3], piecewise-linear curvature correction[4], resistor temperature compensation[5], and the NPN-and-PNP-generated current compensation[6], most of which concentrate on cancelling the high-order T terms of the Taylor series of the base-emitter voltage $V_{BE}(T)$ of a bipolar transistor at a single reference temperature T_r over the whole temperature range, and have such drawbacks as more complicated circuits, larger chip area and more complex fabrication processes.

A new idea for curvature compensation of BGRs and a kind of practical circuitry with its simulation results realizing the idea are proposed in this paper. The idea focuses on finding multiple temperatures in the whole range at which the first order derivatives of the output voltage with respect to temperature equal zero. In this way, the curve of the output voltage is flattened, and a better effect of curvature compensation is achieved.

2 General principles of bandgap references

The basic idea of a BGR is to compensate the negative TC of the base-emitter voltage $V_{BE}(T)$ with the positive one of $\Delta V_{BE}(T)$, which is the difference in junction potential between two junctions operating at different current densities. The output voltage, which is actually a weighted sum of $V_{BE}(T)$ and $\Delta V_{BE}(T)$, can attain a zero TC by proper weighting (Fig. 1).

Suppose two bipolar transistors Q1 and Q2, whose saturation currents are I_{S1} and I_{S2}, are injected with collector currents of I_1 and I_2, respectively. The difference of their base-emitter voltages can be written as[8]

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$$\Delta V_{BE}(T) = \frac{kT}{q}\left(\ln\frac{I_1}{I_{S1}} - \ln\frac{I_2}{I_{S2}}\right) = V_T \ln\left(\frac{I_1}{I_2}\times\frac{I_{S2}}{I_{S1}}\right) \quad (1)$$

where k is the Boltzmann's constant, T is the absolute temperature, and q is the charge of an electron. Therefore, $\Delta V_{BE}(T)$ is proportional to the absolute temperature (PTAT).

On the other hand, the relationship of base-emitter voltage to temperature can be expressed as[9]

$$V_{BE}(T) = V_{G0r}\left(1-\frac{T}{T_r}\right) + \frac{T}{T_r}V_{BE}(T_r) - \eta V_T \ln\frac{T}{T_r} + V_T \ln\frac{I_C}{I_C(T_r)} \quad (2)$$

Here, V_{G0r} is the bandgap voltage of silicon extrapolated from a reference temperature T_r to 0K, η is a temperature constant depending on the technology, and I_C is the collector current injected into the bipolar transistor.

Therefore the bandgap reference voltage can be given by

$$V_{REF}(T) = V_{BE}(T) + M\Delta V_{BE}(T) \quad (3)$$

If the ratio M is carefully selected, $\Delta V_{BE}(T)$ can compensate the first-order T term in $V_{BE}(T)$, which is the principle of conventional first-order compensated BGRs.

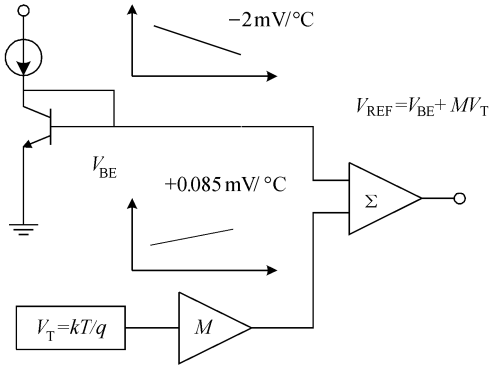

Fig. 1　Hypothetical bandgap reference circuit[7]

3　Traditional high-order curvature compensation techniques

Conventional first-order compensated BGRs fail to compensate the high-order T terms, especially the $V_T \ln T$ term in $V_{BE}(T)$, which can lead to an extra TC of about 10～40ppm/℃. To solve this problem, several techniques have been proposed.

The quadratic temperature compensation technique[1] involves canceling the second-order T term of the Taylor series of V_{BE} at T_r by adding a PTAT^2 term to the reference voltage of a first-order BGR, while exponential temperature compensation[2] involves canceling or reducing the second- or higher-order T terms of V_{BE} by adding an exponential function of temperature. As for the resistor temperature compensation[5], it also demands a Taylor series of reference voltage at T_r in which the second-order T terms of V_{BE} are compensated by the temperature characteristic of different types of resistors.

However, the Taylor formula of finite terms can only guarantee a relatively high accuracy in a very small neighborhood around the reference temperature T_r. That is, the error between the actual and the polynomial value can be large when the temperature T is far from T_r. Unfortunately, in most applications the TR concerned can reach as high as one hundred or more degrees, but the compensation for the Taylor polynomial of V_{BE} is usually to a second-order T term in such circuits. Apparently, the accuracy of such curvature compensation techniques is not so high at some temperatures, i.e. the ends of the temperature range.

4　Multi-point curvature compensation technique

Most conventional first-order and traditional high-order BGRs limit their focus to a single reference point T_r in a relatively large temperature range, hoping that at this temperature the first- or even second-order derivative of reference voltage respect to T could be made zero. However, this can still lead to a fairly large error at other temperatures far away from T_r. Consider, if we properly design the circuit and find several local extrema (peak or valley) of the curve of reference voltage in the whole temperature range, the curve versus temperature will certainly be flattened and the accuracy be improved.

The idea of the proposed curvature-compensation technique is illustrated in Fig. 2. All the pMOS transistors have the same size so that they provide the same drain current, if the channel-length modulation effect is neglected. The bipolar transistor Q2 has an area that is N times that of Q1 and Q3 so that the saturation current of Q2 is

also N times higher. The ratio of resistor R_2 to R_1 is M. We denominate the emitter currents of Q1, Q2, and Q3 by I_{Q1}, I_{Q2}, and I_{Q3}, respectively.

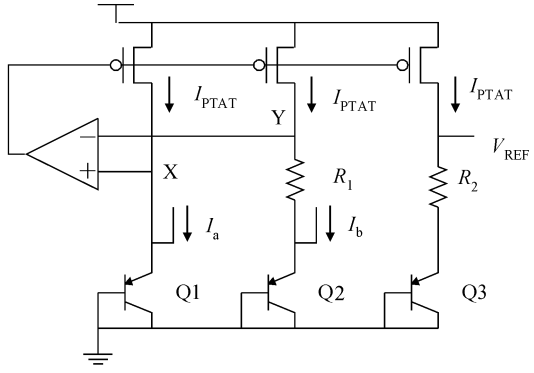

Fig. 2 Structure of the proposed MPCC BGR

The output reference voltage can be expressed according to Eqs. (2) and (3) by

$$V_{REF}(T) = V_{G0r}\left(1-\frac{T}{T_r}\right)+\frac{T}{T_r}V_{BE}(T_r)-\eta V_T\ln\frac{T}{T_r}+V_T\ln\frac{I_{Q3}}{I_{Q3}(T_r)}+MV_T\ln\left(\frac{I_{Q1}}{I_{Q2}}N\right) \quad (4)$$

Considering currents I_{Q1}, I_{Q2} and I_{Q3}, and neglecting the channel-length modulation effect of transistors and the thermal effect of resistors, we have

$$\begin{aligned} I_{Q1} &= I_{PTAT}+I_a \\ I_{Q2} &= I_{PTAT}+I_b \\ I_{Q3} &= I_{PTAT} \end{aligned} \quad (5)$$

The potentials at nodes X and Y are guaranteed to be equal by negative feedback of an operational amplifier. In the design, currents I_a and I_b can be made much smaller than I_{PTAT}, and therefore $I_{Q1}\approx I_{Q2}$ and the PTAT current is given by

$$I_{PTAT}=\frac{\Delta V_{BE}}{R_1}=\frac{V_T}{R_1}\ln\left(\frac{I_{Q1}}{I_{Q2}}\times\frac{I_{S2}}{I_{S1}}\right)\approx\frac{V_T}{R_1}\ln N \quad (6)$$

Computing the first-order derivative of the reference voltage respect to temperature and substituting I_{Q1}, I_{Q2} and I_{Q3} in Eq. (5) for those in Eq. (4), we have

$$\frac{\partial V_{REF}}{\partial T}\approx\frac{-V_{G0r}+V_{BE}(T_r)}{T_r}-(\eta-1)\frac{k}{q}\left(1+\ln\frac{T}{T_r}\right)+\frac{k}{q}M\ln N+MV_T\left(\frac{1}{I_{Q1}}\times\frac{\partial I_{Q1}}{\partial T}-\frac{1}{I_{Q2}}\times\frac{\partial I_{Q2}}{\partial T}\right) \quad (7)$$

Notice that currents I_a and I_b are part of currents I_{Q1} and I_{Q2}, respectively, and we can safely assume that they have a relationship to temperature as below by design:

$$\begin{aligned} I_a &= a_0+a_1T+a_2T^2+a_3T^3 \\ I_b &= b_1+b_1T+b_2T^2+b_3T^3 \end{aligned} \quad (8)$$

To make Eq. (6) hold, we must make sure that

$$|I_a|\ll|I_{PTAT}|,\ |I_b|\ll|I_{PTAT}| \quad (9)$$

Thus the first-order derivatives respect to temperature can be written as

$$\begin{aligned} \frac{\partial I_a}{\partial T} &= a_1+2a_2T+3a_3T^2 \\ \frac{\partial I_b}{\partial T} &= b_1+2b_2T+3b_3T^2 \end{aligned} \quad (10)$$

Therefore we have

$$\begin{aligned} f(T) = \frac{\partial V_{REF}}{\partial T} &\approx \frac{-V_{G0r}+V_{BE}(T_r)}{T_r}-(\eta-1)\frac{k}{q}\left(1+\ln\frac{T}{T_r}\right)+\frac{k}{q}M\ln N+M\frac{V_T}{I_{PTAT}}\left(\frac{\partial I_a}{\partial T}-\frac{\partial I_b}{\partial T}\right) \\ &= \frac{-V_{G0r}+V_{BE}(T_r)}{T_r}-(\eta-1)\frac{k}{q}\left(1+\ln\frac{T}{T_r}\right)+\frac{k}{q}M\ln N+M\frac{R_1}{\ln N}[(a_1-b_1)+2(a_2-b_2)T+3(a_3-b_3)T^2] \end{aligned} \quad (11)$$

Now our target is to set up proper a_i and b_i ($i=1,2,3$) so that we can find three points in the whole temperature range $[T_L, T_H]$ satisfying $T_1<T_r<T_3$ and $f(T_1)=f(T_r)=f(T_3)=0$. Assume

$$\begin{aligned} f_1(T) &= \frac{-V_{G0r}+V_{BE}(T_r)}{T_r}-(\eta-1)\frac{k}{q}\left(1+\ln\frac{T}{T_r}\right)+\frac{k}{q}M\ln N \\ f_2(T) &= K\frac{R_1}{\ln N}[(a_1-b_1)+2(a_2-b_2)T+3(a_3-b_3)T^2] \end{aligned} \quad (12)$$

To make $f(T_r)=0$, we just need to assure that

$$\frac{-V_{G0r}+V_{BE}(T_r)}{T_r}+(1+M\ln N-\eta)\frac{k}{q}=0 \quad (13)$$

$$(a_1-b_1)+2(a_2-b_2)T_r+3(a_3-b_3)T_r^2=0 \quad (14)$$

In fact, Equation (13) is what returns to the conventional first-order BGR circumstances and can be easily satisfied by carefully selecting M and N. On the other hand, Equation (14) gives one more constraint that a_i and b_i ($i=1,2,3$) must meet.

Another two constraints are that at selected T_1 and T_3, we must make sure that $f_1(T_1)=-f_2(T_1)$ and $f_1(T_3)=-f_2(T_3)$, that is

$$K\frac{R_1}{\ln N}[(a_1-b_1)+2(a_2-b_2)T_1+3(a_3-b_3)T_1^2]=$$

$$(\eta-1)\frac{k}{q}\ln\frac{T_1}{T_r}$$

$$K\frac{R_1}{\ln N}[(a_1-b_1)+2(a_2-b_2)T_3+3(a_3-b_3)T_3^2]=$$

$$(\eta-1)\frac{k}{q}\ln\frac{T_3}{T_r} \tag{15}$$

Given a certain η determined by technology and having obtained M and N from Eq. (13), and being aware of the precondition given by Eq. (9), we can certainly find a_i and b_i ($i=1,2,3$) from Eqs. (14) and (15).

Now that we have proved the existence of a certain circuit in which the reference voltage can have several first-order derivative zeros in the whole temperature range, in the practical design we can replace the polynomial temperature-related current in the derivation with an exponential temperature-related one. With the help of circuit simulation software, the accurate sizes of transistors in the circuit can be determined.

5 Circuit design and simulation results

The schematic of our MPCC BGR is given in Fig. 3. In this circuit, currents I_a and I_b are produced by MOS transistors operating in the sub-threshold region, and the pMOS transistor of the current source for the bipolar transistor Q1 is 4 times larger than the others. pMOS transistor P1 is to inject current into Q1, while nMOS transistor N1 is to extract current from bipolar transistor Q2, that is, a negative injection of current. As for

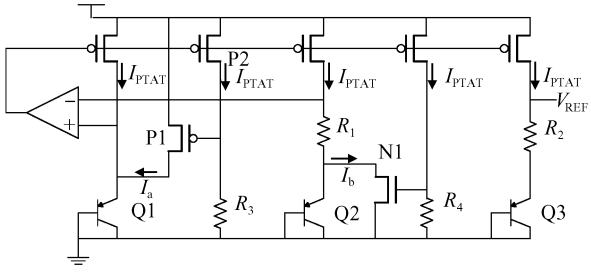

Fig. 3　Schematic of the proposed MPCC BGR

a transistor operating in the sub-threshold region, its drain current can be expressed as[8]

$$I_D \cong \frac{W}{L}I_{D0}\exp\left(\frac{V_{GS}}{V_T}\right) \tag{16}$$

in which I_{D0} is a parameter determined by the process, and V_T, W and L are the threshold and the dimensions of the transistor, respectively. Now we can write I_a and I_b as

$$\begin{aligned} I_a &\cong \frac{W_{P1}}{L_{P1}}I_{D0,P1}\exp\left(\frac{V_{DD}-R_3I_{PTAT}}{V_T}\right)\\ I_b &\cong -\frac{W_{N1}}{L_{N1}}I_{D0,N1}\exp\left(\frac{R_4I_{PTAT}}{V_T}\right) \end{aligned} \tag{17}$$

and then we can safely write Eq. (17) as a Taylor series within the allowable accuracy, so the parameters a_i and b_i ($i=1,2,3$) in Eq. (8) are functions of the transistors' dimensions and resistors' values.

$$\begin{aligned} a_i &= g_i(W_{P1},L_{P1},R_3)\\ b_i &= h_i(W_{N1},L_{N1},R_4) \end{aligned}, \quad i=1,2,3 \tag{18}$$

Taking Eq. (18) into Eq. (15), we can conclude that in theory any arbitrary T_1 and T_3 can be obtained by choosing W_{P1}, L_{P1}, W_{N1}, L_{N1}, R_1, R_3 and R_4, and the solutions might not be unique. Therefore, the circuit in Fig. 3 can successfully realize the function demonstrated in Fig. 2. However, the required caculation is rather complicated, and simulation by EDA tools is a must.

Compared to the proposed circuit in Ref. [10], the part of this circuit formed by pMOS transistors P1 and P2 and resistor R_3 can generate one more zero of the first-order derivative of the reference voltage respect to temperature, at a lower temperature, and therefore our MPCC BGR can further achieve a much lower TC over a wide temperature range.

The circuit is simulated in ST microelectronics 0.18μm technology and via Cadence Spectre simulator. The supply voltage is 3.3V and the total current dissipated is about 90μA. The OPA employed in this bandgap is a simple two-stage one that can achieve a gain of about 100dB with a phase margin of about 64°. Choosing a typical model, in a temperature range between −40 and 125℃, the TC of the compensated BGR can achieve a value as low as 1ppm/℃, as shown in Fig. 4. We can see that before compensation the difference between the largest and smallest output voltages over the temperature range is about 1.5mV, while the same value is reduced to only about 200μV after compensation. Meantime, for the topology in Ref. [10] the same quantity is about 700μV. Besides, when choosing FF and SS models respectively, this value can reach about 700 and 600μV, which also improve the temperature characteristic of the BGR a lot.

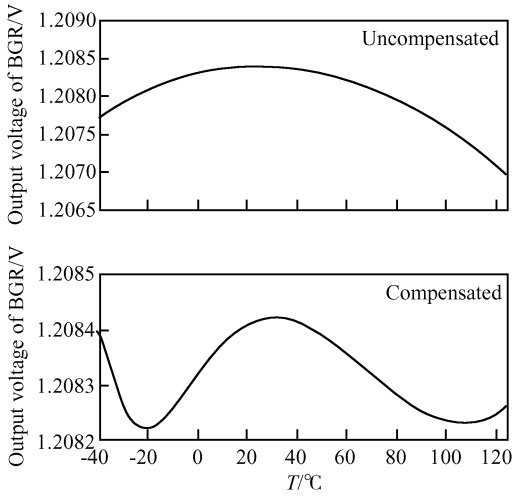

Fig. 4 Reference voltage before and after compensation

If we check the curve of the first- and second-order derivatives of the reference voltage respect to temperature, we can observe that there are three and two zeros in the whole temperature range, respectively. Remember that in most traditional high-order curvature compensation techniques there is only one zero of the derivative.

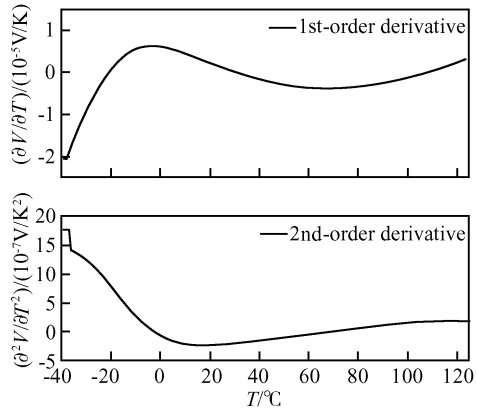

Fig. 5 First- and second-order derivatives of reference voltage with respect to temperature

Finally, we check the curve of currents I_a and I_b with respect to temperature, and their values are really much less than those of I_{Q1} and I_{Q2}, which fit the assumption we made before. In fact, the realization of I_a and I_b is one of the most important factors in this circuit. Were we to find a better circuit realizing such currents, we may find even more than three zeros of the first-order derivative of the reference voltage respect to temperature, and the temperature performance of the BGR may be further improved.

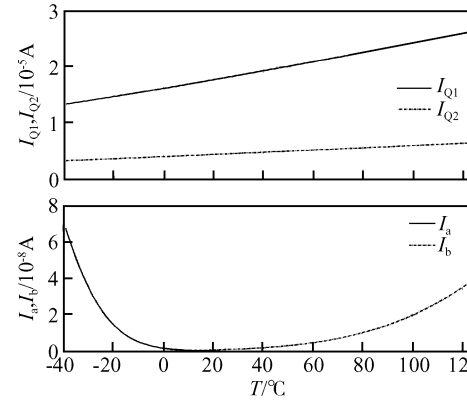

Fig. 6 Current I_{Q1} and I_{Q2} versus I_a and I_b

6 Conclusion

A new multiple-point curvature-compensated CMOS BGR has been proposed. Temperature compensation is achieved by setting more than one zero of first-order derivatives of the reference voltage respect to temperature in the whole temperature range. Compared to the traditional curvature compensation technique, this method is a kind of innovation of the design methodology. The proposed BGR can achieve a fairly small TC and is very simple, requiring only four more MOS transistors and two more resistors.

The circuit is simulated in ST Microelectronics 0.18μm technology and under typical conditions the compensated BGR can achieve a temperature coefficient of 1ppm/℃ over the temperature range of -40 to 125℃. Simulations results convinced us of the feasibility of the MPCC method for BGR design, and in the future the circuit will be taped out and tested.

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多点曲率补偿的带隙基准电压源设计方法

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摘要：提出了一种对带隙基准电压进行多点曲率补偿的新思路，给出了它的设计原理、推导过程和一种实现电路. 与传统的曲率校正方法不同，分布式曲率补偿着眼于在整个温度范围内寻找多个基准输出电压对温度的一阶导数的零点，从而限定基准输出电压随温度变化曲线的幅度，使曲线更平缓，达到提高曲率补偿效果的目的. 采用 ST 公司的 0.18μm CMOS 工艺对实现电路进行了电路模拟，结果表明，在 $-45\sim120$℃ 的温度范围内，采用该方法设计的带隙基准电源的温度系数仅为 1ppm/℃.

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