A Patterned SOI LDMOSFET by Masked SIMOX for RF Power Applications*

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Abstract: A novel patterned-SOI LDMOSFET with a silicon window beneath the p-type channel was designed and fabricated for RF power amplifier applications. This novel device has good DC and RF characteristics. It has no kink effect on output performance, an off-state breakdown of up to 13V, and f_T = 6GHz at DC bias of $V_g = V_d$ = 3.6V. At 1.5GHz, a power-added efficiency (PAE) of 50% is achieved with an output power of up to 27dBm from this device.

Key words: patterned-SOI; LDMOSFET; SIMOX; RF power amplifier
EEACC: 1220; 1350; 7310
CLC number: TN386.1 **Document code**: A **Article ID**: 0253-4177(2007)04-0480-04

1 Introduction

The lateral double diffused MOSFET (LDMOSFET) is a popular candidate in power amplifier applications. But its high parasitic output capacitance and leakage current on bulk substrate result in low power gain and power-added efficiency. The silicon-on-insulator (SOI) LDMOSFET has much lower parasitic output capacitance and leakage current, making it a better candidate for high frequency applications[1~4]. However, the buried oxide layer induces a serious floating body effect in partially-depleted SOI devices, such as a kink in the *I-V* characteristics, which gives rise to distortion during power operation and results in low power efficiency[5]. In addition, application of SOI in a high-power integrated circuit is limited by the self-heating effect caused by the poor thermal conductivity of the insulating SiO_2 layers.

Body contact technology[5], shallow source implantation technology[6], and patterned-SOI technology[7,8] are suggested to eliminate the floating body effect. However, a body contact structure will reduce gate width effectively, and a shallow source implantation requires careful process control, especially for a thin-film SOI structure. Ren *et al*.[7] fabricated a patterned-SOI LDMOSFET without buried oxide beneath the source and p-type well regions, resulting in poor isolation between adjacent circuits. In addition, the process to form the patterned SOI materials is too complex to be accepted widely. Park *et al*.[8] simulated a patterned-SOI structure without buried oxide underneath the drain region, which increases the leakage current and parasitic output capacitance.

In this paper, a novel patterned-SOI (PSOI) LDMOSFET structure is proposed. The buried oxide is interrupted beneath the p-type well region, which is called a silicon window. PSOI materials can be realized easily by masked SIMOX technology[9,10].

2 Device fabrication

The main processes to form PSOI materials are illustrated bellow. Thick thermal SiO_2 was grown on p-type wafer (10 ~ 20Ω · cm) and etched selectively where the buried oxide layer would be formed. Then oxygen ions were implanted (3.0×10^{17} cm^{-2}, 100keV, by ULVACIM-200) and annealed (1300℃, 5h). Figure 1 shows a cross section of the PSOI LDMOSFET. The thickness of

* Project supported by the Science and Technology Projects of the Department of Education of Zhejiang Province of China (No. KYG051205053)
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Received 27 October 2006, revised manuscript received 9 November 2006

the active silicon is about 0.2μm, the thickness of the buried oxide is about 0.1μm, and the length of the silicon window is about 0.8μm.

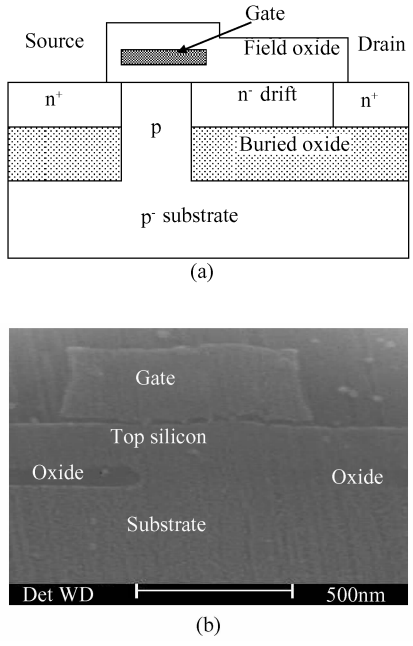

Fig. 1　Schematic cross section of PSOI LDMOSFET (a) and SEM image (b)

The PSOI LDMOSFET was fabricated to be compatible with a standard 1μm CMOS process. Each cell has 20 fingers with a 50μm gate finger width for a 1mm total gate width. The gate oxide was thermally grown on SOI of 30nm thickness and 1μm length. Boron ions (1.5×10^{13} cm^{-2}, 35keV) were implanted into the source region, and then annealed for 2h at 1150℃ to form p-well doping. The length of the drift region was 0.5μm. The drift region doping was achieved by a blanket implantation of phosphorus (2×10^{12} cm^{-2}, 50keV) and annealing. An oxide was deposited by TEOS and etched selectively to define the drift region and to form a spacer wall. After the source and drain regions were made by phosphorus ion implantation, a titanium silicide was performed.

3　Results and discussion

The DC output characteristics are shown in Fig. 2. The gate voltage varies from 2 to 5V by 1V steps. The output characteristics curves in the saturation region of the PSOI LDMOSFET are very flat, which prove that the floating body effect, like the kink effect, is eliminated by the novel PSOI structure we proposed, because the holes, generated by the impact ionization, in the neutral p-type region can easily flow to the substrate through the silicon window. The leakage current is about 10^{-8} A. The on-state and off-state breakdown voltages of the PSOI LDMOSFET are 8 and 15V, respectively, which can satisfy the requirements of RF power amplifiers in cell phones. Here we should also explain that the output drain current is locked to 100mA for self-protection of the equipment.

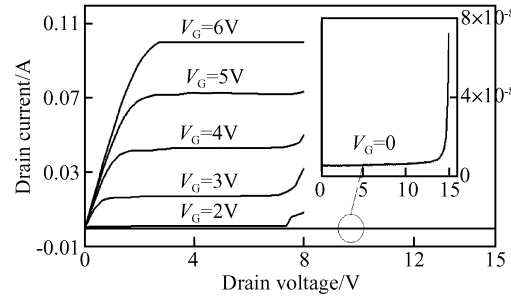

Fig. 2　DC output characterization of the device

The small signal characterization was performed using coplanar waveguide GSG probes. The *S*-parameters of the devices were measured to 10GHz and de-embedded by open-short structures. The f_T of the PSOI LDMOSFET is about 6GHz at $V_g = V_d = 3.6$V, calculated by mag(H_{21}) of Fig. 3.

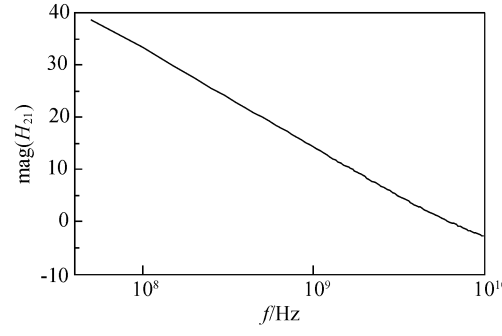

Fig. 3　Mag(H_{21}) versus frequency of the device at $V_d = V_g = 3.6$V

The on-wafer RF power characteristics of the PSOI LDMOSFET, measured by a Focus Programmer Tuner 1808, are shown in Fig. 4 at a supply voltage of 3.6V and a frequency of 1.5GHz. The bias current was 30mA and the input and output matching networks were set to 102 + j52Ω and

161 + j114Ω, respectively, to maximize the PAE. Under these conditions, the RF power cell had a power gain of 16dB in the linear region, the PAE and output power up to 50% and 27dBm, respectively. The frequency spectrum of the cell was also monitored, as shown in Fig. 5, and no oscillation or self-oscillation occurred.

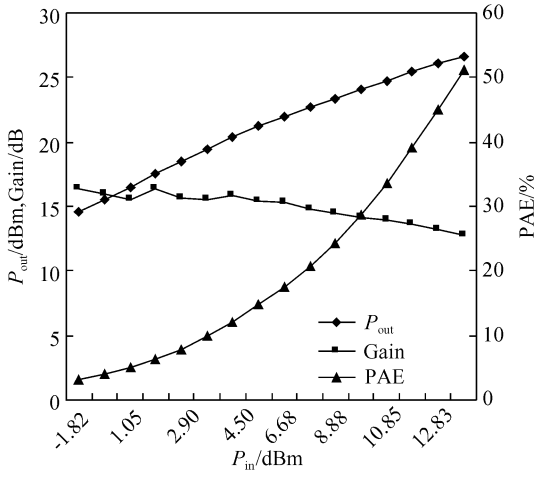

Fig. 4 RF power characteristics of the PSOI at 1.5GHz

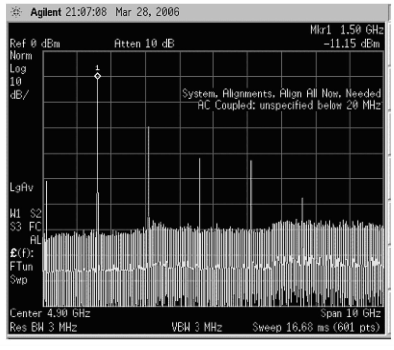

Fig. 5 Frequency spectrum of the device at optimum matching condition

4 Conclusion

An RF power PSOI LDMOSFET was fabricated using masked SIMOX technology and a standard SOI CMOS process. This novel device has good DC and RF power characteristics. It has no kink effect on output performance, an off-state breakdown of up to 15V, f_T = 8GHz at DC bias of $V_g = V_d = 3.6$V, and a PAE of 50% with an output power of up to 27dBm at 1.5 GHz. This is a promising technology for RF PAs in the future generations of highly integrated wireless systems.

References

[1] Luo Luyang, Fang Jian, Luo Ping, et al. Breakdown characteristics of novel SOI-LDMOS with reducing field electrode and U-type drift region. Chinese Journal of Semiconductors, 2003, 24(2): 194 (in Chinese) [罗卢杨, 方健, 罗萍, 等. 具有降场电极 U 形漂移区 SOI-LDMOS 的耐压特性. 半导体学报, 2003, 24(2): 194]

[2] Matsumoto S, Hiraoka Y, Sakai T. A high-efficiency thin-film SOI power MOSFET having a self-aligned offset gate structure for multi-gigahertz applications. IEEE Trans Electron Devices, 2001, 48(6): 1270

[3] Trivedi M, Khandelwal P, Shenai K, et al. Design and modeling of bulk and SOI power LDMOSFETs for RF wireless applications. Solid-State Electron, 2000, 44: 1343

[4] Fiorenza J G, Antoniadis D A. RF power LDMOSFET on SOI. IEEE Electron Device Lett, 2001, 22(3): 139

[5] Matasumoto S, Hiraoka Y, Sakai T. Radio-frequency performance of a state-of-art 0.5μm-rile thin film SOI power MOSFET. IEEE Trans Electron Devices, 2001, 48(6): 1251

[6] Fiorenza J G, Del Alamo J A. Experimental comparison of RF power LDMOSFETs on thin-film SOI and bulk silicon. IEEE Trans Electron Devices, 2002, 49(4): 687

[7] Ren C H, Cai J, Liang Y C, et al. The partial silicon-on-insulator technology for RF power LDMOSFET devices and on-chip microinductors. IEEE Trans Electron Devices, 2002, 49(12): 2271

[8] Park J M, Grasser T, Kosina H, et al. A numerical study of partial-SOI LDMOSFETs. Solid-State Electron, 2003, 47(2): 275

[9] Dong Yemin, Wang Xi, Cheng Jin, et al. Low defect density and planar patterned SOI materials by masked SIMOX. Chem Phys Lett, 2003, 378: 470

[10] He Ping, Dong Yemin, Wang Xi, et al. Experimental results on drain and source on insulator MOSFETs fabricated by local SIMOX technology. Solid-State Electron, 2003, 47: 1061

一种适合射频功率放大器应用的图形化 SOI LDMOSFET 新结构*

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摘要：设计并制备了一种新颖的在栅下开硅窗口的图形化 SOI LDMOSFET.该器件具有良好的直流和射频特性：输出曲线平滑，没有明显翘曲(kink)效应；静态击穿电压为 13V；在栅漏偏压为 3.6V 时，截至频率为 6GHz.负载牵引测试表明，该器件在 1.5GHz 时，PAE 为 50%，输出功率为 27dBm，表明该器件适合射频功率放大器的应用.

关键词：图形化 SOI；LDMOSFET；SIMOX；射频功率放大器

EEACC：1220；1350；7310

中图分类号：TN386.1　　**文献标识码**：A　　**文章编号**：0253-4177(2007)04-0480-04

* 浙江省教育厅科技计划资助项目（批准号：KYG051205053）

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2006-10-27 收到，2006-11-09 定稿