A 16bit 96kHz Chopper-Stabilized Sigma-Delta ADC

Cao Ying, Ren Tenglong, and Hong Zhiliang†

(*State Key Laboratory of ASIC & Systems, Fudan University, Shanghai 201203, China*)

Abstract: A 16bit sigma-delta audio analog-to-digital converter is developed. It consists of an analog modulator and a digital decimator. A standard 2-order single-loop architecture is employed in the modulator. Chopper stabilization is applied to the first integrator to eliminate the $1/f$ noise. A low-power, area-efficient decimator is used, which includes a poly-phase comb-filter and a wave-digital-filter. The converter achieves a 92dB dynamic range over the 96kHz audio band. This single chip occupies 2.68mm^2 in a 0.18μm six-metal CMOS process and dissipates only 15.5mW power.

Key words: sigma-delta modulation; chopper stabilize; decimator; poly phase; wave digital filter; on-chip noise

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1 Introduction

The proliferation of mainstream consumer digital audio equipment has generated increasingly stringent requirements for high-performance analog-to-digital converters (ADC) used in the audio signal processing chain. Sigma-delta ADCs are the most popular converters for audio applications currently. Several 16bit converters have been developed throughout the years, but they have always been restricted to the audio-frequency range, i. e. 20kHz. With the widespread use of stereo audio techniques, this range should be larger. 96kHz is an optimal stereo audio-frequency range, and a converter with 16bit accuracy and 96kHz bandwidth is suitable for stereo audio applications.

This paper presents a low-power low-distortion audio ADC intended for the mainstream consumer audio market. It includes an analog modulator and a digital decimation filter. According to the simulation results, the converter achieves a dynamic range greater than 98dB within a bandwidth of 96kHz. The whole chip occupies 2.68mm^2 (including pad area) in a 0.18μm six-metal CMOS process.

2 System level design of modulator

2.1 Sigma-delta modulator topology

To achieve 16bit resolution, a 98dB circuit noise contribution below the full-scale signal voltage is needed. A two-order modulator with an oversampling ratio of 256 was chosen to satisfy this requirement. A standard 1-stage 2-order modulator architecture was reported several years ago[1]. In this work, it has been found that at higher oversampling ratios, the performance improvement obtained by increasing the oversampling ratio is reduced. Flicker noise in the input transistors of the first integrator has been found to be the primary limitation when the signal is oversampled by a factor greater than 64. Chopper stabilization is applied to the first integrator to eliminate the $1/f$ noise.

Figure 1 shows the circuit topology for the modulator. The modulator operation is controlled by two nonoverlapped clock phases, namely sampling phase ck1 and integration phase ck2. In order to attenuate the signal-dependent clock feedthrough, delayed versions of the two phases (ck1d and ck2d) are also provided. The comparator is controlled by both ck1d and ck2d, and the feedback DAC is activated by ck2d.

As can be seen from Fig. 1, capacitor C_s is used for sampling the analog input during ck1 and the relevant voltage reference during ck2. This structure has a 3dB kT/C noise advantage over traditional structures, which use different capacitors for sampling the input and voltage reference.

† Corresponding author. Email: zlhong@fudan.edu.cn
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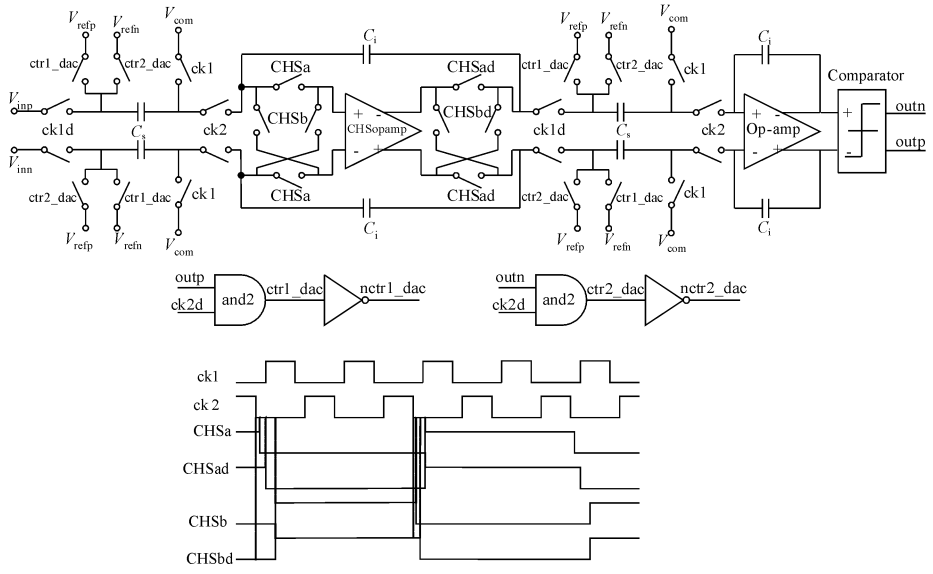

Fig. 1　Modulator circuit topology

This is because there is only one capacitor used for sampling in this structure, while in the traditional structure, there are two. Meanwhile, in the traditional structure, the values of different capacitors used for sampling the input and voltage reference are always the same. Thus, the thermal noise induced by the sampling capacitors in the traditional structure is twice that in this structure. This improvement represented logarithmically is 3dB. In addition, the topology shown in Fig. 1 can draw negligible signal-dependent current from the signal input.

2.2　Chopper-stabilization implementation

For voice-band application of modulators, the dominant noise source is often the $1/f$ noise component of the operational amplifier[2]. The $1/f$ noise can be reduced by a number of methods. One technique for reducing the $1/f$ noise density at low frequencies is chopper-stabilization (CHS). The CHS technique was introduced about 50 years ago to realize high-precision DC gains with AC-coupled amplifiers[3]. This technique applies modulation to transfer the signal to a higher frequency where there is no $1/f$ noise, and then demodulates it back to the baseband after amplification. Meanwhile, the $1/f$ noise component has been shifted to the odd harmonic frequencies of the chopping square wave. The $1/f$ noise density at low frequencies is now equal to the "folded-back" noise from those harmonic $1/f$ noise components. Therefore, if the chopper frequency is much higher than the signal bandwidth, the $1/f$ noise in the signal band will be greatly reduced by the use of this technique.

2.3　Behavior-level modeling and building-blocks specification

Let M be the oversampling ratio, L the integrator's orders, and N the quantizer's output steps. Theoretically, the dynamic range of a classical second-order modulator can be expressed as[4]

$$\mathrm{DR} = 10\lg\left[\frac{3}{2}(2L+1)\right] - 10L + 6(L+0.5)\log_2 M + 20\lg(2^N - 1) \qquad (1)$$

In our design, this value is 108.75dB. Unfortunately, it is difficult to achieve due to the nonidealities of analog components. A behavior-model of the modulator was constructed and a behavior-level simulation was run at first. During this process, the overall modulator specifications were mapped onto each of the building-block specifications. Meanwhile, the effects of finite DC-gain, bandwidth and slew-rate of the op-amp and hysteresis of the comparator were taken into consideration, which were the main sources of the circuit's nonidealities.

An approximate expression for the quantization noise when the quantizer is modeled by an additive white-noise source is

$$S_B = \frac{\pi^4}{5} \times \frac{1}{M^5} \times \frac{\Delta^2}{12}, \quad M \gg 1 \qquad (2)$$

The coefficient Δ is the output-range of the quan-

Table 1 Building-block specifications

SPEC:98dB@96kS/s			Value
Integrator & op-amp	Integrator	Settling time (max)	9ns
		Settling error (max)	0.1%
		Sampling capacitor	1pF
		Integration capacitor	2pF
	Op-amp	Open-loop gain	>70dB
		Bandwidth	350MHz
		Slew rate	150V/μs
		Output swing	2V
		Phase margin	60°
Comparator	Hysteresis (max)		30mV
	Resolution time		9ns
Clock	Non-overlapping time		1ns
	Advanced cut-off time		0.5ns

tizer. Let H_0 be the DC gain of the integrator, which is nearly the same value of the op-amp's DC open-loop gain. Let ΔS_B be the increase of the in-band quantization S_B. We can obtain the following equation:

$$\frac{\Delta S_B}{S_B} = \frac{5}{\pi^4}\left(\frac{M}{H_0}\right)^4 + \frac{10}{3\pi^2}\left(\frac{M}{H_0}\right)^2 \quad (3)$$

According to the simulation results, in order to prevent the increase of the quantization noise beyond 1dB, H_0 should be much larger than 60dB.

The comparator appears after the loop gain block and before the output terminal, and the nonidealities associated with it are shaped by the loop in the same way that the quantization noise it produces is shaped. But there are still some circuit design issues to watch out for[4]. One of them is hysteresis. Let h be the comparator hysteresis. Then the sum of the quantization noise and the hysteresis is

$$S_N = \frac{\pi^{2L}}{2L+1} \times \frac{\Delta^2}{M^{2L+1}}\left[\frac{1}{12} + 4h^2\right], \quad M \gg 1 \quad (4)$$

From analytical results, we can get that S_N is virtually unchanged for hysteresis as large as 10% of the full scale converter input. Table 1 shows the system specification and overall performance requirements for all building-blocks.

3 Analog circuits implementation

3.1 Op-amp design

The op-amp of the integrator is one of the most critical circuits in a sigma-delta converter. The primary design criteria of the op-amp are its DC open-loop gain, setting performance, and output swing. As shown in Fig. 2(a), a two-stage fully

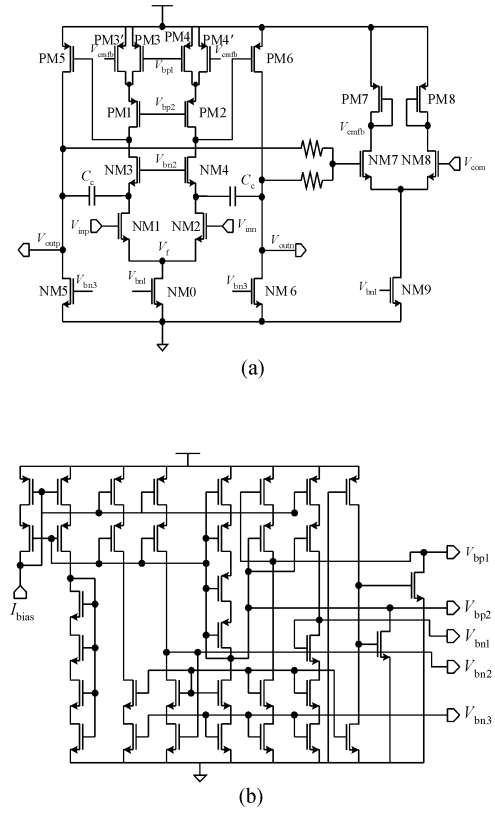

Fig. 2 (a) Main op-amp of the integrator; (b) Bias circuits of the op-amp

differential structure is used for both integrators. A telescopic amplifier is used as the first stage, which is followed by a co-source stage structure as the second stage. A cascode-style compensation strategy has been used between two stages. In order to stabilize the output common-mode voltage, a continuous-time common-mode feedback circuit is employed, which consists of two feedback resistors and a small-current amplifier. The sizes of PM7, PM8, and NM9 are proportional to PM3′, PM4′, and NM0. The bias voltages used in the main amplifier are all generated by a current-bias style voltage-generating circuit, which consists of 6 current-mirror branches and a start up circuit (shown in Fig. 2(b)).

The simulated open-loop DC gain is 91.2dB, and the unity-gain bandwidth is 370MHz. These results are sufficient for the system requirements, which are presented in Table 1, and also some margins are left. The total current consumed by the op-amp is 2.4mA.

There is a little difference between two op-amps in the two integrators. As described above, for reducing the flicker noise produced by the op-

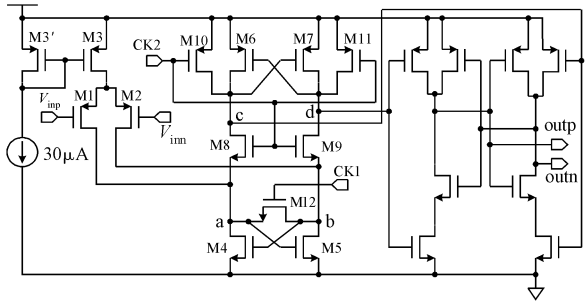

Fig. 3　Schematic of the comparator

amp, 4 chopper-stabilized switches are used on both input port and output port of the first op-amp (shown in Fig. 1). There is no similar scheme adopted with the second op-amp, since the noise introduced by it is suppressed by the noise-shaping loop.

3.2　Comparator design

In this design, the performance's requirements for the comparator are quite relaxed, and they are given in Table 1. But the comparator must be fast.

The comparator[5] schematic is presented in Fig. 3. It consists of a differential input pair (M1, M2), a CMOS latch circuit, and an S-R latch. The CMOS latch is composed of an n-channel flip-flop (M4, M5) with a pair of n-channel transfer gates (M8, M9) for strobe and an n-channel switch (M12) for resetting, and a p-channel flip-flop (M6, M7) with a pair of p-channel precharge transistors (M10, M11). Ck1 and Ck2 are the two non-overlapping clocks.

The reference current can be increased to raise the comparison speed. However, a larger offset will be induced, and a lower accuracy will be achieved. The simulation result shows the comparator can perform comparisons with 1mV sensitivity for sampling rates of 50MHz with $I_{bias} = 30\mu A$.

4　Decimator

While the resolution and conversion rate of the sigma-delta ADC are typically determined by the analog component, its power and die area are governed largely by the digital decimation filter. To reduce power consumption and save die area, a multistage decimator structure was used in Ref. [6]. The filter described herein employs a 4-

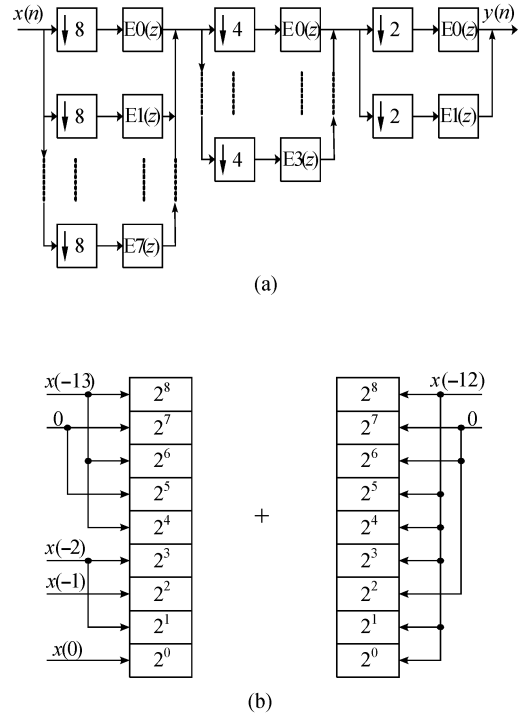

Fig. 4　(a) Polyphase comb-filter topology; (b) Multiplier-free and adder-less 1bit input stage

stage structure. Unlike the scheme presented in Ref. [6], in order to optimize this design further, some special methods are used, such as a polyphase comb-filter structure and a wave digital filter structure. The decimator is required to have −98dB of stopband rejection, and the passband of the filter lies between 0～96kHz.

After the modulator 1bit output, a poly-phase comb-filter follows[7]. The poly-structure can efficiently decrease the operation frequency of the major part of the filter, only leaving a few switching components operating on the sampling rate. This comb filter is designed to achieve a decimation factor of 64. To reduce the circuit complexity, it can also be decomposed into 3 stages. In order to perform this high decimation factor at the input of the first stage, we can also exploit the polyphase decomposition. The z-domain transfer function of the comb filter is given by

$$H(z) = H_1(z)H_2(z)H_3(z) = \left(\frac{1-z^{-8}}{8\times(1-z^{-1})}\right)^4 \times \left(\frac{1-z^{-4}}{4\times(1-z^{-1})}\right)^4 \times \left(\frac{1-z^{-2}}{2\times(1-z^{-1})}\right)^4 \quad (5)$$

This comb topology is shown in Fig. 4(a). Although coefficients resulting from this decomposi-

tion require expensive multiplication operations and larger word length, the overall power consumption is lower. This is due to the significant reduction of the operating frequency.

Since the input is a stream of 1bit data, a multiplier-free and adder-less structure can be implemented as the input stage of the comb filter[8]. A description of this scheme is shown in Fig. 4(b) (the presented circuit is used for calculating "$x(0)+4x(-1)+10x(-2)+336x(-13)+315x(-12)$").

The multistage comb filter is followed by a decimation-by-2 half-band FIR filter. The Parks-McClellan algorithm was used to estimate the order of the filter. The number of filter taps was 22. To reduce the coefficients' complexity, the canonical signed-digit (CSD) form was used. The CSD representation of a fractional filter coefficient c has the form

$$c = \sum_{k=1}^{K} s_k 2^{-k} \tag{6}$$

When $s_k \in \{1, 0, -1\}$, K is the number of bits in the coefficient and no two nonzero digits s_k are adjacent.

To save much more area, a wave digital filter (WDF) was employed as the last decimation stage[9]. It consumed much less hardware than the case for which an FIR was used as the last stage, since there were feedbacks used in it. The wave digital filter used in this design has 31 filter-taps, and also, to reduce system sensitivity, the whole WDF was decomposed into 3 stages (stage 1 and stage 2 are the same).

$$\begin{aligned} H_{1,2}(z) &= H_{\mathrm{D}}(z)(H_{\mathrm{E}}(z))^2 + z^{-1}(H_{\mathrm{E}}(z))^2 \\ H_3(z) &= H_{\mathrm{D}}(z)H_{\mathrm{E}}(z) + z^{-1}(H_{\mathrm{E}}(z))^2 \end{aligned} \tag{7}$$

The cell D and cell E have transfer functions as follows:

$$H_{\mathrm{D}}(z) = \frac{k + z^{-2}}{1 + kz^{-2}}, H_{\mathrm{E}}(z) = \frac{-(k-1) + z^{-2}}{1 - (k-1)z^{-2}} \tag{8}$$

The coefficients of the WDF were also coded in CSD form, which could reduce the coefficients' complexity, as mentioned above.

5 Measurements

Since both the analog and digital circuitries of the ADC are embodied in the same integrated circuit, preventing the large electronic noise generated by digital circuitry coupling into the sensitive analog circuitry is needed[10]. For reducing the deleterious effects of electrical noise generated by the on-chip digital circuitry, the leading edge of the digital slave clock Dclk is delayed with respect to the trailing edge of the sampling analog clock ck1. This delay is illustrated in Fig. 5.

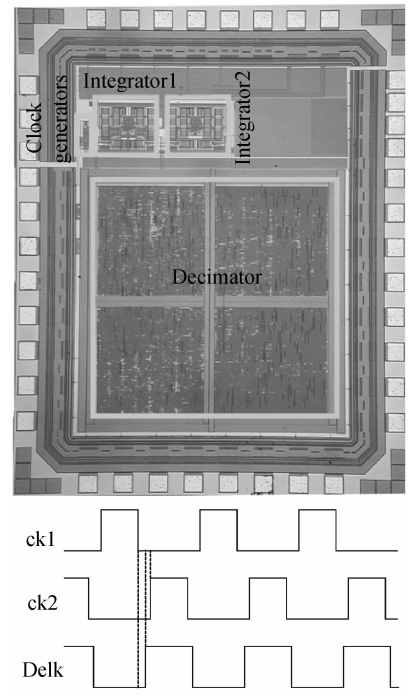

Fig. 5 Die photo and chip clock management scheme

The whole chip integrates the analog sigma-delta modulator and the digital decimation filter. It was implemented in a 0.18μm 6-metal CMOS process. The die has an area of 2.68mm^2 and 39 pads. Both the analog and digital components used 1.8V power supply. Figure 5 also shows a die photo of the whole chip.

Figures 6 (a) and (b) show fast Fourier transform (FFT) plots (2048 points FFT) for a clock frequency of 50MHz and signal frequencies of 12 and 50kHz, respectively. Figure 6 (a) demonstrates an SNR of 97.5dB and SDR of 82.6dB. Figure 6 (b) demonstrates an SNR of 93.6 dB. Figure 6 (c) shows FFT plots (2048 points) for a clock frequency of 50MHz and a signal frequency of 92kHz. It demonstrates an SNR of 82.7dB. The total power consumed by the chip is 15.5mW. The total performance is presented in Table 2.

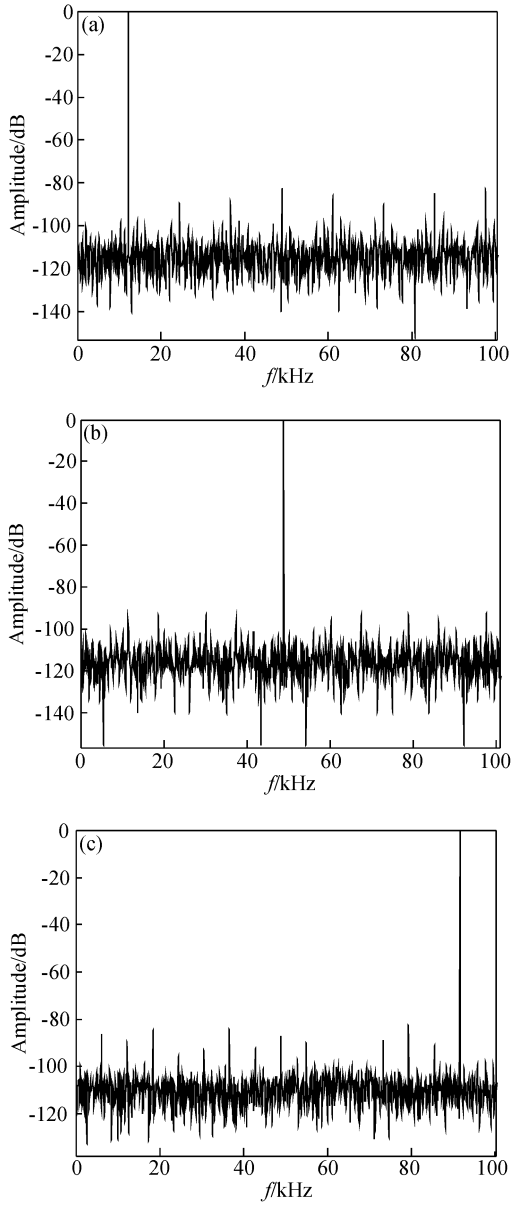

Fig. 6　(a) Measured spectrum (f_{in} = 12kHz, F_s = 50MHz); (b) Measured spectrum (f_{in} = 50kHz, F_s = 50MHz); (c) Measured spectrum (f_{in} = 92kHz, F_s = 50MHz)

Table 2　Performance summary

SNR: f_{in} = 12kHz, F_s = 50MHz	97.5dB
f_{in} = 50kHz, F_s = 50MHz	93.6dB
f_{in} = 92kHz, F_s = 50MHz	82.7dB
THD: f_{in} = 12kHz, F_s = 50MHz	82.6dB
Dynamic range	92dB
Sampling rate	50MHz
Oversampling ratio	256
Differential input range	1Vp-p
Bandwidth	96kHz
Power supply	1.8V
Power dissipation	9.8mW (Ana) + 5.7mW (Dig)
Area	2.68mm^2
Technology	0.18μm CMOS

6　Conclusion

An audio sigma-delta analog-digital converter with 16bit resolution, for a signal bandwidth of 96kHz, has been presented. The converter, implemented in a standard 0.18μm CMOS technology, integrates an analog modulator and a digital decimator in a single chip. Meanwhile, the die area, including the pad rings, is only 2.68mm^2. A chopper stabilization technique is employed to remove high $1/f$ noise. To reduce the deleterious effects of electronic noise generated by digital components, a noise management scheme has been employed. The decimation filter also uses a novel, low power, and area-efficient architecture.

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一种采用斩波稳零技术的 16 位,96kHz 带宽 Σ-Δ AD 转换器

曹 楹 任腾龙 洪志良†

(复旦大学专用集成电路与系统国家重点实验室,上海 201203)

摘要:介绍了一个 16 位精度 Σ-Δ 型模拟数字转换器.它由一个模拟的调制器和一个数字降采样滤波器组成.调制器采用了传统的单环两阶的结构,在第一阶调制器中采用了斩波稳零技术来消除电路的闪烁噪声.数字的降采样器包括多相梳状滤波器和波数字滤波器,功耗低,面积小.实验结果表明转换器获得了 92dB 的动态范围和 96kHz 的带宽.整个芯片由 0.18μm 六层金属 CMOS 工艺制造,芯片面积为 2.68mm^2,功率消耗仅为 15.5mW.

关键词:Σ-Δ 调制;斩波稳零技术;降采样器;多相分解;波数字滤波器;片上噪声

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† 通信作者.Email:zlhong@fudan.edu.cn

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