A New High Performance FM Transmitter*

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Abstract: A new FM transmitter is reported. It adopts a fractional-N PLL synthesizer to realize the FM modulator. An extra offset current has also been applied to eliminate the effects of the mismatch in CP. The chip is fabricated with CSMC 0.5μm DPTM CMOS technology. Experiments show that it achieves THD$\leqslant$0.08% and SNR$\geqslant$82dB, and the maximum outband emission energy $\leqslant -90$dBc/Hz. Furthermore, it also uses an auto frequency adjusting method to avoid tuning up the external inductances. All these merits are very suitable for FM transmission.

Key words: FM; fraction N frequency synthesizer; in-band phase noise
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1 Introduction

With the rapid development of digital TV and communication, the need has arisen to reduce the cost and power consumption of frequency synthesizers[1]. To keep costs down, an entire radio, including its digital baseband processor, analog baseband module, and RF circuits, would ideally be completely integrated into a single silicon die with a minimal count of external components. Thus a fully integrated high performance FM transmitter with cheap CMOS technology is in demand by both trend and market.

The advantages of digital FM modulation over traditional analogue techniques are well known[2]. It can solve problems such as over-modulation and poor THD, which occur in traditional analogue FM modulators. While most conventional digital FM modulations use direct digital synthesis (DDS) technology to synthesize FM signals[3,4], the DDS part usually works at more than eighty MHz, which dissipates much power and consumes large silicon area. Further more, an FM modulator requires a high frequency, high precision DAC component to realize the FM signal, making this method quite costly. This paper describes a new FM modulator based on a fractional N PLL frequency synthesizer. It is a closed loop FM modulator that achieves THD$\leqslant$0.08% and SNR$\geqslant$82dB, and its maximum outband emission energy is less than -90dBc/Hz. It is realized in CSMC 0.5μm DPTM technology.

2 Structure

A diagram of the new FM transmitter, which can adopt an analog or digital signal, is presented in Fig. 1. The analog signal is encoded from a

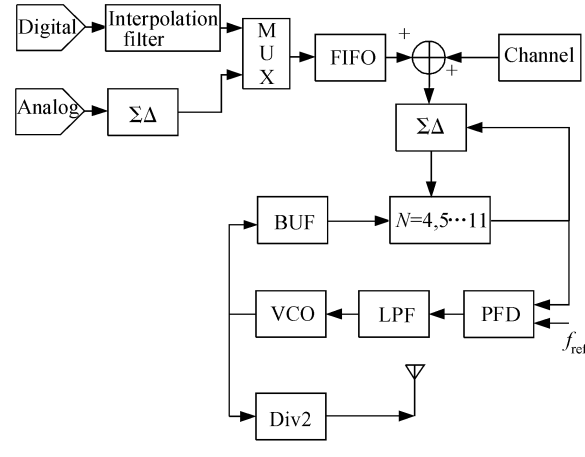

Fig. 1 Diagram of the digital FM modulator

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2-stage, 3-bit (Fig. 2 (a)) analog sigma-delta modulator with a 12.288MHz clock frequency, and then sent to a 3-stage, 3-bit (Fig. 2 (b)) digital modulator, altogether with the channel word, which controls the divider of the PLL. Sample and hold part has been inserted to increase the clock frequency to 12.288MHz, and the two depth FIFO has also been jointed to balance the digital modulator clock and the sample and hold clock, which is equal to the reference frequency of the PFD. Similarly, the digital signal can be interpolated and then sent to the FIFO. Owing to the new closed loop FM synthesizer, the THD can be decreased greatly, and the maximum frequency deviation can also be precisely set by the digital sigma-delta modulator. The maximum digital clock is just 12.288MHz, while the high speed and high precision DAC block is omitted, which saves much more power than the other digital FM methods[2~4].

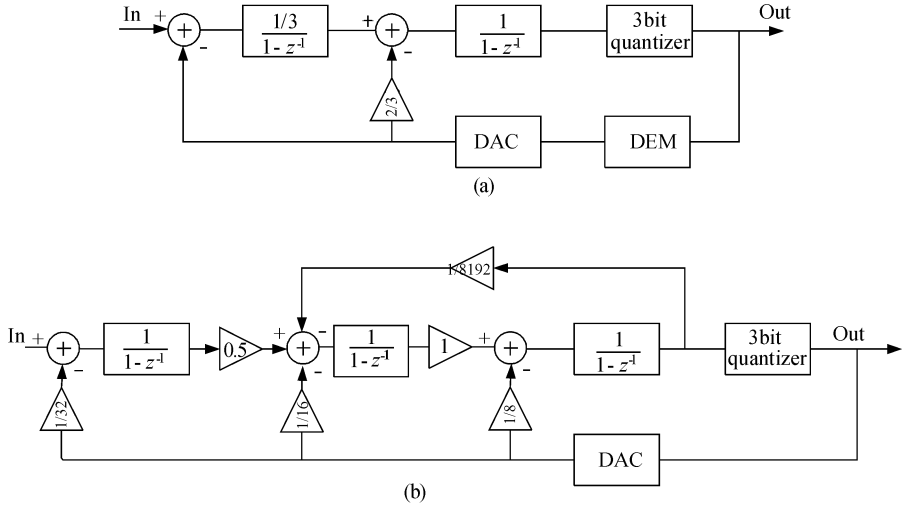

Fig. 2 (a) Two-stage three-bit analog modulator; (b) Three-stage three-bit digital modulator

3 Phase noise analysis and simulation

The final SNR of the FM signal is mainly determined by the in-band phase noise of the PLL, which comes from the flicker noise and thermal noise of the PFD/CP, VCO, divider, and quantization noise of the sigma delta modulator. To simplify calculating the SNR of the transmitter, all the noise is calculated as the input noise voltage of the VCO. Thus, the equivalent PFD noise is

$$S_{\Phi\mathrm{PFD}}(j\omega) = S_{\mathrm{PFD}}(j\omega)N^2\left|\frac{G(j\omega)}{1+G(j\omega)}\right|^2\Big/\left(\frac{K_{\mathrm{VCO}}}{j\omega}\right)^2 \tag{1}$$

where $G(j\omega)$ is the open loop transfer function of the PLL, N is the division ratio, K_{VCO} is the gain of the VCO, and $S_{\mathrm{FPD}}(j\omega)$ is given by Ref. [5].

$$S_{\mathrm{PFD}}(j\omega) = \left(1+\frac{\omega_c}{j\omega}\right)(\mathrm{FOM}+10\lg f_s) \tag{2}$$

Here ω_c is the corner frequency of the PFD flicker noise, f_s is the reference frequency, and FOM is a technical parameter, which is equal to $-213\sim 222\mathrm{dBc/Hz}$[5].

The equivalent CP noise is

$$S_{\Phi\mathrm{CP}}(j\omega) = S_{\mathrm{CP}}(j\omega)N^2\left|\frac{G(j\omega)}{1+G(j\omega)}\right|^2 t_{\mathrm{on}} f_{\mathrm{ref}}\Big/\left(\frac{K_{\mathrm{VCO}}}{j\omega}\right)^2 \tag{3}$$

where $S_{\mathrm{CP}}(j\omega)$ is the power spectral density of the thermal and flicker noise in the CP, and t_{on} is the charging or discharging time of the CP.

The equivalent VCO noise is

$$S_{\Phi\mathrm{VCO}}(j\omega) = S_{\mathrm{VCO}}(j\omega)N^2\left|\frac{1}{1+G(j\omega)}\right|^2\Big/\left(\frac{K_{\mathrm{VCO}}}{j\omega}\right)^2 \tag{4}$$

where $S_{\mathrm{VCO}}(j\omega)$ is the thermal and flicker noise spectral density of the VCO. The divider noise can be eliminated by re-sampling the divider's output signal with the VCO output signal[6], as depicted in Fig. 5. The equivalent quantization noise is a little more complicated since

$$f_d(t) = \frac{f_o(t)}{n+q(t)} \tag{5}$$

where $f_d(t)$ is the transient output frequency of the divider, $f_o(t)$ is the transient output frequency of the VCO, n is the fraction divider ratio, and $q(t)$ is the transient quantization noise. Thus the normalized instantaneous frequency departure $y(t)$ is given by

$$y(t) = \frac{1}{1+\frac{q(t)}{n}} - 1 = -\frac{q(t)}{n} + \left(\frac{q(t)}{n}\right)^2 - \left(\frac{q(t)}{n}\right)^3 \cdots\cdots \quad (6)$$

If the RMS spectral density of the quantization noise, $q(t)$, is labeled $Q(f)$, then the power spectral density of the normalized frequency deviations will be given by

$$S_y(f) = \left(-\frac{Q(f)}{n} + \left(\frac{Q(f)}{n}\right)^2 - \left(\frac{Q(f)}{n}\right)^3 + \cdots\right)^2 \quad (7)$$

The equivalent phase noise before the VCO is given by[5]

$$S_{\Phi q}(j\omega) = S_y(j\omega) N^2 \left|\frac{G(j\omega)}{1+G(j\omega)}\right|^2 \left(\frac{2\pi f_d}{j\omega}\right)^2 \Big/ \left(\frac{K_{VCO}}{j\omega}\right)^2 \quad (8)$$

From Eqs. (1, 3, 4, 8), enlarging the closed-loop bandwidth will increase both the phase noise caused by the PFD/CP and quantization, and decrease the effects of the phase noise of the VCO in the base band. From Eq. (7), it can be concluded that the high frequency quantization will be folded into the base band. Furthermore, the nonlinearity of the components, such as the mismatch of the CP, will also fold the high frequency quantization noise into the base band[7,8]. Simulation results are drawn with the solid line in Fig. 3. To cancel this effect, an offset current has been added into the CP, as shown in Fig. 4, since only the down transistor of the CP will discharge the charge of the capacitor in the locked state, which just induced an extra phase offset[9] between the reference input phase and the VCO output phase. For comparison, the SNR after adding the offset current has also been simulated and is labeled with the '+' line in Fig. 3. For simplicity, only the quantization noise is considered in Fig. 3, but in fact, since thermal and flicker noise of the transistors exist in each block of the PLL, the SNR will be decreased.

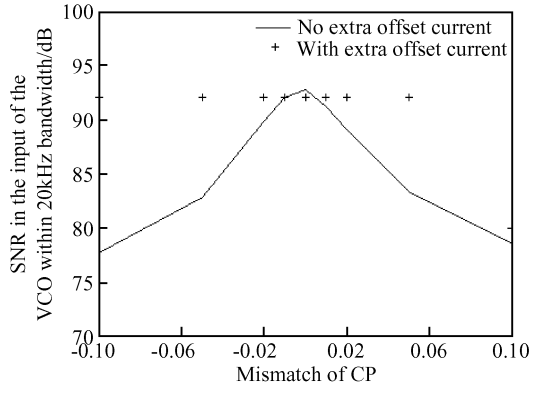

Fig. 3　Effects of the CP mismatch by folding the high frequency quantization noise

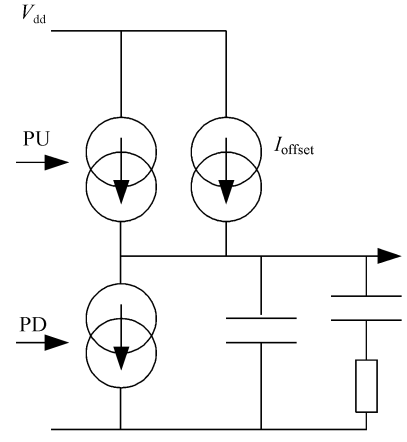

Fig. 4　Charge pump with an extra offset current

4　Circuits

A diagram of the whole FM transmitter is shown in Fig. 5. A controllable capacitor array is used to alleviate the precision of the external inductance. In the initial state, the PLL loop will be broken at point 'A' and the capacitor array is set with the minimum value. Then, a constant voltage which is equal to $V_{dd}/2$ is set at point 'A', while at the same time two counters are triggered by the output signal of the divider clock and the reference clock, respectively. By elaborate design, the divider clock will run much faster than the reference clock after 512 periods, and so the capacitor array will be enlarged to repeat the countering process till the rising edge of the two clocks are within one reference period after countering 512 periods. This means that the loop can be locked with the current capacitor and external inductance value, and it goes back to the closed loop function.

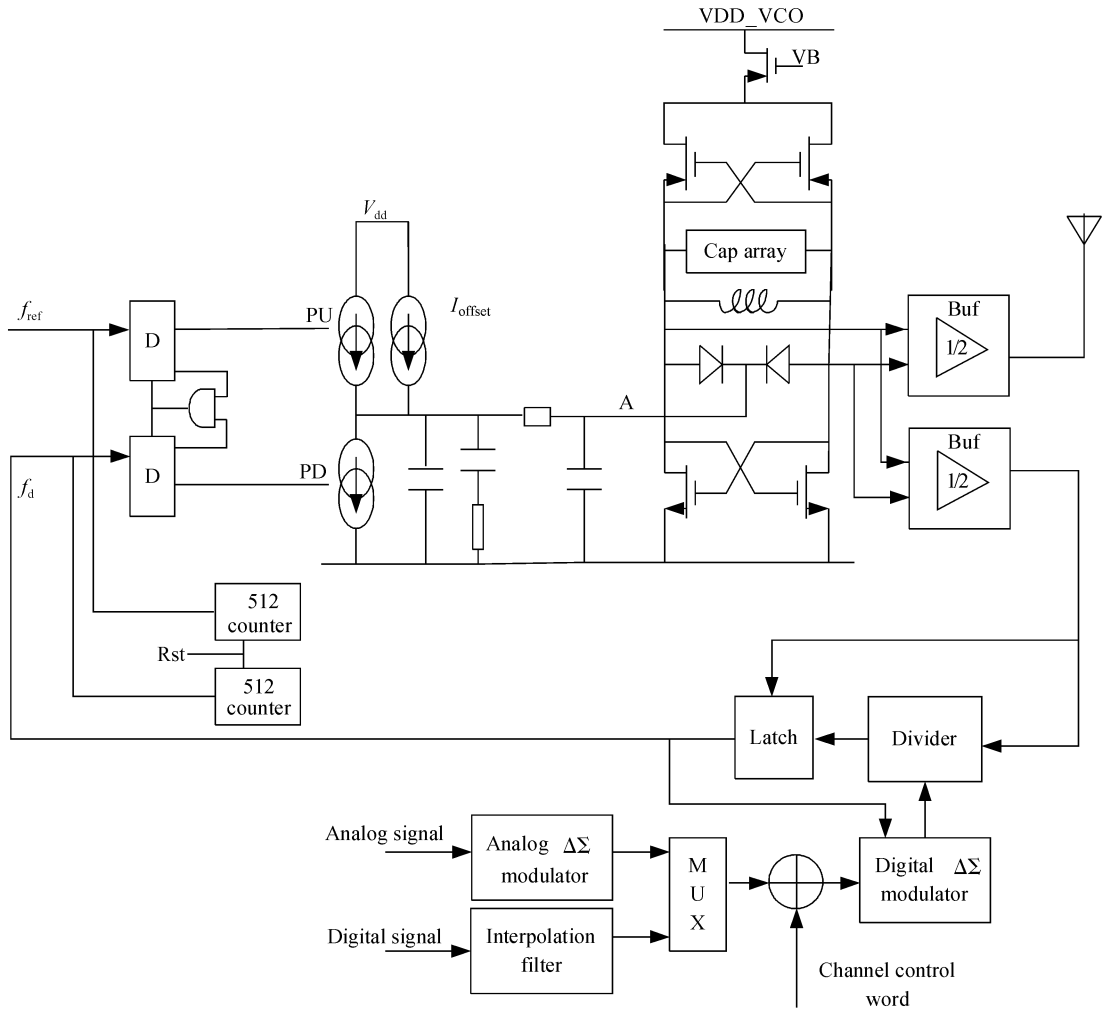

Fig. 5 Full diagram of the FM transmitter

5 Testing results

The proposed FM modulator has been implemented in CSMC 0.5μm DPTM CMOS technology. The active area of this chip is 2.2mm × 2.2mm, and the current dissipation is less than 15mA.

Experimental results show that the carry frequency can be auto-locked by the pointed channel word. The external inductance is 72nH, whereas it has been changed by ±10%, and the FM transmitter still can work correctly in the full radiating frequency range. Figure 6 (a) is the FM spectrum of the 1kHz sine stimulant signal, and Figure 6 (b) shows the phase noise of the FM transmitter measured by an Agilent spectrum analyzer 4396B. A high quality FM receiver Hitachi AM/FM tuner FT-M44 and a THD analyzer DF4120A were also used to demodulate the FM signal and test the SNR and THD. Experimental results are listed in Table 1. For comparison, some similar chips have also been added in Table 1 that adopt the traditional structure to modulate the FM signal.

6 Conclusion

A new digital modulator has been fabricated in 0.5μm DPTM technology, which adopts the closed loop synthesizing method to form an FM signal. Owing to the fractional N PLL frequency synthesizer, the maximum deviation frequency is precisely controlled and THD is decreased greatly. Furthermore, the new method saves much power and is much cheaper than conventional digital FM transmitters. To cancel the effects of the mismatch of the CP, an extra offset current has been jointed in the PLL. The experimental results show

that the SNR could be above 82dB, the THD is lower than 0.08%, and the maximum outband emission energy is below −90dBc/Hz.

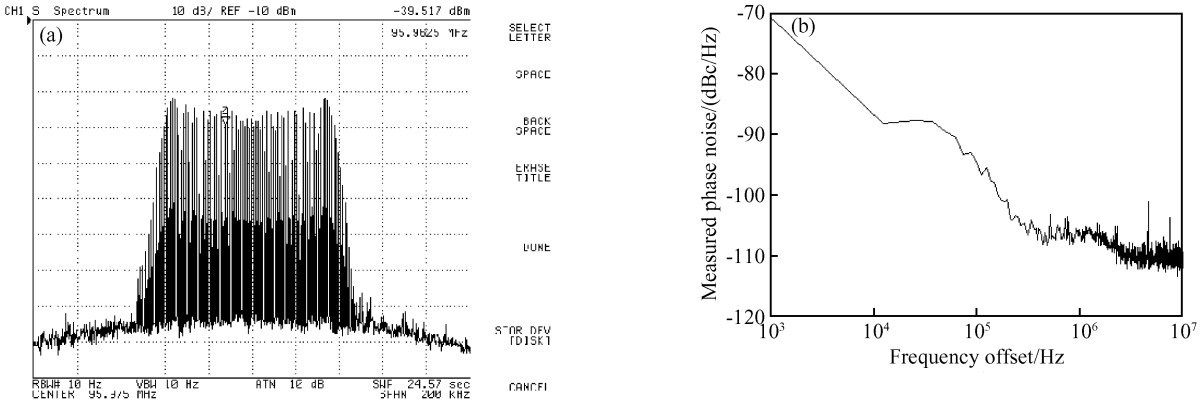

Fig. 6　(a) FM spectrum by the 1kHz sine stimulant signal measured by an Agilent spectrum analyzer 4396B; (b) Phase noise data of the FM transmitter measured by Agilent spectrum analyzer 4396B and plotted by Matlab

Table 1　Experiment results of the digital FM transmitter

Parameter	This chip	BH1417[10]	THG4649[11]
Technology	CMOS 0.5μm	Bipolar	0.35μm SiGe BiCMOS
SNR	≥82dB	55dB	70dB
THD	≤0.08% @1kHz, half of the maximum frequency deviation*	0.1%	0.5%
Open loop bandwidth	100kHz		
Maximum outband emission energy	≤−90dBc/Hz		
Radiating energy	3mW	1.3mW	13mW

* Limited by Hitachi FT-M44

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新型高性能调频发射机的研究*

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摘要：介绍了一种全新的 FM 调制器结构.该调制器基于小数分频锁相环技术，并在电荷泵单元中引入额外偏差电流消除电荷泵失配对带内噪声的影响.该芯片采用 CSMC 0.5μm DPTM CMOS 工艺，测试结果表明，其 SNR≥82dB，THD≤0.08，最大带外辐射能量低于－90dBc/Hz.此外，该芯片还采用自动频率调整的方法避免调节片外电感.该芯片的这些特点十分适合调频发射的要求.

关键词：调频；小数频率合成器；带内相位噪声

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