Design of an Analog Front End for Passive UHF RFID Transponder IC*

Chen Liying, Wu Shunhua, Mao Luhong†, and Hao Xianren

(*School of Electronic Information Engineering, Tianjin University, Tianjin 300072, China*)

Abstract: This paper introduces a high-performance analog front end for a passive UHF RFID transponder IC, which is compatible with the ISO/IEC 18000-6B standard, operating at the 915MHz ISM band with a total supply current consumption less than 8μA. There are no external components, except for the antenna. The passive IC's power supply is taken from the energy of the received RF electromagnetic field with the help of a Schottky diode rectifier. The RFID analog front end includes a local oscillator, clock generator, power on reset circuit, matching network and backscatter, rectifier, regulator, and AM demodulator. The IC, whose reading distance is more than 3m, is fabricated with a Chartered 0.35μm two-poly four-metal CMOS process with Schottky diodes and is EEPROM supported. The core size is 300μm×720μm.

Key words: RFID; passive transponder; analog front end; low power
PACC: 8630; 7280C; 7230
CLC number: TN402 **Document code**: A **Article ID**: 0253-4177(2007)05-0686-06

1 Introduction

Radio frequency identification (RFID) is becoming a hot topic, and applications for RFID are multiplying rapidly. RFID is an emerging technology used for object identification by radio waves. Some of the common fields of applications include supply chain management, automation toll collection systems, access to control buildings, airport baggage, and public transportation. The increasing applications require high volume, low cost, small size, and higher data rates. This paper presents an analog front end (AFE) of the long range, low power, passive UHF RFID transponder IC.

Several frequency ranges are commonly used in RFID technology. Inductive tags usually operate at around 125kHz or 13.56MHz[1] using a coil as an antenna. Because coupling is inductive, these transponders operate in the magnetic near field of the reader's coil antenna, and their reading range (maximum distance between the transponder and the reader) is typically limited to less than 1.2m, and the bandwidth in Europe and other regions is limited by regulations to a few kilohertz[2]. But operation at UHF (865～960MHz) or microwave (2.4GHz) frequencies allows longer reading distance, higher data rates, and smaller antenna sizes. There is a strong interest in UHF frequency band RFID transponders, especially for 865～960MHz and 2.4GHz ISM band. Also, UHF frequency bands used in RFID vary throughout the world. For example, in North and South America the center frequency is 915MHz, whereas Europe, the Middle East, and the Russian Federation mainly use 866MHz. Asia and Australia use frequencies within the band from 866 to 954MHz. Thereby, the whole bandwidth used in UHF RFID is from 865 to 960MHz[1,3].

This paper presents an AFE of a transponder with low power and long range. The technology is a 0.35μm two-poly four-metal CMOS process that supports EEPROM and Schottky diodes. The Schottky diodes, with low series resistance and low forward-voltage drop, allow for a higher conversion efficiency of the received RF input signal energy to DC supply power. The reading distance of the AFE is more than 3m with a supply current of about 8μA and an antenna gain of about 0 at 4W (36dBm) EIRP base-station transmission power, operating at 915MHz. The system architecture and the operation of the different building

* Project supported by the National High Technology Research and Development Program of China (No. 2006AA04A109)
† Corresponding author. Email: tju_rfid@163.com
Received 27 November 2006, revised manuscript received 28 December 2006

blocks are described, respectively. The experimental results are presented, and a conclusion is provided.

2 Architecture

A block diagram of the AFE is shown in Fig. 1. The individual blocks of this diagram will be described in detail in the following paragraphs. The antenna is the only external component of the AFE. It can provide low loss and be matched to the input impedance of the rectifier by the matching network. The rectifier converts the RF input signal power to a DC supply voltage. The regulator maintains the power supply at a certain level and limits the amplitude of the dc supply to protect the chip. The AM demodulator extracts the data that are embedded in the carrier waveforms. The backscatter fulfils the return data link by alternating the impedance of the AFE using a MOS varactor. The circuit of the power on reset (POR) generates the chip power on reset signal. Unlike the HF transponder, the clock in the UHF transponder can't be extracted directly from the carrier. The local oscillator and clock generation generate the system clock to the logic circuitry which isn't within the scope of this paper.

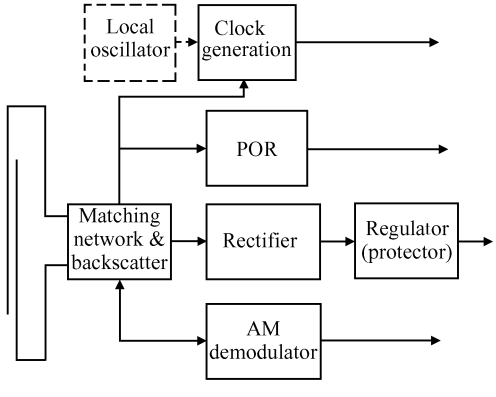

Fig. 1　Block diagram of the AFE

3 Circuit design

3.1 Rectifier and regulator

The rectifier is used to generate the DC power supply from the RF input signal power for the whole transponder chip. A schematic of the rectifier is shown in Fig. 2[4]. Schottky diodes with low series resistance and low junction capacitance are used, which allow for a higher conversion efficiency of the received RF input energy to DC power supply. For the RF signal, all the diodes are connected in parallel (or antiparallel) by the poly-poly capacitors. For DC, they are connected in series to allow a DC current to flow between nodes V_{DD} and V_{SS}. The voltage generated between them is approximately equal to[4]

$$V_{DD} = n(V_{p,RF} - V_{f,D})$$

where n is the number of diodes, $V_{p,RF}$ is the amplitude of the RF input signal, and $V_{f,D}$ is the forward voltage of the Schottky diodes, which is approximately 272mV at 7.88μA. The size of each stage poly-poly capacitor is about 1.4pF except for the last stage, which is larger than the others.

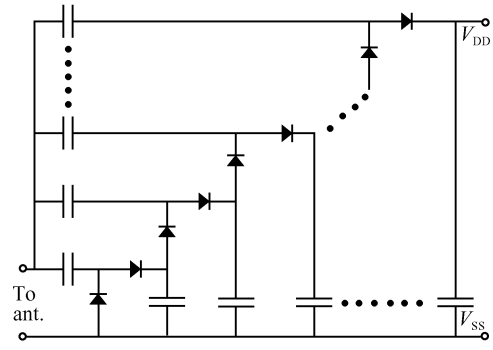

Fig. 2　Schematic of the rectifier circuit

The regulator holds the AFE output supply at a preferred value and provides a stable voltage to prevent the chip from breaking down with the amplitude of the RF input power varied at different physical locations. The structure of a proportional to absolute temperature (PTAT) voltage is used. Furthermore, the structure of the self-bias cascode is used to promote PSRR and reduce the current in order to depress the power dissipation. In addition, unlike conventional RFID tags, the low power voltage and current reference[5] is used with a low-power startup circuit[6], which completely turns off once the reference is started, and there is no dissipation during the typical operation state.

3.2 Matching network and backscatter

Unlike HF RFID tags at 13.56MHz, a dipole antenna is used in this UHF frequency band RFID

transponders[7]. Figure 3 shows the equivalent Spice circuits of the dipole antenna[8]. The antenna is modeled by the series resonant circuit, which consists of an inductance L_1, a capacitance C_1, a radiation resistance R_r, and a loss resistance R_l. The resistance R_l, which is 1MΩ, is used for Spice convergence. The capacitor C_2 is used to improve the performance of the antenna above the resonant frequency f_0. This circuit has its minimum impedance ($R_r + R_l$) at the resonant frequency f_0. A voltage source V_{rx} represents the received voltage due to external electromagnetic waves. The equivalent antenna impedance Z_a, resonant frequency f_0, and quality factor Q can be written as[8]

$$Z_a = (R_r + R_l)\left(1 + j\omega \frac{L}{R_r + R_l} - j\frac{1}{\omega(R_r + R_l)C_1}\right) \quad (1)$$

$$f_0 = \frac{1}{2\pi\sqrt{L_1 C_1}} \quad (2)$$

$$Q = \frac{\omega_0 L_1}{R_r + R_l} = \frac{1}{R_r + R_l}\sqrt{\frac{L_1}{C_1}} \quad (3)$$

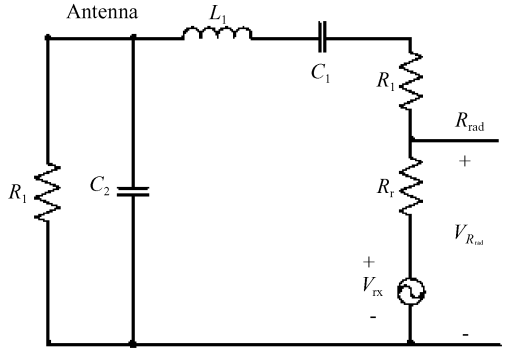

Fig. 3 Electrical equivalent of a half wavelength dipole antenna

To reduce the chip size and facilitate the integration, the equivalent inductance of the antenna is put into the L-type matching network. The conjugate match of the complex number requested is converted to match the input impendence of the AFE to 105Ω. By calculating, the input impendence of the AFE is approximately 105 − j406.6Ω.

The modulation is implemented by a backscatter approach[4]. By modulating the input impedance of the AFE, the electromagnetic wave backscattered by the antenna is modulated. The modulation of the imaginary of the transponder is easier to apply by modulating the capacitance rather than the inductance in CMOS process. By changing the capacitance of the MOS varactor, the Bi-state amplitude modulated backscatter is implemented. With the modulation, high power efficiency for DC supply voltage generation and high modulated backscatter power for the backward link are achieved simultaneously. The schematic of the backscatter modulation circuit is shown in Fig. 4.

3.3 AM demodulator

The demodulator is used to demodulate the input carrier signal by the forward link from the reader to the transponder. Figure 5 shows a block diagram of the demodulator. The envelope detector uses the same circuit as the rectifier to extract the envelope. The following low-pass filter is used to eliminate the carrier noise and power ripple, whose parameters are determined by the data rate. Then, the output data waveform is generated by the hysteresis comparator.

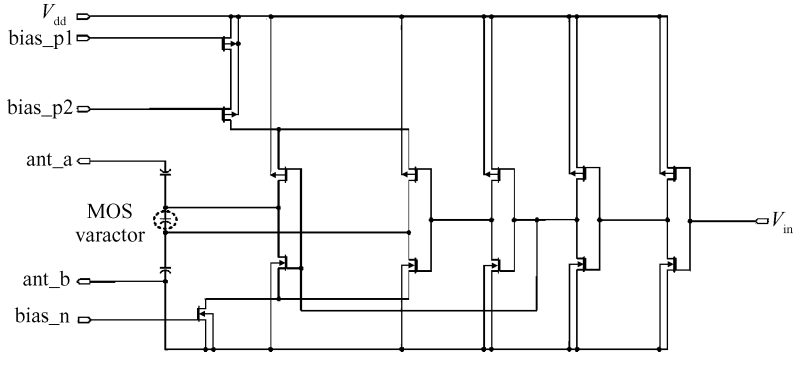

Fig. 4 Schematic of the backscatter circuit

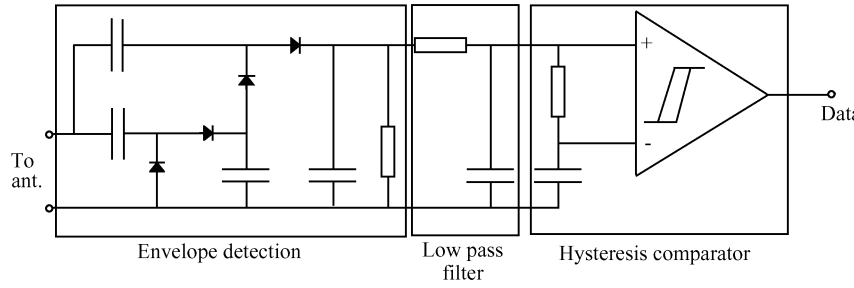

Fig. 5　Block diagram of the AM demodulator

3.4　POR

The POR circuit is used to reset the logic block when the transponder enters the electromagnetic field of the reader, and to prevent the logic block from error operations when the power supply descends to a certain level or when the transponder suddenly departs from the reader. In order to get a reset delay of 10μs, pairs of capacitors and inverters are employed.

3.5　Local oscillator and clock generation

Unlike an HF transponder, in a UHF transponder the clock can't be extracted directly from the antenna[7]. The local oscillator and clock generation have to be implemented in the UHF tag chip, which generate the system clock to the logic circuitry. The three stages of the ring oscillators are applied with the buffer shaping. The clock frequency is approximately 250kHz. It slightly varies with the temperature, supply voltage, and process parameter; however, the performance of the logic circuitry can't be affected.

4　Experimental results

This chip is fabricated using a Chartered 0.35μm two-poly four-metal CMOS process with Schottky diodes and EEPROM. Because the AFE is a part of the transponder, the core size of the AFE is 300mm × 720mm excluding pads. A die photograph is shown in Fig. 6. The different building blocks, such as local oscillator and clock generation, power on reset circuit, matching network and backscatter, rectifier, regulator, and AM demodulator, are labeled. In normal applications, only two bonding wires are required to connect the antenna to the transponder. The other bonding pads seen in Fig. 6 are used for testing purposes. The die photograph only shows the AFE of the transponder IC and a small part of the logic control circuitry. The rest not shown contains the other of the logic circuits and EEPROM. Figure 7 shows the testing results of the total AFE circuit, where Figure 7(a) shows the waveform of the input signal and Figure 7(b) shows the demodulated waveform by the AFE circuit as measured by an Agilent 54642A oscilloscope. With 4W EIRP at 915MHz and 0dB transponder antenna gain, the reading distance of the AFE is more than 3m.

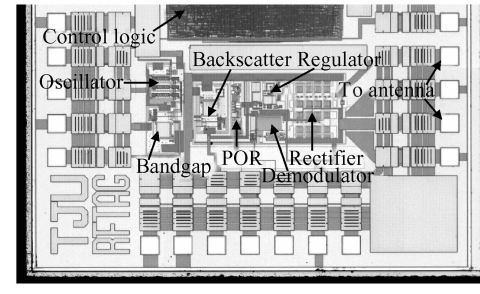

Fig. 6　Die photomicrograph of the AFE

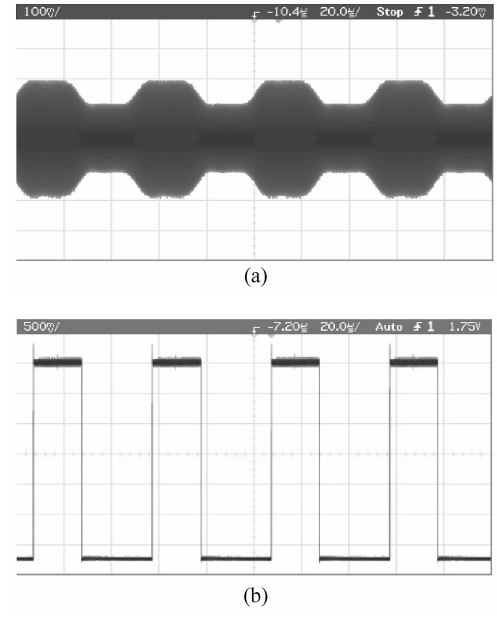

Fig. 7　Measured waveforms of the total AFE circuit

5 Conclusion

We have presented a high performance AFE for a passive UHF RFID transponder, which is compatible with the ISO/IEC 18000-6B standard, operating at the 915MHz ISM band with a total supply current consumption less than 8μA. Theoretical analysis used for the design optimization have been proposed. The whole chip has been fabricated with a Chartered 0.35μm two-poly four-metal CMOS process with Schottky diodes. Because the AFE is a part of the transponder, the core size of the AFE is 300mm×720mm excluding Pads. A novel impendence matching network, clock generation topology, voltage generation circuit, AM demodulator, and backscatter link were achieved with 4W (36dBm) EIRP base-station transmission power, operating at 915MHz. The reading distance of the AFE is more than 3m, and the measurement result meets the specification of the proposed system.

Acknowledgements The authors would like to thank Li Yanming and Wang Rui for their help in the process of design and measurements.

References

[1] Finkenzeller K. RFID handbook. 2nd ed. New York: John Wiley & Sons, 2003

[2] Hornby R M. RFID solutions for the express parcel and airline baggage industry. Proc IEE Colloq RFID Technology, 1999: 2/1-2/5

[3] EPC Global. Regulatory status for using RFID in the UHF spectrum 20.2006. http://www.epcglobalcanada.org/docs/RFIDatUHFRegulations20 050 720.pdf

[4] Karthaus U, Fischer M. Fully integrated passive UHF RFID transponder IC with 16.7mW minimum RF input power. IEEE J Solid-State Circuits, 2003, 38(10): 1602

[5] Ka N L, Mok P K T. A sub-1-V 15-ppm/℃ CMOS bandgap voltage reference without requiring low threshold voltage device. IEEE J Solid-State Circuits, 2002, 37(4): 526

[6] Boni A. Op-Amps and startup circuits for CMOS bandgap references with near 1-V supply. IEEE J Solid-State Circuits, 2002, 37(10): 1339

[7] Zhu Z. RFID analog front end design tutorial (version 0.0). Auto-ID Labs at University of Adelaide, 2004. http://autoidlabs.eleceng.adelaide.edu.au/Tutorial/RFIDanadesign.pdf

[8] Gerrits F M J, Hutter A A, Ayadi J, et al. Modeling and simulation of a dipole antenna for UWB applications using equivalent spice circuits. IEEE Antennas and Propagation Society International Symposium, 2004

[9] Abrial A, Bouvier J, Senn P, et al. A new contactless smartcard IC using an on-chip antenna and an asynchronous micro-controller. IEEE J Solid-State Circuits, 2001, 36(7): 1101

[10] Tikhov Y, Won J H. Impedance-matching arrangement for microwave transponder operating over plurality of bent installations of antenna. Electron Lett, 2004, 40: 574

[11] Ukkonen L, Sydänheimo L, Kivikoski M. Effects of metallic plate size on the performance of microstrip patch-type tag antennas for passive RFID. IEEE Antennas and Wireless Propagation Letters, 2005, 4: 410

[12] Ukkonen L, Sydänheimo L, Kivikoski M. A novel tag design using inverted-F antenna for radio frequency identification of metallic objects. Proc IEEE Sarnoff Symp Advances Wired and Wireless Communication, 2004: 91

[13] Ritamäki M, Ruhanen A, Kukko V, et al. Contactless radiation pattern measurement method for UHF RFID transponders. Electron Lett, 2005, 41: 723

[14] Kitayoshi H, Sawaya K. Development of a passive RFID-tag with 10-m reading distance under RCR STD-1 specification. Proc ISAP, 2004: 969

[15] Mun L N, Kin S L, Cole P H. Analysis of constrains in small UHF RFID tag design. IEEE International Symposium on Microwave, Antenna, Propagation and EMC Technologies for Wireless Communications Proceedings, 2005: 507

[16] Qi Z, Liang B. Design of microstrip antenna with broader bandwidth and beam. Proc IEEE Int Conf Antennas and Propagation, 2005, 3A: 617

无源 UHF RFID 电子标签模拟前端设计*

陈力颖　吴顺华　毛陆虹†　郝先人

（天津大学电子信息工程学院，天津　300072）

摘要：提出了一种符合 ISO/IEC 18000-6B 标准的高性能无源 UHF RFID 电子标签模拟前端，在 915MHz ISM 频带下工作时其电流小于 8μA.该模拟前端除天线外无外接元器件，通过肖特基二极管整流器从射频电磁场接收能量.该 RFID 模拟前端包括本地振荡器、时钟产生电路、复位电路、匹配网络和反向散射电路、整流器、稳压器以及 AM 解调器等.该芯片采用支持肖特基二极管和 EEPROM 的 Chartered 0.35μm 2P4M CMOS 工艺进行流片，读取距离大于 3m，芯片面积为 300μm×720μm.

关键词：RFID；无源电子标签；模拟前端；低功耗

PACC：8630；7280C；7230

中图分类号：TN402　　**文献标识码**：A　　**文章编号**：0253-4177(2007)05-0686-06

* 国家高技术研究发展计划资助项目(批准号:2006AA04A109)

† 通信作者.Email:tju_rfid@163.com

2006-11-27 收到，2006-12-28 定稿