A High Linearity CMOS DVB-S Front-End

Zhang Chi† and Wang Shufu

(*Beijing Embedded System Key Laboratory*, *Beijing University of Technology*, *Beijing* 100022, *China*)

Abstract: A direct conversion CMOS DVB-S front-end employs a T-configuration variable attenuator, a single-to-differential low noise amplifier, and a low noise mixer. By innovative use of the attenuator, the linearity handling ability of the system is dramatically improved. The system is designed and fabricated in SMIC 0.18μm RF CMOS technology. The measurement data show that the front-end provides a total of more than 30dB dynamic range and a noise figure of 5dB in the wide frequency signal band. The prototype front-end consumes only 10mA and achieves an IIP3 of +20dBm.

Key words: DVB-S; tuner; wide-band; high linearity
PACC: 2960C **EEACC**: 1205
CLC number: TN4 **Document code**: A **Article ID**: 0253-4177(2007)07-1036-05

1 Introduction

Digital signal broadcasting is a major application in consumer electronics. With the current trends in technology, the dominant demand from the market is for high bandwidth, low power, low cost, and a high level of integration solutions. These demands have partially been met by the development of state-of-art CMOS technology for improving the theoretical maximum device frequency. CMOS TV tuner designs, however, face great challenges due to the difficulty of linearity handling within a reasonable power dissipation level. This is because the received signal power in cable and wireless communication systems may vary by orders of magnitude and has not, unfortunately, scaled down with the advancement of technology.

The traditional method to control the input power level is to implement a variable gain amplifier (VGA) in a loop with automatic gain control (AGC). In essence, to approach the gain variation goal, one can tune the amplification ability (in the presence of effective transconductance g_m), the effective load, and the level of degeneration, tuning the transfer function of the negative feedback network. It also can be achieved by an attenuator preceding the RF front-end. Accordingly, there are forms of architectures that lend themselves conveniently to the realization of RF VGA. They are signal summing (by tuning the effective g_m)[1~4], source degeneration[5,6], variable loads[1,3,6,7], tunable feedback networks[2,3,6], and attenuators[5]. However, the first four methods may consume hundreds of milliwatts to meet the specification. For applications such as a handheld DVB receiver, it is extremely difficult to meet the requirement that power dissipation be below a few tens of milliwatts, which amounts to only milliamps from a 1.8V supply. Also, to increase the linearity, it is very popular to use an internal spiral inductor in the low supply voltage design[2,6]. However, the mandating of a number of reactive components requires a larger die area, especially for wideband (950~2150M for the DVB-S) and low frequency design (downward to 40M for the DVB-T), so it is not a generic solution and is not our concern.

On the other hand, attenuators with FET devices working in the resistive linear region are passive blocks and do not dissipate any power. Recent works have been reported that such an attenuator can be integrated into a single ship and is suitable for wideband RF applications[8,9]. Therefore, the purpose of this work is to test the usability of the mainstream CMOS process to implement the wideband, high linearity, low noise TV tuner with low power dissipation and validate it.

† Corresponding author. Email: ihczhang@msn.com
Received 20 December 2006, revised manuscript received 4 March 2007

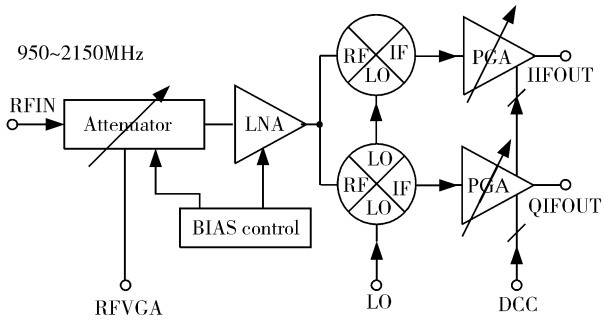

Fig. 1　Tuner chip block diagram

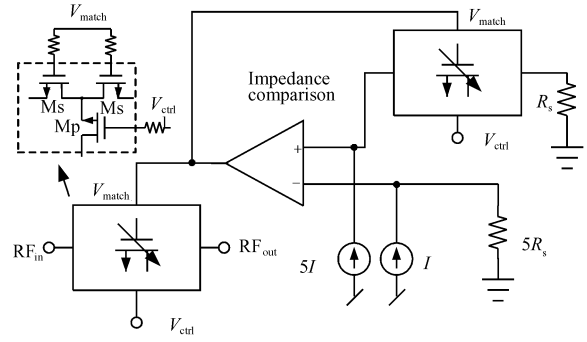

Fig. 2　Attenuator diagram and the control circuitry

2　System architecture

The receiver front-end architecture shown in Fig. 1 is based on a wideband front-end and an output driver for DC offset cancellation and testing. The variable gain attenuator first processes the RF band, which is from 950 to 2150MHz. Then, after being amplified by a fixed gain low noise amplifier (LNA) with single-to-differential conversion, the signal is down-converted to the baseband signal by a complex I/Q mixer. The channel is selected by the LO source. All the signal paths are differential after the LNA, although the diagram is single-ended for simplicity.

3　Circuit description

3.1　T-network attenuator with dynamic matching control

The attenuator not only controls the input signal power, but also provides impedance matching. There are many types of attenuators. The most commonly used types are the passive T-configuration[8,10], bridged T-configuration and the π-configuration[9], which are designed using FET devices working in the triode region. Figure 2 shows the realization of the attenuator with dynamic matching feedback control. It consists of a traditional T-configuration network, a master feedback loop to control the impedance matching, and controlled voltage to vary the gain factor. The key points of merit of an attenuator are minimum insertion loss and power handling capability as measured by the power 1dB compression point. According to these, we chose the simple T-configuration for the reasons below:

(1) The minimum insertion loss can be achieved by setting the serial transistor Ms to a large size. Research has shown[11] that the on resistance is at a feasible level (2～3Ω) for current technology when matching 50 or 75Ω. More importantly, the block must achieve the minimum NF across the entire wideband.

(2) According to its passive property, high linearity can be achieved without any extra power penalty.

(3) No additional control circuits are needed for the dB linear control for the T-configuration other than the π and the bridged-T. This is because the scaling factor is nearly proportional to the value of the shunt resistor and the resistance is inversely proportional to the control voltage.

Under all process corners, the T-network needs to maintain the input S_{11} matching and output S_{22} matching. This is controlled by the impedance comparison concept illustrated in Fig. 2. When the voltage V_{ctrl} varies, the replica servo circuit dynamically controls the matching condition of the T-network, with the result that S_{11} and S_{22} both meet the matching requirement under all V_{ctrl} values and through the entire RF band. Simulations with SpectreRF show that the matching condition will not change due to the process, voltage supply, or temperature (it is PVT independent). The results in Fig. 3 show that the attenuator can achieve a minimum assertion loss of 0.7 to 1dB in the signal band of 950～2150MHz, and the minimum attenuation gain is 33dB in the matching condition.

3.2　Wideband LNA design

The LNA is shown in Fig. 4. The purpose of the LNA in the TV receiver is to provide wideband input matching and amplification as well.

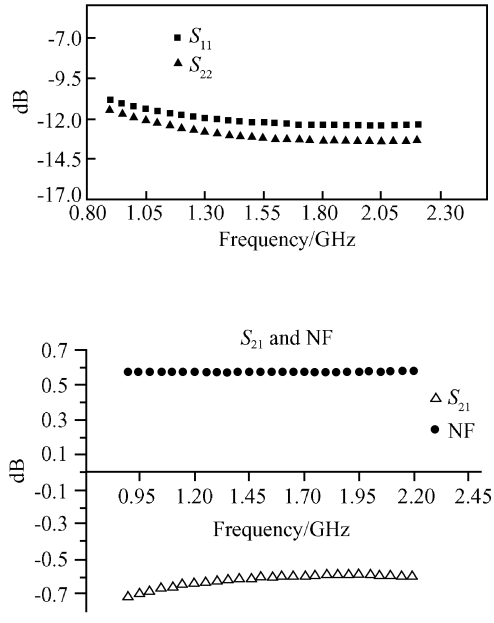

Fig. 3 T-network performance results

The LNA is a wide-band amplifier and provides single-ended to differential conversion via the common-source device M1 and the capacitor C_1. The usage of the single-to-differential conversion scheme is due to the TV tuner's single-ended input. This conversion can be achieved in many ways. Besides the off-chip balun approach[4], which is not discussed in this work due to its large area and narrow band nature, they are based on the voltage latency effect of the capacitor[1] and the tail current division effect[6]. We chose this capacitor solution architecture for its power saving advantages and low noise degradation properties. The resistive shunt-feedback provides good wideband impedance matching and flat gain response[12,13]. Therefore, no external matching networks are needed to achieve the wideband 75Ω input impedance. The design procedure is as follows: the proposed LNA is first optimized at 1.5GHz by selecting the width of common source transistor and the bias condition[14]. Then, with feedback resistor R_f, which tends to be a few hundred ohms, the bandwidth extends to cover 850MHz～2.5GHz. The LNA provides a low noise figure of 3dB and a voltage gain of 18dB and consumes only about 6mA.

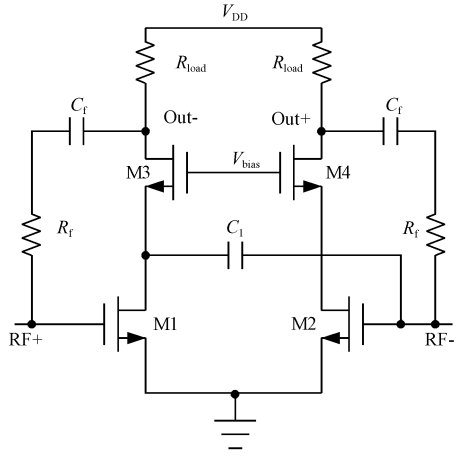

Fig. 4 LNA schematic

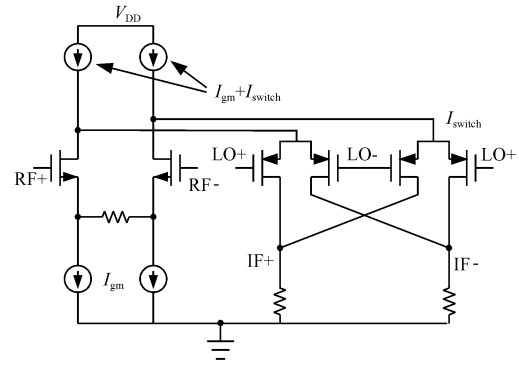

Fig. 5 Down-mixer schematic

3.3 Down-mixer design

The traditional current-folded, double-balanced Gilbert mixer shown in Fig. 5 is used for I/Q down conversion. Using the pre-attenuator technique, linearity is not so stringent, and the noise becomes the main consideration. For the purpose of noise reduction, we propose the current splitting scheme: We supply a large current to the transconductance stage, while a smaller current is injected into the switch quad network. This scheme not only addresses the conversion gain issue, but also reduces the flicker noise pulse. The four pMOS switches required must be wide enough to consume minimal voltage headroom while allowing a bandwidth greater than 50MHz at the output without overloading the LO buffer. According to the direct conversion architecture, there are time-invariant DC offset problems, especially through bond wire coupling for the LO provided externally. Therefore, a DC-offset servo loop is needed to control the mixer outputs for eliminating the DC-offset in order not to saturate the subsequent stages. Further linearity improvement is achieved by the source degeneration.

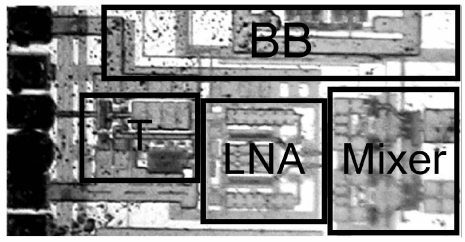

Fig. 6　Chip photograph

The down-mixer needs a power level of about 0dBm from local oscillator. Simulations indicate that the mixer displays an NF of 8dB and a voltage conversion of 10dB while drawing 4mA from the supply. The IIP3 of the mixer is 20dBm.

4　Chip implementation and measurement results

Besides the attenuator, the LNA, and the mixer, the prototype also includes a baseband variable amplifier, which can switch gain between 0 and 12dB. The baseband amplifier also has the function to drive the output load (up to 5pF capacitor with 2kΩ resistor in parallel) and consumes 2mA current.

The designed tuner front-end is fabricated in a 0.18μm 1P5M CMOS process at SMIC and occupies a die area of only 0.21mm^2 (300μm × 700μm). The simulator is SpectreRF from Cadence and the model is BSIM3V3.2. A die photograph is shown in Fig. 6.

The die was housed in QFN56, and is tested on two-layer FR4 PCB substrate. The input reflection coefficient was tested by means of an Agilent 5071B network analyzer. The $S_{11} < -10$dB is met throughout the entire signal band.

At the receiver output, a high-speed low-distortion differential amplifier (MAX4146) was used to convert the differential IF output signal to a single-ended format, driving the measurement equipment 50Ω input ports, and to raise the front-end output noise above the sensitivity level of the E4440A spectrum analyzer which is used to capture its frequency content. The NF is 4.8dB with the $1/f$ corner at 0.8MHz. The two-tone testing by E4440A shows that the IIP3 of the receiver will be as high as 20dBm in the low gain mode. A summary of the most relevant measurements and a comparison with the state of the art is reported, and it meets all the specifications and is suitable for application as a DVB-S tuner. The data also show that the simulation results depicted by SpectreRF are a little different from the measurement results. We believe that the simulation does not consider the board level insertion loss, and the device model may not be accurate enough, especially the noise model of flicker noise.

5　Conclusion

This paper has demonstrated that an innovation technique for using a resistor-based T-network attenuator can provide high linearity up to 20dBm in the low gain mode, low insertion loss down to 0.7dB, and wide-band input matching to cover the band from 950MHz to 2.1GHz.

Table 1　Testing results and requirements

Parameter	Simulated	Measured	Required
S_{11}/dB	<-16	<-12	<-10
Noise figure/dB	4.1	<5	<6
Voltage gain/dB	−5～40	−5～40	−5～35
Linearity (IIP3)/dBm	20	20	15

References

[1] Connell L, Hollenbeck N, Bushman M, et al. A CMOS broadband tuner IC. ISSCC, 2002

[2] Kim B E, Kim S Y, Lee T J, et al. A CMOS single-chip direct conversion satellite receiver for digital broadcasting system. Symposium on VLSI Circuits Digest of Technical Papers, 2002: 238

[3] Heng C H, Gupta M, Lee S H, et al. A CMOS TV tuner/demodulator IC with digital image rejection. IEEE J Solid-State Circuits, 2005, 40: 2525

[4] Antoine P, Bauser P, Beaulaton H, et al. A direct-conversion receiver for DVB-H. IEEE J Solid-State Circuits, 2005, 40: 2536

[5] Nagashima T, Ideno K, Yamamoto A, et al. A 0.95—1.8GHz GaAs tuner for direct broadcast satellite reception. ISSCC, 1990

[6] Kim B E, Yoon H M, Cho Y H, et al. A 9dBm IIP3 direct-conversion satellite broadband tuner-demodulator SOC. ISSCC, 2003

[7] Dawkins M, Payne A, Cowley N. A single-chip tuner for DVB-T. IEEE J Solid-State Circuits, 2003, 38: 1307

[8] Dogan H, Meyer R G, Niknejad A M. A DC-2.5GHz wide dynamic-range attenuator in 0.13μm CMOS technology. Digest of Technical Papers of Symposium on VLSI Circuits, 2005: 90

[9] Dogan H, Meyer R G, Niknejad A M. A DC-10GHz linear-in-dB attenuator in 0.13μm CMOS technology. Proceedings of the IEEE Custom Integrated Circuits Conference, 2004: 609

[10] Lefebvre B, Bessemoulin A. High dynamic range, triple gate-

based compact DC-40GHz variable attenuator MMIC for Ka-band variable gain amplifier ICs. IEEE 25th Annual Technical Digest of Gallium Arsenide Integrated Circuit (GaAs IC) Symposium,2003:135

[11] Huang F J, Kenneth O. A 0.5-μm CMOS T/R switch for 900-MHz wireless applications. IEEE J Solid-State Circuits, 2001,36(3):486

[12] Razavi B. Design of analog CMOS integrated circuits. New York:McGraw-Hill,2001

[13] Kim C W, Kang M S, Anh P T, et al. An ultra-wideband CMOS low noise amplifier for 3—5-GHz UWB system. IEEE J Solid-State Circuits,2005,40(2):544

[14] Lee T H. The design of CMOS radio-frequency integrated circuits. UK,Cambridge:Cambridge University Press,1998

一个高线性度的 CMOS DVB-S 前端芯片

张 弛† 王树甫

(北京工业大学北京嵌入式系统重点实验室，北京 100022)

摘要：提出了基于 CMOS 工艺的直接频率变换的 DVB-S 射频前端电路设计.设计采用了 T 型匹配网络的可变衰减器、具有单端到双端变换功能的低噪声放大器以及低噪声混频器.通过使用衰减器,系统处理线性度的能力得到很大的提高.设计和流片基于 SMIC 0.18μm CMOS 工艺.测试结果表明,该设计能够达到超过 30dB 的动态范围,噪声系数小于 3dB,消耗电流为 10mA.在低增益情况下,具有 +20dBm 的输入三阶交调能力.

关键词：卫星电视广播系统；调谐器；宽带；高线性度

PACC：2960C **EEACC**：1205

中图分类号：TN4 **文献标识码**：A **文章编号**：0253-4177(2007)07-1036-05

† 通信作者.Email:ihczhang@msn.com

2006-12-20 收到,2007-03-04 定稿