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A New Empirical Large Signal Model of 4H-SiC MESFETs for the Nonlinear Analysis*

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Abstract: A new comprehensive empirical large signal model for 4H-SiC MESFETs is proposed. An enhanced drain current model, along with an improved charge conservation capacitance model, is presented by the improvement of the channel length modulation and the hyperbolic tangent function coefficient based on the Materka model. The Levenberg-Marquardt method is used to optimize the parameter extraction. A comparison of simulation results with experimental data is made, and good agreements of *I-V* curves, P_{out} (output power), PAE (power added efficiency), and gain at the bias of $V_{DS} = 20V$, $I_{DS} = 80mA$ as well as the operational frequency of 1.8GHz are obtained.

Key words: 4H-SiC MESFET; large signal; empirical model; Levenberg-Marquardt method
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1 Introduction

Silicon carbide has recently received increasing attention for the unique properties of wide bandgap (3.2eV), high conductivity (4.9W/(cm·K)), high saturated electron drift velocity (2×10^7cm/s), and high breakdown electric field ($(2 \sim 4) \times 10^6$V/cm). 4H-SiC MESFETs are considered to be potentially important devices for the next generation in applications of high power, high frequency, and high efficiency RF & MW electric circuits[1~3]. The increasing demands of CAD of MMIC and power RF & MW electric circuits for 4H-SiC MESFETs provide the impetus for accurate and reliable large signal modeling.

Much effort has been made on the large signal modeling of 4H-SiC MESFETs. The analytical model[4~8] and numerical model[9] have been used to investigate devices' operating principles and to evaluate their performance. But the accuracy is limited and usually CAD tools cannot be embedded directly in most cases. The table-based model[10] has the advantages of rapid and accurate modeling, but it has the limits of interpolation function and the scope of parameters extracted, and also requires enough measured data to obtain high accuracy.

The empirical and semi-empirical model is one of the best choices of commercial RF & MW circuit CAD tools for its advantages of simple expression, high accuracy and ease of implementation into CAD tools. Sayed[11] and Manohar[12] have developed a 4H-SiC MESFET empirical large signal model, but some incomprehensible parameters in their models limit their applications. In addition, an accurate and robust model is needed to satisfy the increasing demands for the design of radio frequency integrated circuits (RFIC's).

In this study, an accurate and robust empirical large signal model for 4H-SiC MESFETs is proposed. In this model, the drain current is improved by the modification of the channel length modulation and the saturation voltage coefficient based on the Materka model, and a new charge conservation capacitance model is also developed. Moreover, the validity of the present model is made by the comparison of simulated results with measured data.

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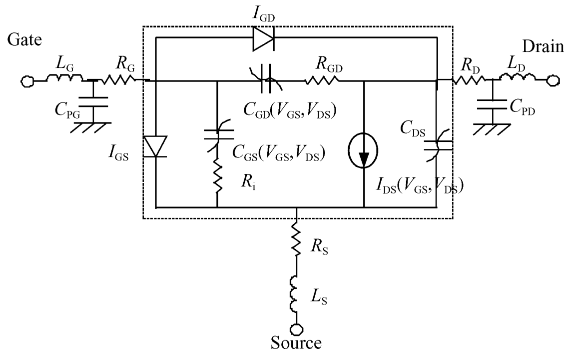

Fig. 1 4H-SiC MESFET large-signal equivalent circuit

2 Model description

The large-signal equivalent circuit of a 4H-SiC MESFET is shown in Fig. 1. The circuit includes two parts including the external or parasitic elements that are independent of the biasing conditions and the intrinsic elements (I_{DS}, I_{GD}, I_{GS}, C_{GD}, C_{GS}, C_{DS} and R_i) within the dotted line box that are dependent on the biasing conditions. The parasitic elements can be obtained by the "cold FET" method[13,14], and the diode current (I_{GS}, I_{GD}) parameters by the Schottky junction current model. The drain-source capacitance C_{DS} is usually modeled by a linear element as 2 ~ 3 times C_{DSP}[17]. Therefore, the critical elements in the large signal equivalent circuit are drain current I_{DS}, gate-drain, and gate-source capacitance.

2.1 Drain current model

The operational mode of a 4H-SiC MESFET is different from that of a GaAs MESFET due to its physical characteristics of high thermal conductivity, high breakdown voltage, high saturated electron drift velocity, and incomplete ionization of dopants in 4H-SiC. Therefore, an improved empirical DC drain current model for a 4H-SiC MESFET is given by

$$I_{DS} = I_{DSS0} \times \left(1 - \frac{V_{GS}}{V_T}\right)^Q \times [1 + \lambda(V_{GS}) V_{DS}] \times \tanh[\alpha(V_{GS}) V_{DS}], \quad V_{GS} > V_T \tag{1a}$$

$$I_{DS} = 0, \quad V_{GS} \leqslant V_T \tag{1b}$$

where

$$\lambda(V_{GS}) = \lambda_0 + C_1 V_{GS} \tag{2}$$

$$\alpha(V_{GS}) = \alpha_0 + C_2 V_{GS} \tag{3}$$

The undetermined coefficients in this new model are: I_{DSS0}, linearly extrapolative drain-source saturation current value at $V_{GS} = 0$; V_T, threshold voltage; Q, fitting parameter; λ_0, channel length modulation coefficient at $V_{GS} = 0$; α_0, saturation voltage coefficient at $V_{GS} = 0$; C_1, C_2, fitting parameters.

Table 1 Differences of parameters between present model and Materka model

Parameter	Present model	Materka model[10]
V_T	Constant	Associated with V_{DS}
λ	Changes with gate applied voltage V_{GS}	Independent on V_{GS}
α	Changes with gate applied voltage V_{GS}	Independent on V_{GS}
Q	Undetermined coefficient	Kept constant at 2

The form of this presented DC drain current model is based on the Materka model and Ref. [12]. The differences between the present model and the Materka model are listed in Table 1.

As can be seen from the new drain current model, the following features can be observed:

(1) Initialization is easily obtained due to the fact that the new model has only 6 undetermined coefficients, less than the 7 of the Manohar model and 10 of the Sayed model, and the parameters have their physical meaning which make for easy initialization with the assistance of analytical model[12];

(2) Robustness and easier convergence are expected since there are no exponential undetermined coefficients.

2.2 Capacitance model

As investigated before, the capacitance model with the expression of Q-V (charge-voltage) can reduce the errors produced by the conventional approach of C-V (capacitance-voltage) by avoiding charge nonconservation[17~19]. Also, consistency of large- and small-signal models requires that the condition of charge conservation be satisfied. Therefore, the form of Q-V is generally used with respect to C-V to use the same equivalent circuit as the small- and large-signal models. Here an improved charge conversation capacitance model is developed. The charge expressions are given by

$$Q_{GS} = C_{GS0} V_{GS} + \frac{C_f \lg\{\cosh[S_g(V_{GS} - D_C \tanh(D_K V_{GD})) + K]\}}{S_g} \tag{4}$$

$$Q_{GD} = C_{GD0} \frac{[1-(P_{21}-P_{22}V_{GS})V_{GD}]^{-M}}{(m-1)(a+bV_{GS})} \quad (5)$$

where C_{GS0} is the zero biased gate-source capacitance; C_f, S_g, D_C, D_K, and K are the fitting parameters related to gate-source capacitance; C_{GD0} is the zero biased gate-drain capacitance; and P_{21}, P_{22}, and M are the fitting parameters related to gate-drain capacitance.

The gate-source charge expression (4) is from Ref.[20], and a modification is made by adding the coefficient K to enhance the accuracy of Q_{GS}, which is different from the Angelov model[21] but similar to the model presented in Ref.[22]. The additional coefficient K can describe the variation of the nonlinear characteristics of Q_{GS} with drain terminal voltage accurately without altering the properties of C_{GS} to Q_{GS}.

The gate-drain charge model based on the Statz model[19] is improved by the modification of $\frac{1}{V_{bi}}$ as $P_{21}-P_{22}V_{GS}$ to describe the variation of C_{GD} with applied gate voltage.

From Eqs.(4) and (5), ignoring cross effects of gate-drain voltage V_{GD} on Q_{GS} during the differential coefficient, the *C-V* expressions of capacitances are given as

$$C_{GS} = \frac{\partial Q_{GS}}{\partial V_{GS}} = C_{GS0} + C_f \tanh[S_g(V_{GS} - D_C \tanh(D_K V_{GD})) + K] \quad (6)$$

$$C_{GD} = \frac{\partial Q_{GD}}{\partial V_{GD}} = C_{GD0}[1-(P_{21}+P_{22}V_{GS})V_{GD}]^{-M} \quad (7)$$

3 Optimization strategy

The least-square method is used in the parameter extraction. The merit function is minimized as follows in performing nonlinear regression.

$$\chi^2(\alpha) = \sum_{j=1}^{N_1}\left\{\sum_{i=1}^{N_2}\left[\frac{y_{ij}-y(x_{ij},a)}{\sigma_{ij}}\right]^2\right\} \quad (8)$$

where y_{ij}, $y(x_{ij},a)$ are the calculated and measured data respectively, and σ_{ij} is the standard deviation of the ijth point.

To obtain the minimized merit function, the Levenberg-Marquardt method is used in the optimization. This method overcomes the problem of instability in the iteration, which will be generated if the GAUSS-NEWTON method is used for the odd derivative matrix once a linear correlation in the derivative matrix appears[23].

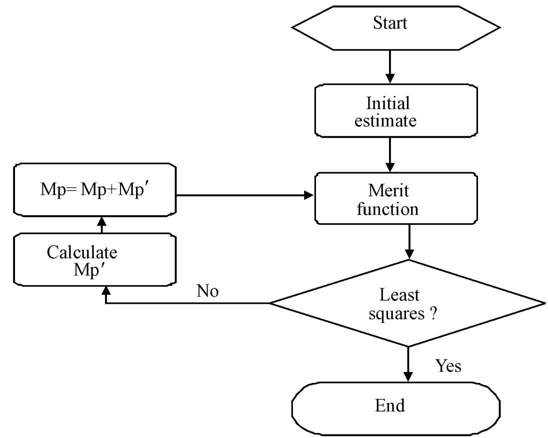

Fig. 2　Flow chart of optimization

The flow chart of optimization is shown in Fig. 2, where M_P is the undetermined parameter matrix and M_P' is the derivative matrix formed by the Levenberg-Marquardt method.

4 Model verification and discussion

The verification is made through embedding the present model into advanced design system (ADS) developed by Agilent Corporation. The parasitic elements are obtained by the “cold FET” method, the capacitances can be extracted from high frequency small signal parameter extraction, and the current elements from the DC are measured with pulsed *I-V*.

The measured data are obtained from Ref.[10]. The structure of the 4H-SiC MESFET is an n-type channel with an asymmetrical gate structure, with a 0.25μm depth of the n-type channel doped around $1.4\times10^{17}cm^{-3}$, 0.2μm thickness of n^+-type contact layer doped around $7\times10^{18}cm^{-3}$, p-type buffer layer doped about $5\times10^{15}cm^{-3}$, the channel length and width of the gate are 0.7μm and 2mm, respectively (multiple gate fingers), and the spaces of the gate/source and gate/drain are about 0.5 and 3μm, respectively. The initial guesses for iteration can be made with the drain current quasi-analytical model[12] and analytical capacitance model[24]. This will accelerate the convergence and reduce the cases of “pseudo-convergence” or “divergence” effectively. Parasitic elements cited from Ref.[10] are listed in Table 2. The extracted parameters of the drain current and capacitance model are listed in

Table 2 Values of extrinsic elements for present 4H-SiC MESFET[10]

R_S/Ω	R_G/Ω	R_D/Ω	L_S/pH	L_G/pH	L_D/pH	C_{PG}/fF	C_{PD}/fF
5	12.5	9	440	498	205.5	374	520

Table 3 Extracted parameters of I_{DS}, C_{GD}, C_{GS} in present model using Levenberg-Marquardt method

I_{DSS0}/mA	V_T/V	Q	λ_0/V^{-1}	α_0/V^{-1}	C_1/V^{-1}	C_2/V^{-1}
242	-11.5	1.99	0.021	0.350	0.0038	0.100
C_{GD0}/pF	P_{21}/V^{-1}	P_{12}/V^{-1}	M			
0.5	0.056	-0.002	2.52			
C_{GS0}/pF	C_f/pF	S_g/V^{-1}	D_K/V^{-1}	K/V		
0.417	0.430	0.14	0.001	3.57		

Tables 3 and 4, respectively, where the Levenberg-Marquardt method is used to obtain the optimization in the parameter extraction. The reverse saturation current of the Schottky gate current model is assumed to be 1mA and the ideality factor to be 2. As can be seen from Tables 3, the main extracted parameters I_{DSS0}, V_T, C_{GS0}, C_f, and C_{GD0} are all proposed for a quantitative view, making the present model robust and easy to comprehend. It should be of practical significance for the application of the present model to CAD tools.

Figure 3 shows a comparison of simulated results of the DC *I-V* curves of the 4H-SiC MESFET with measured data, and a very good agreement is observed. Figures 4 and 5 show a comparison of the simulated results of C_{GS} and C_{GD} with measured data, and good agreements are also achieved, especially in the high applied drain voltage range in which the device operates mostly. Thus the error of gate-source and gate-drain capacitance from the present model will have an acceptable influence on the high frequency characteristics of the MESFET.

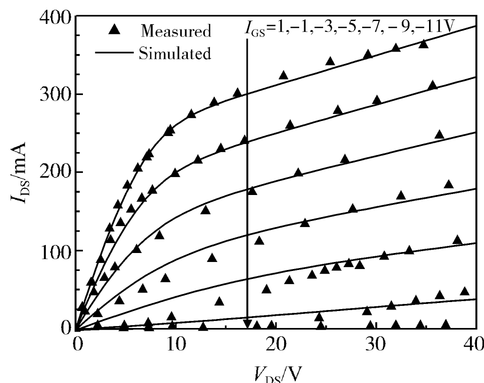

Fig. 3 Measured (symbol) and simulated (solid lines) DC *I-V* characteristics of 4H-SiC MESFET

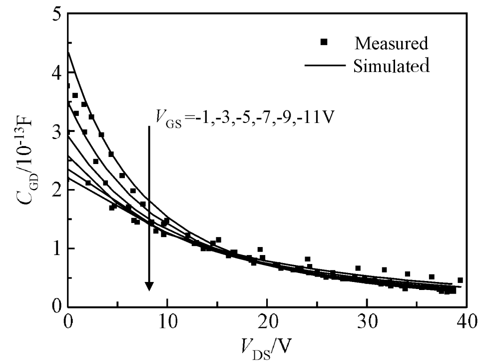

Fig. 4 Simulated and measured results of C_{GD} when static bias: V_{DS} = 19V, I_{DS} = 76mA, f = 0.9～6GHz

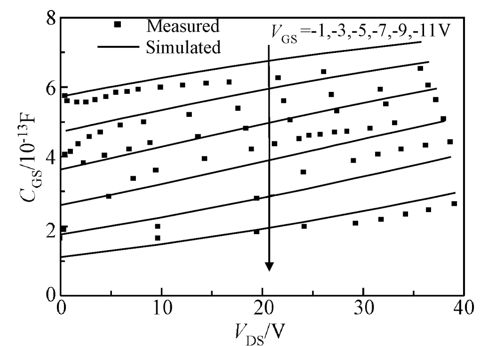

Fig. 5 Simulated and measured results of C_{GS} when static bias: V_{DS} = 19V, I_{DS} = 76mA, f = 0.9～6GHz

Table 4 shows a comparison of the simulation results from the present drain current model to that from the Curtice-Cubic and Materka models, which are active models of CAD tools, and Sayed and Manohar's models, which are the most recently reported 4H-SiC MESFET models. The regression tolerance is set at 10^{-10}, and the number of unchanged iterations is 10. In Table 4, RMS is the root mean square. The results show that present model has the best accuracy. Compared to Manohar and Sayed's models, the new model decreases the difficulty of setting initial values and accelerates convergence by avoiding the coefficients

Table 4 Comparison of the RMS error of the present drain current model with the most used CAD model in ADS

Drain current model	RMS /%	Number of undetermined coefficients
Present model	0.0125	7
Sayed model (Modified_Anglev model)	1.68	10
Manohar model	2.24	7
Curtice-Cubic[12]	5.78	7
Materka[13]	6.68	5

Table 5 Comparison of the RMS error of the present gate-source capacitance model with Normman Scheinberg and Chameber model

C_{GS} model	RMS/%	Number of undetermined coefficients
Present model	10.5	6
Normman Scheinberg	10.7	5
Chameber	12.5	3

Table 6 Comparison of the RMS error of the present gate-drain capacitance model with Normman Scheinberg and Chameber model

C_{GD} model	RMS/%	Number of undetermined coefficients
Present model	8.6	4
Normman Scheinberg	13.2	5
Chameber	18.3	3

with exponential behavior or undetermined coefficients. Also, the accuracy has been improved by the modification of the channel length modulation coefficient and saturation voltage coefficient compared to the GaAs FET-based Materka, Curtice-Cubic, Statz, and TOM3 models.

Tables 5 and 6 show a comparison of the simulation results from the present capacitance model to that from Normman Scheinberg and Chameber's model. The results show that our capacitance model is significantly more accurate.

A comparison of the simulated results for P_{out} (output power), PAE (power added efficiency), and gain with the measured data is shown in Fig. 6 ~8. The bias is $V_{DS} = 20V$, $I_{DS} = 80mA$, and the operational frequency f_0 is 1.8GHz. The simulated input and output impedances are 33.4 − 74.2j and 41.4 + 53.8j, respectively, which are quite comparable to the measured input and output impedances 22.4 − 74.2j and 41.4 + 53.8j.

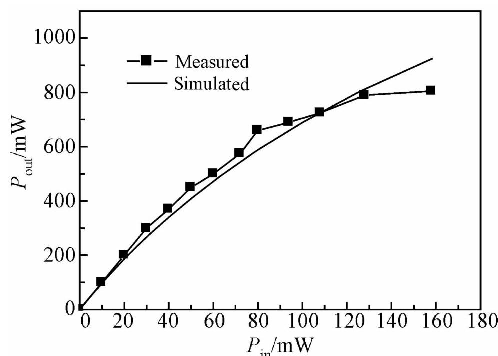

Fig. 6 Measured and simulated results of P_{out} at $V_{DS} = 20V$, $I_{DS} = 80mA$, $f_0 = 1.8GHz$

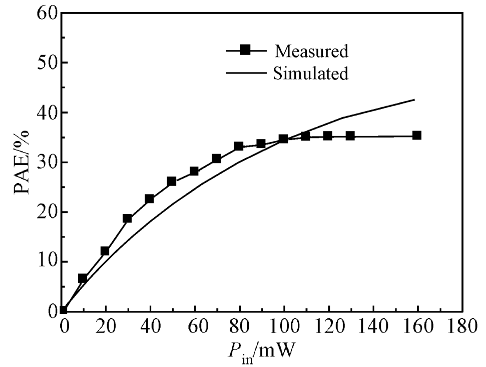

Fig. 7 Measured and simulated of PAE at bias of $V_{DS} = 20V$, $I_{DS} = 80mA$, $f_0 = 1.8GHz$

As can be seen from the comparisons, all simulation results match the experimental data well. The difference between the simulated and measured data increases when the input power is more than 100mW. The reasons may be: (1) The reduction of gain[25] due to the self-heating effects for the MESFET; (2) The trap effects in the buffer layer increasing the errors between modeled results and measured data near the pinch-off region for complicated *I-V* curves, which maybe mainly introduced by the conducting substrate of the 4H-SiC MESFET[26]; (3) The shift of the parasitic resistance due to frequency dispersion[26,27]. Therefore it can be expected for the present model that better agreement will be achieved if a semi-insulating substrate is used for the device.

5 Conclusion

A novel empirical large signal model has been presented for 4H-SiC MESFETs with an improved drain current model for the modification of the

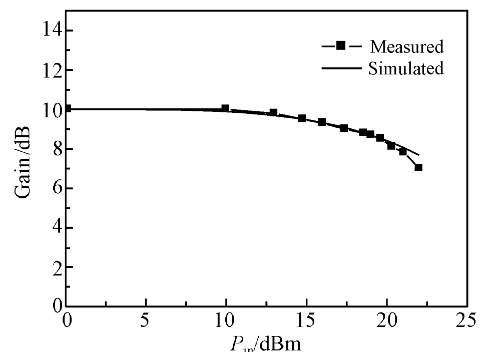

Fig. 8 Measured and simulated of gain at $V_{DS} = 20V$, $I_{DS} = 80mA$, $f_0 = 1.8GHz$

channel length modulation coefficient and the saturation voltage coefficient based on the Materka model, and with an improved charge conserving capacitance model for the improved Angelov model for C_{GS} and a new model for C_{GD}. The Levenberg-Marquardt method was used to optimize the parameter extraction. The present model has been embedded into ADS to simulate the performance of a 4H-SiC MESFET. The comparison of simulated results with measured data shows that good agreements are obtained for the DC I-V curves, P_{out}, PAE, and gain at the bias of V_{DS} = 20V, I_{DS} = 80mA and operational frequency of f_0 = 1.8GHz. The present model can be used for the design of a 4H-SiC MESFET RF & MW circuit, particularly 4H-SiC MESFET MMIC.

Further research should focus on modeling some other important remnant issues such as self-heating, frequency dispersion, and trap effects. They should be also considered in the 4H-SiC MESFETs large signal model in the future.

References

[1] Henry H G, Augustine G, DeSalvo G C, et al. S-band operation of SiC power MESFET with 20W (4.4W/mm) output power and 60% PAE. IEEE Trans ED, 2004, 51(6): 839

[2] Chen P, Chang H R, Li X, et al. Design and fabrication of SiC MESFET transistor and broadband power amplifier for RF applications. The 16th International Symposium on Power Semiconductor Devices and ICs, 2004: 317

[3] Sadler R A, Allen S T, Alcorn T S, et al. SiC MESFET with output power of 50watts CW at S-band. 56th Device Research Conference Digest, 1998: 92

[4] Zhu C L, Tin C C, Yoon S F, et al. A three-region analytical model for short-channel SiC MESFETs. Microelectron Eng, 2006, 83(1): 6

[5] Aggarwal S K, Gupta R, Haldar S, et al. A physics based analytical model for buried p-layer non-self aligned SiC MESFET for the saturation region. Solid-State Electron, 2005, 49 (7): 1206

[6] Mukherjee S S, Islam S S, Bowman R J. An analytical model for SiC MESFET incorporating trapping and thermal effects. Solid-State Electron, 2004, 48(10/11): 1709

[7] Yang Lin'an, Zhang Yimen, Lü Hongliang, et al. Analytical model of large-signal DC-IV characteristics 4H-SiC RF power MESFET's. Chinese Journal of Semiconductors, 2001, 22 (9): 1160 (in Chinese)[杨林安，张义门，吕红亮，等. 4H-SiC 射频功率 MESFET 大信号直流 I-V 特性解析模型. 半导体学报, 2001, 22(9): 1160]

[8] Murray S P, Roenker K P. An analytical model for SiC MESFETs. International Semiconductor Device Research Symposium, 2001: 195

[9] Lü Hongliang, Zhang Yimen, Zhang Yuming. Numerical modeling of anisotropy in 4H-SiC MESFETs. Chin Phys, 2003, 12: 895

[10] Siriex D, Noblanc O, Barataud D, et al. A CAD-oriented nonlinear model of SiC MESFET based on pulsed $I(V)$ pulsed S-parameters measurements. IEEE Trans Electron Devices, 1999, 46(3): 584

[11] Sayed A, Boeck G. An enhanced empirical large signal model of SiC MESFETs for power applications. IEEE SBMO/IEEE MTT-S International Conference on Microwave and Optoelectronics, 2005: 28

[12] Manohar S, Pham A, Evers N. Development of an empirical large signal model for SiC MESFETs. 59th ARFTG Conference Digest, 2002: 23

[13] Dambrine G, Cappy A, Heliodore F, et al. A new method for determination the FET small-signal equivalent circuit. IEEE Trans Microw Theory Tech, 1988, 36(7): 1151

[14] Henandez J A R, Rangel-Patino F E, Perdomo J. Full RF characterization for extracting the small-signal equivalent circuit in microwave FET's. IEEE Trans Microw Theory Tech, 1996, 44(12): 2625

[15] Cao Quanjun, Zhang Yimen, Zhang Yuming. A CAD oriented quasi-analytical large-signal drain current model for 4H-SiC MESFETs. Chin Phys, 2007, 16(4): 1097

[16] Kacprzak T, Materka A. Compact DC model of GaAs FETs for large-signal computer calculation. IEEE J Solid-State Circuits, 1983, 18(2): 211

[17] Wei C J, Tkachenko Y A, Bartle D. An accurate large-signal model of GaAs MESFET which accounts for charge conservation, dispersion. IEEE Trans Microw Theory Tech, 1998, 46(11): 1638

[18] Hallgren R B, Litzenberg P H. TOM 3 capacitance model: linking large- and small-signal MESFET models in SPICE. IEEE Trans Microw Theory Tech, 1999, 47(5): 556

[19] Root D. Nonlinear charge modeling for FET large-signal simulation and its importance for IP3 and ACPR in communication. Proceedings of the 44th IEEE Midwest Symposium on Circuits and Systems, 2001, 2: 768

[20] Scheinberg N, Chisholm E. A capacitance model for GaAs MESFETs. IEEE J Solid-State Circuits, 1991, 26(10): 1467

[21] Angelov I, Rorsman N, Stenarson J, et al. An empirical table-based FET model. IEEE Trans Microw Theory Tech, 1999, 47(12): 2350

[22] Yang Lin'an, Zhang Yimen, Zhang Yuming. An analytical large signal capacitance model for 4H-SiC MESFET. Chinese Journal of Semiconductors, 2002, 23(2): 188

[23] Bates D M, Watts D G. Nonlinear regression analysis and it's application. New York: John Wiley & Sons Inc, 1988

[24] Royet A S, Quisse T, Cabon B, et al. Self-heating effects in silicon carbide MESFETs. IEEE Trans Electron Devices, 2000, 47(11): 2221

[25] Yang Lin'an, Zhang Yimen, Yu Chunli. A compact model describing the effect of p-buffer layer on the I-V characteristics of 4H-SiC power MESFETs. Solid-State Electron, 2005, 49(4): 517

[26] Andersson K, Sudow M, Nilsson P A, et al. Fabrication and characterization of field-plated buried-gate SiC MESFETs. IEEE Electron Device Lett, 2006, 27 (7): 573

[27] Mitra S, Rao M V, Jones K A. Transconductance frequency dispersion measurements on fully implanted 4H-SiC MESFETs. Solid-State Electron, 2004, 48(1): 143

一种用于非线性分析的新型4H-SiC MESFET大信号经验模型*

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摘要：提出了一种简洁的新型4H-SiC MESFET经验大信号模型.在Materka漏电流模型基础上,改进了沟道调制因子和饱和电压系数的建模方式,电容模型采用了改进的电荷守恒模型.参数的提取和优化采用了Levenberg-Marquardt优化方法.在偏置点 $V_{DS}=20V$, $I_{DS}=80mA$ 和工作频率1.8GHz下,模型直流电流-电压扫描曲线、输出功率、功率附加效率和增益的模拟结果与实验数据符合良好.

关键词：4H-SiC MESFET；大信号；经验模型；Levenberg-Marquardt优化方法
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