A Novel Power Supply Solution of a Passive RFID Transponder

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Abstract: This paper presents a power supply solution for fully integrated passive radio-frequency identification (RFID) transponder IC, which has been implemented in 0.35μm CMOS technology with embedded EEPROM from Chartered Semiconductor. The proposed AC/DC and DC/DC charge pumps can generate stable output for RFID applications with quite low power dissipation and extremely high pumping efficiency. An analytical model of the voltage multiplier, comparison with other charge pumps, simulation results, and chip testing results are presented.

Key words: AC/DC; DC/DC; charge pump; RFID; voltage regulator; low-power CMOS
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1 Introduction

Radio frequency identification (RFID) systems have been developing rapidly in recent years. RFID systems consist of radio frequency transponders (tags), radio frequency transceivers (readers), and a host computer. Tags are attached to objects. In passive RFID systems at the UHF spectrum, which are considered in this paper, the reader unit and tag communicate via the backscattering of electromagnetic waves. The reader sends energy to the tag, which then harvests the energy and responds by backscattering its identification data. The transponder has a voltage multiplier, which is connected to the antenna. The transponder gets its operating power from the RF field radiated by the reader device. The voltage multiplier converts the antenna RF voltage at the operating frequency into two DC voltages of at least 0.65 and 1.5V for all active circuits on the chip, including the digital section, modulator, demodulator, and DC/DC charge pump for programming EEPROM[1,2].

2 Architecture

In this section, we will describe the design considerations of the power supply section of a fully integrated passive RFID transponder IC, including a voltage multiplier, a low-power voltage regulator, and a DC/DC charge pump. In the tag reading mode, the voltage multiplier and the regulator can provide a typical operating voltage of 1.5V with a 1MΩ load resistor when the input 900MHz RF power is 12μW. In the mode of writing to the EEPROM, the DC/DC charge pump circuit converts the DC supply voltage of 1.5V to a voltage of approximately 14V, which is needed for programming the EEPROM. With the assumption of a 2.5μA programming current, the input 900MHz RF power needs to be 210μW. The DC/DC charge pump works at a frequency of approximately 1MHz generated by an on-chip oscillator, which also can be used as the operating clock of the digital section.

2.1 *n*-stage voltage multiplier

Typical AC-DC charge pump circuits used in RFID are usually composed of a capacitor-diode network[3], as shown in Fig. 1. In order to increase output voltage and conversion efficiency, Schottky diodes are generally used for their low conduction resistance and low junction capacitance. However, the particularity of manufacturing processes for Schottky diodes and the inconsistency in quality between different product batches often make the integration of a Schottky charge pump incom-

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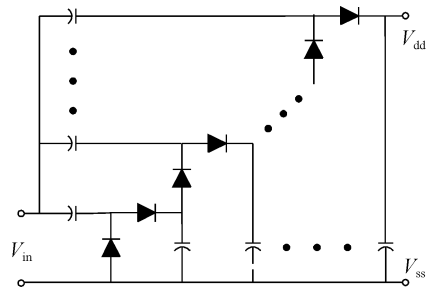

Fig. 1　Conventional Schottky-diode AC/DC charge pump

patible with standard CMOS circuits and thus limit its applications.

This paper presents a novel AC/DC charge pump for RFID application. Instead of expensive Schottky diodes, the proposed charge pump employs MOSFET diodes with low or zero threshold (V_{th}) that is compatible with standard CMOS technologies. With a low-power output regulator, the proposed charge pump converts input radio frequency (RF) signal power into DC voltage with high conversion efficiency and input-independence. In the next section, the novel charge pump circuit will be analyzed in detail.

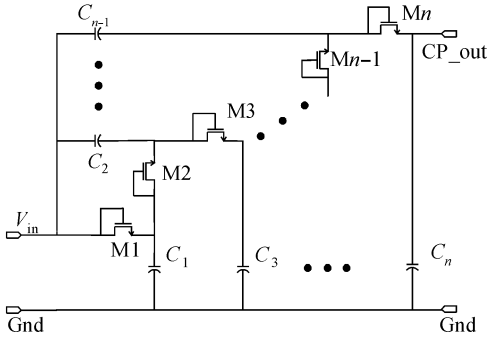

Fig. 2　Schematic of basic MOS charge pump

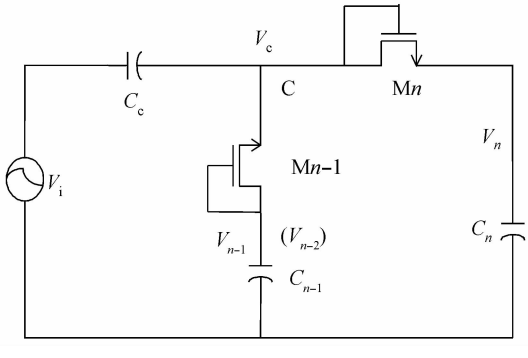

Fig. 3　Initial unit voltage multiplying cell

Figure 2 shows an odd AC/DC charge pump which utilizes ultra-low V_{th} nMOS FETs connected as diodes. Analyzing the initial unit voltage multiplying cell (UVMC) shown in Fig. 3, multiplying capacitor C_{n-1} and C_n can look like a pair of DC voltage sources. C_c is a coupling capacitor that combines input voltage V_i and V_{n-1}, the voltage drop on C_{n-1}, to provide a recharging voltage for the next multiplier. Suppose V_{dn-1} is the voltage drop on nMOS FET M$n-1$, V_{dn} for Mn, and V_c is the DC voltage at point C. Then under steady-state conditions, we have

$$V_c = V_{n-1} - V_{dn-1}$$
$$\therefore \quad V_c = V_n + V_{dn} \tag{1}$$

If W/L of two MOS FETs is identical (both equal to I_{ds}), we have

$$V_{dn} = V_{dn}$$
$$\therefore \quad V_c = (V_n + V_{n-1})/2 \tag{2}$$

The actual input signal for Mn is $V_c + V_i$.

Assume ΔV is the unit voltage increment, namely,

$$\Delta V = V_i - V_{dn},$$
$$(V_n + V_{n-1})/2 + \Delta V = V_n$$
$$\therefore \quad V_n = V_{n-1} + 2\Delta V \tag{3}$$

If re-defining a MOS FET and capacitor pair as new UVMC, the stage number in Fig. 2 becomes two, namely,

$$V_n = V_{n-2} + 2\Delta V \tag{4}$$

where $n = 2k + 1$, and k is the ordinal number of the initial UVMCs and is equal to 1, 2, 3…. With the same aspect ratio for all the MOSFETs in the charge pump, every ΔV would be identical. Iterating the above formula, we have

$$V_n = V_{n-4} + 4\Delta V = V_{n-6} + 6\Delta V \tag{5}$$

and finally, $V_n = n\Delta V$, which results in

$$V_n = n\Delta V = n(V_i - V_{dn}) \tag{6}$$

where n is the number of nMOS FETs and circuit stage number. In RFID applications, due to lack of input power, the output voltage and conversion efficiency of the AC/DC charge pump are hence the two primary performance parameters. One must pay extra attention to the tradeoff those two parameters.

2.2　Low-power regulator for charge pump

Due to the variance between V_i, RF input signals with different power levels, modulation indexes and modes will generate quite different and even unstable output voltages through the charge pump, which is not desired for a steady DC supply

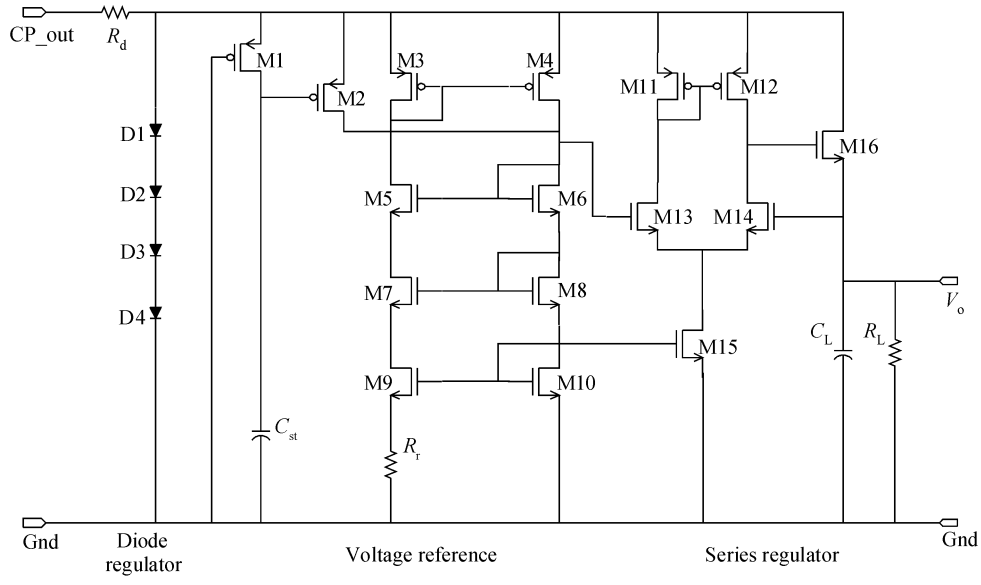

Fig. 4 Complete schematic of the low-power regulator

in an RFID transponder. For stabilizing output voltage, Figure 4 presents a proposed low power regulator that includes a diode regulator, a voltage reference, and a series regulator.

The diode regulator simply utilizes four series diodes to provide an elementary regulating strategy, which only confines large output swing to a comparatively low but still apparent and unfavorable degree. For the two following portions, such pre-regulation is necessary and makes them properly work in an appropriate and acceptable supply swing range to produce a more precise and stable output.

To reduce power dissipation, the required high reference voltage, such as 1.5V, is directly generated through a β self-biasing voltage reference instead of the conventional way to accurately amplify a pre-generated low reference voltage. As shown in Fig. 4, M5～M10 build up a triple cascade connection to increase the output resistance and all operate in the sub-threshold region for reduced power consumption. The series regulator simply utilizes a differential amplifier and a negative feedback nMOS FET to fix the output at a given reference voltage. In order to achieve low-dropout regulation and ensure that M16 operates in the saturation region, a native transistor the same as the one in the basic charge pump and very large W/L are employed.

2.3 DC/DC charge pump

Most DC/DC charge pump designs are based on the circuit proposed by Dickson. However, for high output generated voltages, the increase in the threshold voltage due to the body effect can significantly reduce the pumping efficiency. It is also known that the circuit performance is limited due to the threshold voltage drop of the nMOS devices and the reverse charge-sharing phenomenon. In recent years, several modifications of the Dickson's charge pump circuit have been proposed to solve the output voltage saturation problem.

2.3.1 NCP2 charge pump

The NCP2 circuit proposed by Ref. [4] is shown in Fig. 5. It utilizes charge transfer switches (CTS) to solve the problem of the body effect by using the next pumping voltages to switch each CTS. However, V_{th} still unavoidably grows along with the increasing body effect that results from increasing the pumping voltage presenting at each

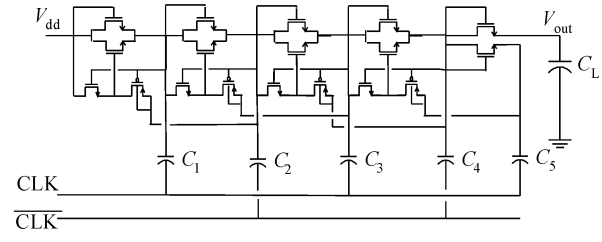

Fig. 5 A four-stage NCP2 charge pump circuit

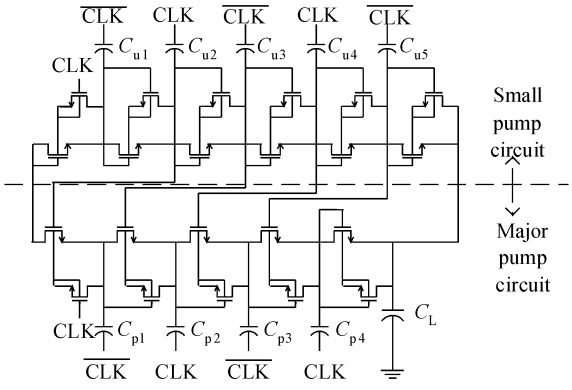

Fig. 6　A four-stage SP charge pump circuit

terminal of CTS. The NCP3 circuit proposed in Ref. [4], which uses a high-voltage clock generator, can eliminate the body effect, but it is not used widely because of the complicated high voltage amplitude clock generator circuit. Another problem of NCP2 mainly lies in increased parasitic capacitance at pumping nodes, which reduces the pumping efficiency.

2.3.2　SP charge pump

The small pump (SP) circuit[5], as shown in Fig. 6, utilizes an extra gate bias control circuit. The design concept in the SP is two-fold. It uses a small pump circuit to control the gates of the major pump circuit, which has a better pumping efficiency than NCP2. But the circuit suffers from two other problems: First, the technique to solve the body effect, utilizing the manufacture of floating body of nMOS transistors or triple-well technology, cannot be implanted in the normal ASIC process; Second, the circuit uses a small pump circuit for gate biasing in the main circuit, and this mechanism results in a reverse charge sharing problem.

2.3.3　Voltage-doubler charge pump

As shown in Fig. 7, the proposed charge pump circuit[6] utilizes cross-connected nMOS, with a voltage doubler as a pumping stage. The charge transfer from one stage to the next is accomplished by using a pair of pMOS as serial switches (MPi). The MOS transistors MSi can ensure the wells of the pMOS transistor switches always in the higher voltage between source and drain. For low-voltage operations and a large number of pumping stages, the MOS transistors MCi and MTi are used to reduce the body effect. The substrates of the pMOS are all connected in the common

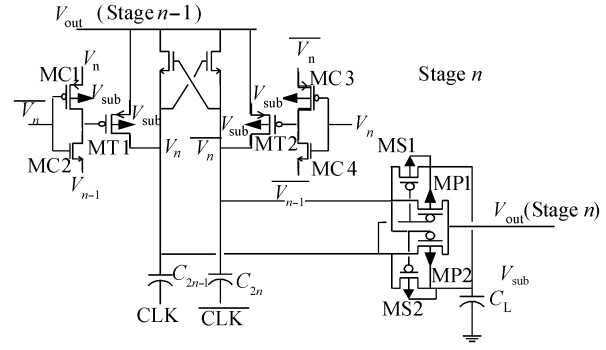

Fig. 7　One stage of the voltage doubler charge pump

node V_{sub} to ensure that they are always tied in the higher voltage between source and drain.

The charge pump circuit is complicated, and such many transistors used will increase the parasitic capacitances, which can reduce the output voltage gain. In addition, for higher voltage operation, the voltage doubler needs a very large transient charging current at the edge of the clock, which is difficult to get from the former stage AC/DC voltage multiplier.

2.3.4　Proposed charge pump

The proposed charge pump circuit is implemented in a normal n-well/p-type substrate CMOS 0.35μm process. As shown in Fig. 8, the two pumping clocks CLK and $\overline{\text{CLK}}$, which are generated by the on-chip oscillator (details omitted), are out-of-phase and have the same voltage amplitude V_{dd}. The pMOS transistors MTi are the main charge transfer parts. The nMOS transistors MNi and pMOS transistors MPi are used in this circuit to turn on and off completely as charge transfer switches. The operation of the charge pump circuit is explained as follows. When CLK becomes low and $\overline{\text{CLK}}$ becomes high, nodes 2 and 4 are charged to $V_2 + \Delta V$ and $V_4 + \Delta V$ by the couple capacitors C_2 and C_4, respectively. The voltages of nodes 1 and 3 are discharged from $V_1 + \Delta V$ and $V_3 + \Delta V$ to V_1 and V_3, respectively, in which $V_1 + \Delta V$ is equal to V_2, $V_2 + \Delta V$ is equal to V_3, and $V_3 + \Delta V$ is equal to V_4. The pMOS transistor MP2 turns on, which makes the gate voltage of MT2 nearly equal to the voltage of node 2. Then the charge transfer transistor MT2 turns off completely. Meanwhile, the nMOS transistor MN3 turns on, which makes the gate voltage of MT3 nearly equal to the voltage of node 1. Then the charge transfer transistor MT3 turns on completely, and charge is pushed from node 2 to node 3.

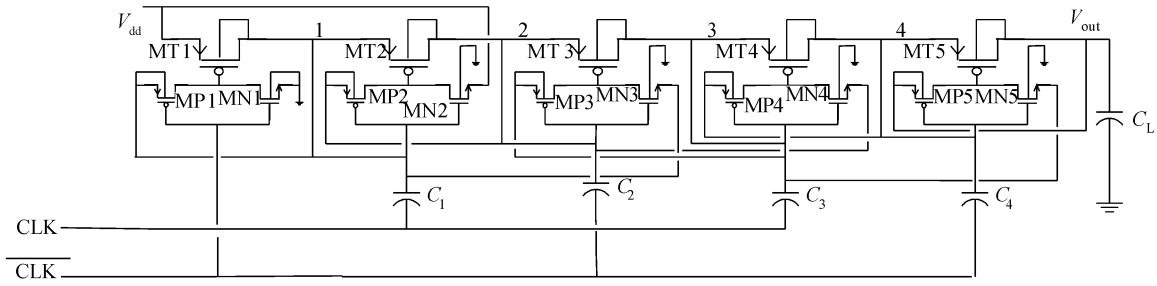

Fig. 8 Proposed charge pump circuit

The analysis of MT4 and MT5 is similar to MT2 and MT3, respectively. On the other hand, when CLK becomes high and $\overline{CLK}$ becomes low, there will be some similar analysis on these charge pumping transistors. Thus the new charge pump circuit will push the charge only in one direction effectively. We adopt a configuration in which the substrates are connected to the drains of the pMOS transistors. Proved by simulation results, the proposed substrate connecting technique has better pumping gain than techniques used in Ref. [7] or Ref. [8].

The proposed new charge pump circuit can reduce the threshold voltage drop, eliminate the body effect completely, and improve the pumping gain. Therefore, the new charge pump circuit can transfer voltage level more effectively than some other circuits.

3 Simulation results

Simulations were performed with the SPECTRE simulator, using 0.35μm CMOS technology with embedded EEPROM from Chartered semiconductor. Figure 9 shows the simulation results of the output voltage of the proposed AC/DC charge pump with different input signals. Based on the practical design demands, the output needs to reach 1.5V with a 1MΩ load resistor. In the tag reading mode, our simulation shows that when input 900MHz RF power changes from −19.25 to 13.22dBm, the deviation of the output V_{out} from 1.5V is less than 15mV. With a −19.25dBm (12μW) input power, the largest obtainable conversion efficiency is still 18.56%, which is higher than the reported results in Ref. [1]. In addition, the minimum input working power of 12μW is much lower than the results in Ref. [1].

In the mode of writing to the EEPROM, the DC/DC charge pump circuit converts the DC supply voltage of 1.5V to a voltage of approximately 14V, which is needed for programming the EEPROM. With the assumption of a 2.5μA programming current, the input 900MHz RF power of the AC/DC voltage multiplier needs to be 210μW.

Figure 10 shows the simulation results of the DC/DC charge pump output voltage against the number of the pumping stages. All the charge pump capacitances (C_i) are 2pF, and all the output load capacitances (C_L) are 20pF. All the sim-

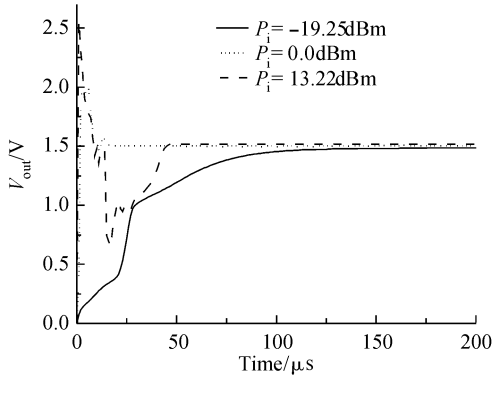

Fig. 9 Simulation results of MOS AC-DC charge pump

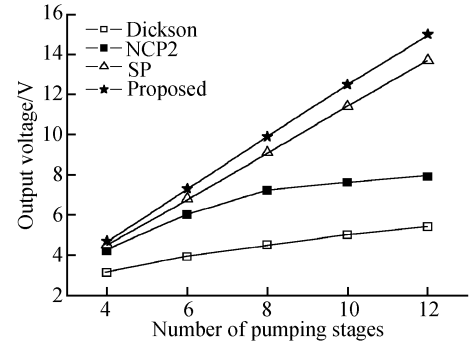

Fig. 10 Simulation results of the DC/DC charge pump output voltage against the number of the pumping stages

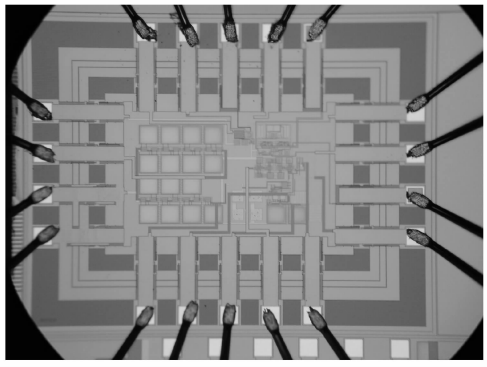

Fig. 11　Chip photograph of the presented circuits

ulations were carried out at 20MHz. It is obvious that the proposed charge pump circuit presents higher voltage gain when compared with other circuits[4,5] for any number of pumping stages. In addition, the proposed circuit is much less complicated than an SP charge pump and has better performance.

The proposed circuits can be used as a power supply for RFID with low power dissipation and high conversion efficiency.

4　Fabrication and measurements

We have implemented the proposed circuits in 0.35μm CMOS from Chartered Semiconductor. A chip photograph is shown in Fig. 11, which can be easily embedded into RFID transponder chips. Meanwhile, it also provides good compatibility with various CMOS digital or analog integrated circuits. Figure 12 shows the testing results of the AC/DC charge pump output voltage. When the amplitude of the 900MHz RF input signal is 80mV, the output voltage is stable at 1.52V, with a deviation less than 10mV. This agrees with the simulation results (1.5V) very well. With a 2.5μA load programming current, the tested output voltage of the DC/DC charge pump is 9.7V, which is lower than the simulation result (14.8V). This is due to an extra testing pad whose parasitic capacitance enormously worsens the pumping clock of the DC/DC charge pump. These testing results indicate that the presented novel circuit is capable of providing an efficient, stable and input-independent power supply for RFID transponder tags.

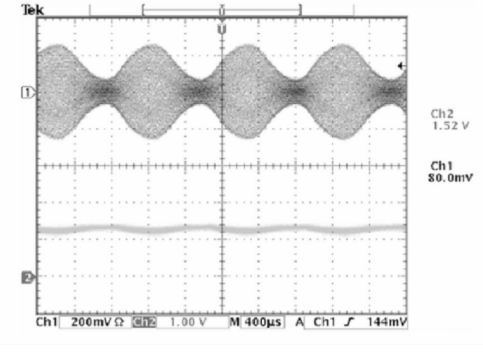

Fig. 12　Testing results of the AC/DC charge pump output voltage

5　Conclusions

We have reported a novel power supply section for passive UHF transponders. Theoretical analyses and circuit simulations used for the design optimization were presented. Proved by the chip testing, the circuit demonstrates the capability of generating stable and input-independent DC voltages as a power supply for RFID tags. Using more stable and compatible MOS FETs, these new circuits eliminate the process defects existing in the conventional Schottky diode based charge pumps. The proposed circuits are hence more compatible with other CMOS circuits and can be used in many areas where a passive power supply is needed.

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一种新型的基于无源射频身份识别应答器的电源供给方案

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摘要：提出了一种基于全集成的无源射频身份识别(RFID)应答器芯片的电源供给方案，并在特许半导体的 0.35μm 嵌入 EEPROM 的 CMOS 工艺线上流片成功.提出的 AC/DC 和 DC/DC 电荷泵能够为 RFID 的应答器芯片提供稳定的工作电压，同时具有极低的功耗和很高的充电效率.还给出了电压倍增器的分析模型、与其他电荷泵的升压原理的比较以及仿真结果和芯片测试结果.

关键词：AC/DC；DC/DC；电荷泵；射频身份识别；稳压电路；低功耗 CMOS
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