A Novel Fully-Depleted Dual-Gate MOSFET

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Abstract: A novel fully-depleted dual-gate MOSFET with a hetero-material gate and a lightly-doped drain is proposed. The hetero-material gate, which consists of a main gate and two side-gates, is used to control the surface potential distribution. The fabrication process and the device characteristics are simulated with Tsuprem-4 and Medici separately. Compared to a common DG fully depleted SOI MOSFET, the proposed device has much higher on/off current ratio and superior sub-threshold slope. The on/off current ratio is about 10^{10} and the sub-threshold slope is nearly 60mV/dec under a 0.18μm process.

Key words: hetero-material gate; on/off current ratio; sub-threshold slope; SOI FET
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1 Introduction

With the size of devices scaling down, the limits of conventional MOS structures are becoming more pronounced due to strong short-channel effects (SCEs) and quantum effects. The fully-depleted dual-gate (FDDG) SOI MOSFET is a good device candidate for silicon nano-scale CMOS[1~5]. The FDDG SOI structure has attracted particular attention due to its improved current drive capability[6,7]. However, common FDDG SOI MOSFETs also suffer from SCEs and severe anomalous off-state current. In order to improve transport efficiency and suppress SCEs, many methods have been proposed, such as the HALO, unsymmetrical doping, the split gate, and the hetero-material gate MOSFET (HMGFET)[8~13]. There are several technologies to realize the fabrication of sub-0.1μm gates. Ashing and trimming technologies have been successfully used to make about 17nm lines[14]. E-beam lithography has produced 15nm gates[15]. Spacer patterning technology is another way to achieve sub-0.1μm hetero-material gates[16,17]. The HMGFET structure is quite suitable for low-power high performance circuits in the VLSI industry because of its inherent benefits.

To enhance immunity against SCEs and off-state current and thereby improve device reliability in high performance circuit applications, a novel fully-depleted dual-gate MOSFET with hetero-material gate and lightly-doped drain structure is proposed. Only pMOS was studied here because one of the most important applications is for SRAM, in which the off-state current is a crucial issue. The top gate consists of two side gates (SG), which are biased independently of the main gate (MG) to provide an electrical shield to the channel region. To further reduce the off-state current, the S/D LDD frame is employed[10].

A cross-section view of the novel pMOS device is shown in Fig. 1. Compared to a common DG, the proposed configuration is demonstrated as an extremely reliable device configuration for low power high-speed applications.

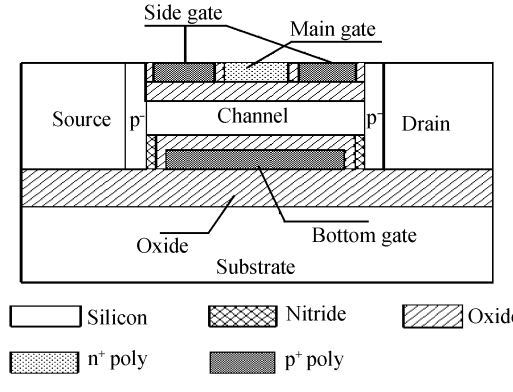

Fig. 1 Cross-sectional view of the novel structure

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2 Process design of the structure

The process flow of the novel structure is shown in Fig. 2. The designed process was simulated with Tsuprem-4.

A p(100) silicon wafer was kept in 1000℃ dry oxygen for 60min to form an oxide film. A 40nm-thick amorphous silicon layer doped with boron was deposited to form the bottom gate (BG). Then a 3nm-thick low temperature oxide (LTO) layer was deposited to form the BG dielectric. After that, a nitride sacrificial layer was deposited, as shown in Fig. 2(a). The nitride sacrificial layer was then polished away by chemical mechanical polishing (CMP) using the BG dielectric as a polish stop. An epi seed window was then opened on the bottom oxide on one side of the BG. The selective epitaxial silicon for the source, drain, and channel was then grown out of the seed window[18,19] (Fig. 2(b)). Later, the wafer was kept in 900℃ dry oxygen for 10min to form the top gate dielectric. The oxides above the drain and source were etched away. A nitride sacrificial layer was deposited on the top. The excess nitride was polished away by CMP using the top gate dielectric as a polish stop. Then the top gate was deposited and heavily doped with phosphorus as shown in Fig. 2(c). The side gates can be realized by a self-aligned asymmetric sidewall spacer process[20]. With one side gate masked, the top gate was asymmetrically etched, and then a 3nm-thick vertical separation oxide was formed by LTO (Fig. 2(d)). Another side of the top gate was done by the same process (Fig. 2(e)). After removing the mask, the side gate was deposited, doped with boron, asymmetrically etched, and finally polished by CMP using the main gate as a polish stop (Fig. 2(f)). Later a nitride sacrificial layer was deposited on the top gate, and then two more separation oxide layers were formed by LTO (Fig. 2(g)). The nitrides were removed by wet etching (H_3PO_4). Finally, the source/drain was elevated by SEG. A conventional LDD process was used. The implant energy for LDD and source/drain doping were both 10keV, and the dose was 2×10^9 for light implanting and 5×10^{14} for heavy implanting. The final structure is shown in Fig. 2(h).

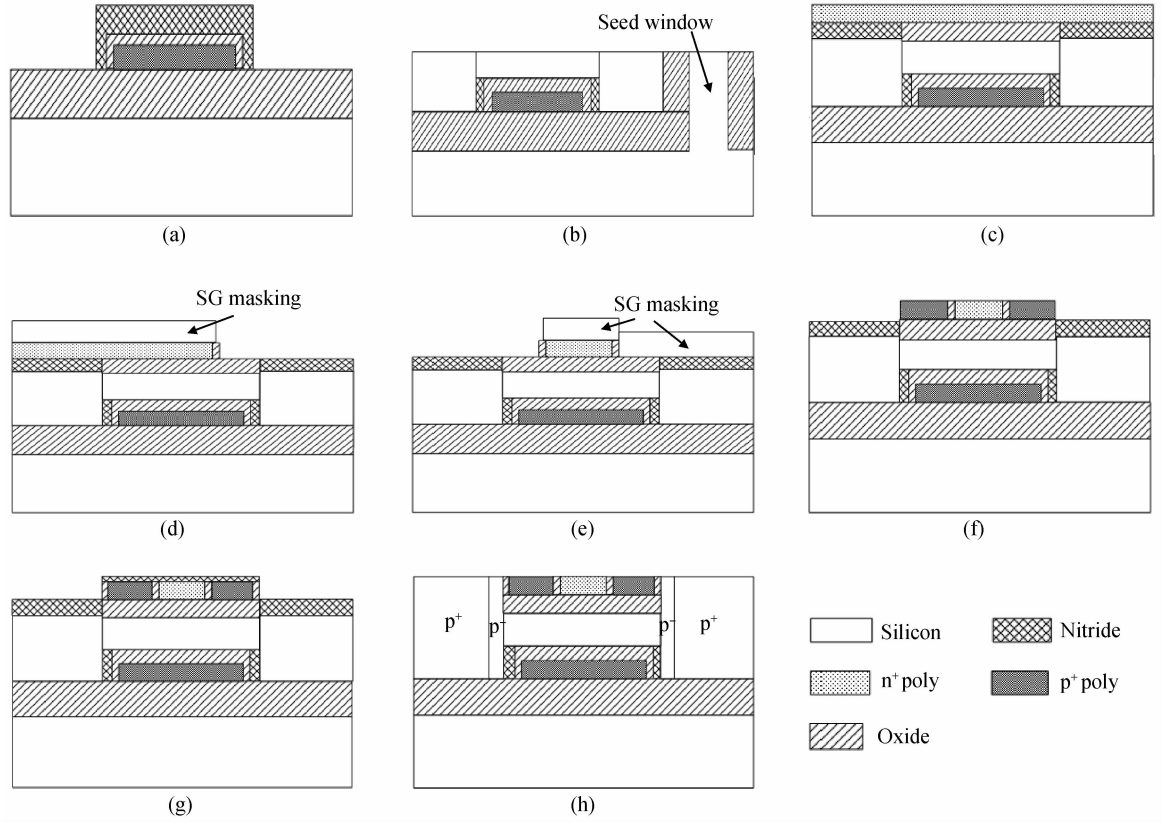

Fig. 2 Process flow of the novel structure

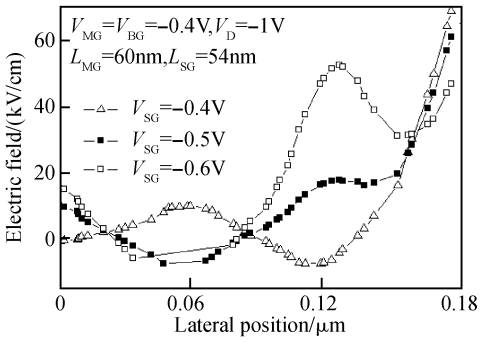

Fig. 3　Electric field distribution in the channel for various drain bias values

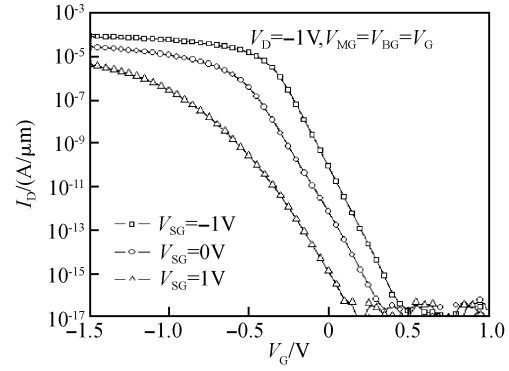

Fig. 5　Simulation results of the drain current

3　Parameter simulation and analysis

The proposed structure was simulated by MEDICI. The simulated longitudinal electric field distribution of the device for various SG bias values is shown in Fig. 3. The lengths of the BG, the front MG, and SG are 0.18, 0.06, and 0.054μm, respectively. The BG and MG are biased at -0.4V. It is evident from the figure that the increasing of the absolute value of negative SG bias reduces the electric field considerably at the drain end and increases the electric field at the source end. The hole velocity was improved and the hot carrier effect was suppressed accordingly. As a result, the on-state and off-state current can be effectively controlled by changing the SG bias.

The novel structure can suppress SCEs due to a screening effect, which is induced by a step change of the potential along the channel. Figure 4 shows the surface potential of the channel for various drain bias values. It can be seen from the figure that due to the presence of shielding provided by the inversion regions under the side gates, there is no significant potential change under the main gate. After current saturation, the additional drain voltage is absorbed under the side gate at the drain end. As a consequence, the V_{DS} has only a very small effect on the drain current after saturation. Therefore, the side gates are expected to effectively suppress the SCEs.

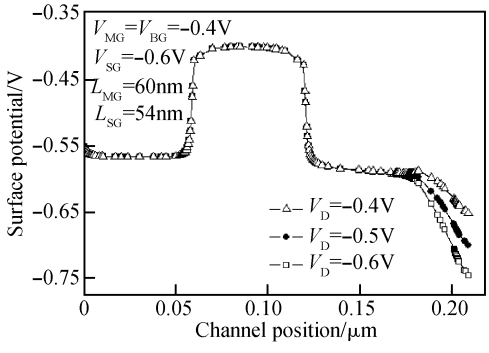

Fig. 4　Surface potential of the channel for various SG bias values

Figure 5 shows the simulated output characteristics. The minimum off-state current is about $10^{-13}\sim10^{-14}$ A/μm. The on-state current is about 10^{-4} A/μm. The ratio of the on and off current is about 10^{10}. A DG MOSFET with LDD was proposed just for the purpose of gaining a slight off-state current in Ref. [10], and the on/off current ratio is about 10^7. Compared to the device in Ref. [10], the anomalous current of the DG MOSFET has decreased remarkably, whereas the change of the on current is negligible. It can be seen that the channel current can be effectively controlled by the side gate bias. As a result, this increases the flexibility in controlling the output characteristics.

Two FETs with channel lengths of 0.18 and 0.35μm, respectively, are studied. As shown in Fig. 6, the sub-threshold slope of 0.35μm is nearly 60mV/dec. The sub-threshold slope of the 0.18μm device is not as good as that; however, it can also be optimized by controlling the side gate bias. It can be seen from the figure that the side gate affects the sub-threshold slope of smaller devices more evidently. Through changing the side gate bias, better sub-threshold slope can be obtained.

The threshold voltage values in the simulation are obtained from the commonly used maximum transconductance method. Figure 7 shows the threshold voltage roll-off as it varies with side gate bias. The roll-off is very small when the side

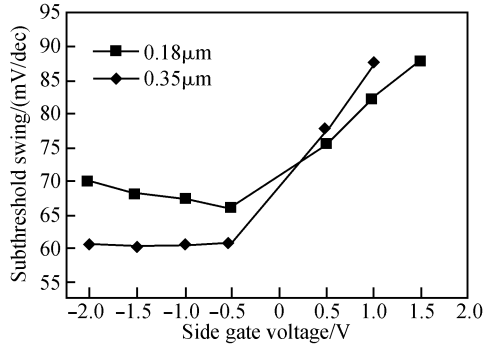

Fig. 6 Sub-threshold slope changes with SG voltage

gate voltage changes in the ideal work region. When given a positive side gate bias, the threshold voltage can also be controlled by changing the side gate bias. But unfortunately, the sub-threshold slope is up at this time.

4 Conclusion and prospect

To enhance immunity against SCEs and off-state current, a novel fully-depleted dual-gate MOSFET with a hetero-material gate and a lightly-doped drain structure is proposed. In the structure, two side gates on either side of the main gate are biased independently of the main gate to provide an effective electrical shield for the channel region from the drain voltage variations. The immunity of short channel effects and output characteristics have been improved accordingly. Compared with the existing common DG FET reported in Ref. [10], the proposed structure has much lower off-state leakage current and superior sub-threshold slope without significant change of the on-state current. A larger on/off current ratio is obtained accordingly. Moreover, the use of a changeable side gate bias to optimize the sub-threshold slope and threshold voltage leads to the flexibility of channel controlling.

Further improvements can be expected by the designing of the process and optimizing the length ratio between MG and SG. It is expected that the proposed device could be of significant use in CMOS applications requiring extreme scaling with low power, high speed, and good reliability.

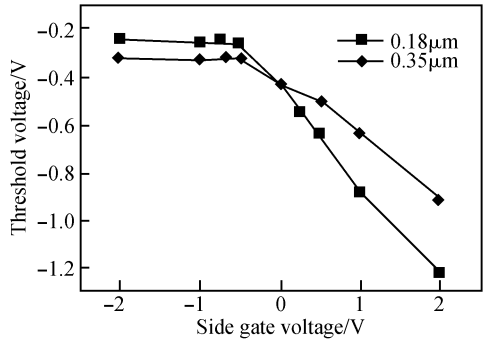

Fig. 7 Adjust threshold voltage with SG voltage

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一种新型全耗尽双栅 MOSFET

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摘要：提出一种新型全耗尽双栅 MOSFET，该器件具有异质栅和 LDD 结构. 异质栅由主栅和两个侧栅组成，分区控制器件的沟道表面势垒. 通过 Tsuprem-4 工艺模拟和 Medici 器件模拟验证表明，与普通双栅全耗尽 SOI 相比，该器件获得了更好的开态/关态电流比和亚阈值斜率. 在 0.18μm 工艺下，开态/关态电流比约为 10^{10}，亚阈值斜率接近 60mV/dec.

关键词：异质栅；关态电流；亚阈值斜率；SOI 场效应晶体管

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