Total Dose Radiation Hardened PDSOI CMOS 64k SRAMs

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Abstract: The first domestic 1×10^6 rad(Si) total dose hardened 1.2μm partially depleted silicon-on-insulator (PDSOI) 64k SRAM fabricated in SIMOX is demonstrated. The address access time is independent of temperature from −55 to 125℃ and independent of radiation up to 1×10^6 rad(Si) for the supply voltage V_{DD}. The standby current is 0.65μA before the total dose of radiation and is only 0.80mA after radiation exposure, which is much better than the specified 10mA. The operating power supply current is 33.0mA before and only 38.1mA afterward, which is much better than the specified 100mA.

Key words: PDSOI; SRAM; total dose; radiation
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1 Introduction

Previous investigations have been reported on radiation hardened 1.2μm partially depleted silicon-on-insulator (PDSOI) H-gate nMOSFETs[1,2] and 4k SRAM fabricated in SIMOX material[3,4]. This work reports the first domestically produced radiation hardened 1.2μm PDSOI 64k SRAM fabricated in SIMOX material. The SOI radiation hardening process was developed by the use of partially depleted front and back channel 1.2μm transistors with body-ties and demonstrated by the fabrication of a radiation hardened 64kb SRAM. Four key elements were specially treated to achieve the hardening: the gate oxide, the gate edge, the field oxide, and the buried oxide[5]. In this work, induced standby currents of 1.2μm PDSOI 64k SRAMs as a function of total dose from 1×10^5 to 1×10^6 rad(Si) are reported. The operating power supply current of the SRAM as a function of total dose from 1×10^5 to 1×10^6 rad(Si) is also reported.

2 Experiment

The SIMOX wafers used in this study were standard O^+ implanted wafers acquired from SIMGUI. The post oxygen implant anneal resulted in approximately 375nm of buried oxide and approximately 190nm of top silicon. The HF decorated defect density is less than 0.5cm^{-2}[6]. The processing steps for 1.2μm PDSOI 64k SRAM essentially include LOCOS isolation, twin well definition, gate oxidation, LDD, n^+/p^+ source and drain implant, contact, first metal, via, second metal. Note that the gate oxide is 18nm, and the source/drain and the polysilicon gate are titanium silicide. Figure 1 shows the layout of the 1.2μm PDSOI 64k SRAM. The chip size for the SRAM is 9.26mm×7.68mm and a cell size of the SRAM is 27μm×23.6μm.

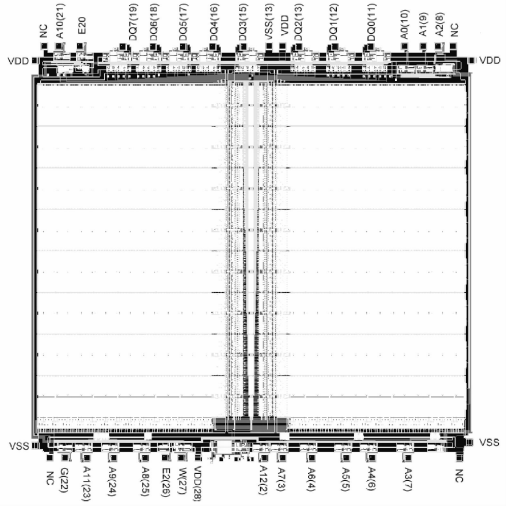

Fig. 1 Layout of 1.2μm PDSOI 64k SRAM

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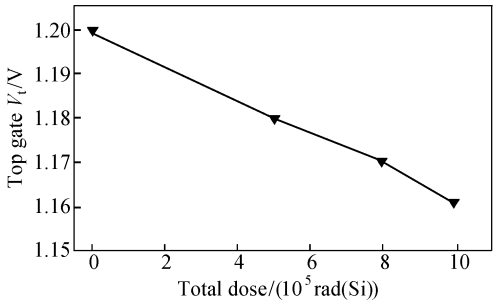

Fig. 2　Top gate V_t as a function of total dose

The Co-60 irradiation facility at the Northwest Institute of Nuclear Technology was used for total dose radiation testing, providing a dose rate of 50rad(Si)/s as measured from the Unidos dose tester. The ambient temperature and humidity of the testing environment were 27.5℃ and 45%, respectively. The experiments were done at V_{DD} = 5V and were tested in real time. The SRAM and ROM radiation effect testing system developed by the Northwest Institute of Nuclear Technology could provide the real time DC and AC electrical parameters of the SRAM.

3　Results and discussion

First, we assessed the total dose hardness of the gate oxide and the buried oxide by measuring the respective threshold voltage shifts of the individual transistor using a Co-60 irradiation source. Very small radiation induced threshold voltage shifts (<50mV) at 1×10^6rad(Si) were observed for 10/1.2 top gate nMOSFETs under turn-on irradiation bias ($V_G = 0$, $V_D = V_{DD}$, $V_S = 0$, $V_{body} = 0$) as shown in Fig. 2. The gate oxide was thus hardened to 1×10^6rad(Si).

Since back gate pMOSFETs do not show unfavorable radiation induced threshold voltage shifts (negative shift only for pMOSFETs), we report here only the results of the back gate nMOSFETs under the turn-on irradiation bias condition. The total dose hardness of the buried oxide is assessed by the back gate threshold voltage as a function of total dose shown in Fig. 3. The back gate threshold voltage at 1×10^6rad(Si) is about 18V, so the buried oxide is total dose hardened to 1×10^6rad(Si).

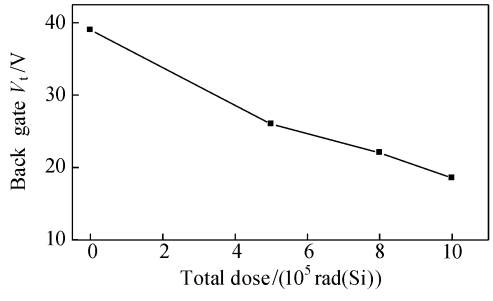

Fig. 3　Back gate V_t as a function of total dose

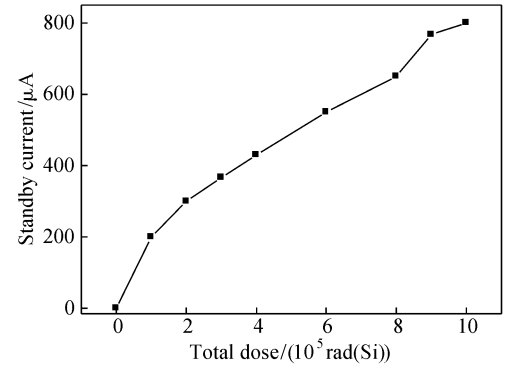

Fig. 4　Pre-radiation and post-radiation standby current as a function of total dose

Second, we assessed the total dose hardness of the gate edge and the field oxide by measuring standby current in packaged 64k SRAMs. The results of the pre-radiation and post radiation standby currents of 64k SRAM are shown in Fig. 4.

The access time as a function of temperature from −55 to 125℃ is shown in Fig. 5 for a 1.2μm PDSOI 64k SRAM. The address access time of the SRAMs varied from 22.4 to 25.2ns at V_{DD} = 5V in the temperature range of −55 to 125℃ before irradiation. The degradation was less than 0.5ns after irradiation to 1×10^6rad(Si).

The write time (write pulse) as a function of the temperature from −55 to 125℃ is shown in Fig. 6 for 1.2μm PDSOI 64k SRAM. The write time of the SRAM varied from 12.9 to 14.1ns at V_{DD} = 5V in the temperature range of −55 to 125℃ before irradiation. The degradation was less than 0.5ns after irradiation to 1×10^6rad(Si).

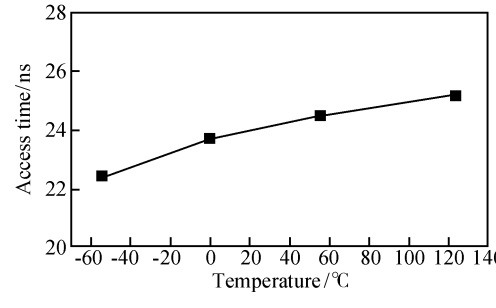

Fig. 5　Access time as a function of temperature

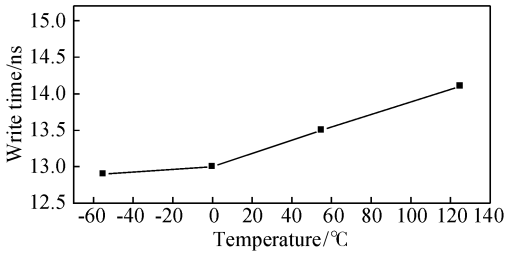

Fig. 6 Write time as a function of temperature

SRAM operating power supply currents were measured as a function of total dose through 1×10^6 rad(Si) at $V_{DD}=5$V. The results are shown in Fig. 7.

4 Conclusions

1×10^6 rad(Si) total dose hardened partially depleted top and back gate individual 1.2μm transistors have been fabricated in SIMOX. The first total dose hardened 1.2μm PDSOI 64k SRAM has been demonstrated. The address access time of the SRAM varied from 22.4 to 25.2ns at $V_{DD}=5$V in the temperature range of -55 to 125℃. Typical access time degradation was less than 0.5ns after irradiation to 1×10^6 rad(Si). The standby current of the 64k SRAM was only 0.8mA at 1×10^6 rad(Si) which is less than the specified 10mA. The operating supply current of the SRAM was 38.1mA, which is less than the specified 100mA.

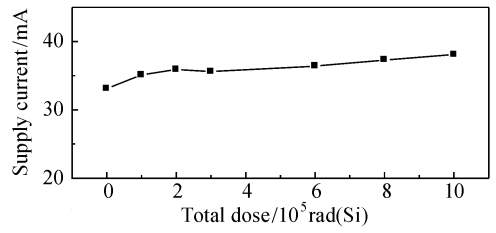

Fig. 7 Power supply current as a function of temperature

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总剂量辐照加固的 PDSOI CMOS 64k 静态随机存储器

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摘要： 在国内首次使得 1.2μm 部分耗尽 SOI 64k 静态随机存储器的抗总剂量能力达到了 1×10^6 rad(Si)，其使用了 SIMOX 晶圆. 在 $-55\sim125$℃ 范围内，该存储器的数据读取时间几乎不变. 在经过剂量为 1×10^6 rad(Si)的总剂量辐照后，该存储器的数据读取时间也几乎不变，静态功耗仅从辐照前的 0.65μA 变化为辐照后的 0.8mA，远远低于规定的 10mA 指标；动态功耗仅从辐照前的 33mA 变化为辐照后的 38.1mA，远远低于规定的 100mA 指标.

关键词： 部分耗尽 SOI；静态随机存储器；总剂量；辐照

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