Combined Novel Gate Level Model and Critical Primary Input Sharing for Genetic Algorithm Based Maximum Power Supply Noise Estimation*

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Abstract: A gate level maximum power supply noise (PSN) model is defined that captures both IR drop and di/dt noise effects. Experimental results show that this model improves PSN estimation by 5.3% on average and reduces computation time by 10.7% compared with previous methods. Furthermore, a primary input critical factor model that captures the extent of primary inputs' PSN contribution is formulated. Based on these models, a novel niche genetic algorithm is proposed to estimate PSN more effectively. Compared with general genetic algorithms, this novel method can achieve up to 19.0% improvement on PSN estimation with a much higher convergence speed.

Key words: power supply noise; gate level model; niche genetic algorithm
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1 Introduction

The continual shrinking of IC devices pushes ICs towards higher frequency, higher power dissipation, and lower supply voltage[1], resulting in lower power supply noise (PSN) margins. PSN reduces devices' actual voltage level and causes performance degradation, reliability problems, and even logic and timing errors [2]. Therefore, maximum power supply noise estimation is becoming a major design concern in nanometer IC design.

Since both the IR drop deriveing from on-chip power grid resistance and di/dt noise from I/O buffer switching contribute to power supply noise greatly, several approaches have been proposed to estimate IR drop[3~6], as well as di/dt noise[7,8]. Senthinathan *et al*.[8] proposed an electrical chip-package interface model and analytical equations to calculate I/O buffers' simultaneous switching noise. Chang *et al*.[7] presented a scaling model to characterize the ground bounce due to internal circuit switching. As far as IR drop is concerned, several algorithms have been proposed to find an upper bound for the maximum instantaneous current. Kriplani *et al*.[3] illustrated a vectorless algorithm based on uncertainty waveform propagation, but this upper bound estimation is too pessimistic. Jiang *et al*.[4] further improved the performance by integer linear programming. Hsieh *et al*.[9] presented a state-of-the-art graph algorithm based on mutually exclusive switching relationships between gates. However, these algorithms are too complicated to suitable for large circuit analysis. Another category of research is to obtain a lower bound of the maximum instantaneous current. Krstic *et al*.[5] presented a timed automatic test pattern generation strategy with the costs of huge memory and extensive computation. Jiang *et al*.[6] proposed a genetic algorithm-based estimation procedure, and their method is similar to the prior approach[5] but requires a shorter execution time.

Previous works have either considered IR drop by maximum instantaneous current or di/dt noise by I/O buffer switching. None has considered di/dt noise due to logic cores, which becomes equally important for high performance chip designs[10]. Its increasing importance can be attributed to large functional density (logic cores draw more current, thus resulting in larger power supply noise), fast clock rates (higher switching

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frequency makes the di/dt noise much larger), and drastically reduced resistance of low-k copper interconnects (lower resistance alleviates IR drop effects and causes di/dt noise to be more important) in nanometer designs[1]. Therefore, this paper focuses on the research of on-chip logic core-induced di/dt noise, as well as IR drop effects.

The contributions in this paper are as below:

(1) To our best knowledge, this is the first proposal of a gate level maximum power supply noise model that captures both IR drop and di/dt noise effects. The novel model in this paper improves power supply noise estimation by 5.3% on average with 10.7% less computation time compared to schemes presented in previous literature[3~6,9].

(2) A primary input critical factor model is formulated that captures the extent of primary inputs' contribution to power supply noise. Based on the models, a novel niche genetic algorithm is brought forward to efficiently estimate the maximum PSN. Compared with simple genetic algorithms, this method improves the estimation by 13.8% on average with negligible computation overhead.

2 Preliminaries and proposed models

In this section, the circuit model used in our analysis is first presented, and then traditional model limits are illustrated and two novel models are proposed.

2.1 Preliminaries

The power/ground network circuit model is illustrated in Fig. 1, where the parasitic resistance, inductance, and capacitance of the power network are denoted as R_i, L_i, and C_i ($i=1,2$ for on-chip power network and $i=$ p, s for package power network, respectively). On-chip inductance can be ignored below 1GHz, and PSN is defined as[10]

$$V_{\mathrm{PSN}}(t) = V_{\mathrm{dd}} - V_{\mathrm{ss}} - V_{\mathrm{ddb}}(t) + V_{\mathrm{ssb}}(t) \quad (1)$$

where V_{dd} and V_{ss} are the package supply voltages, and $V_{\mathrm{ddb}}(t)$ and $V_{\mathrm{ssb}}(t)$ are the transient voltage waveforms.

Although transistor level PSN estimation is accurate, its computation cost is unaffordable. Most works have tried to find input patterns to excite the worst case in the gate level[3~6,9]. In those works, a gate level model is defined to capture the noise trend under a specific input vector p as follows:

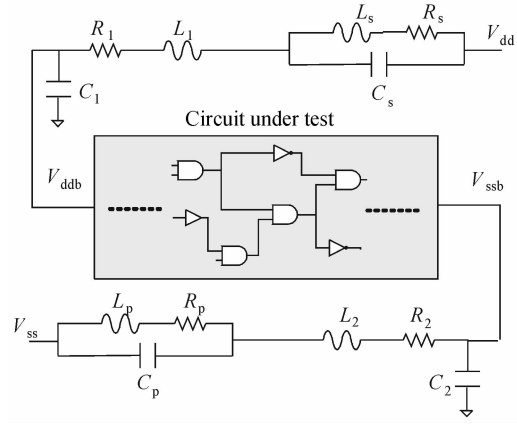

Fig. 1 Power/ground network model

$$\mathrm{Metric\_MIC}(p) = \max_{t_i \in [0, T_{\mathrm{clk}}]} \sum_{g \in \mathrm{circuit}} F(g)\chi(p, t_i) \quad (2)$$

where T_{clk} is the clock cycle time, $F(g)$ is the fanout load of gate g, and $\chi(p, t_i)$ is a function determined by input vector p and time t_i. Its value is 1 if gate switches at time t_i, and otherwise is 0. Metric_MIC(p) represents the trend of maximum instantaneous current, denoted as the MIC model in this paper. From its definition, it is straightforward to see that this model fails to capture the di/dt component in power supply noise.

2.2 Gate level maximum PSN model (GLMP)

With technology scaling down, power/ground switching current rate, i.e. di/dt noise, is becoming even more important[11], and will be the main focus in the following model. The following are three observations on power supply noise by transistor level simulations using TSMC 0.18μm technology.

Observation 1: Primary inputs with larger fanout cone loads contribute more to power supply noise than those with smaller fanout cone loads.

Observation 2: Maximum power supply noise due to di/dt noise occurs in the first few hundred picoseconds. The excitation in primary inputs can control the first few lower level gates in the circuit, but fails to control the deeper level gates[11]. Therefore, a maximum current surge most likely

appears at the beginning of the clock edge.

Observation 3: Switching in small fanout gates contributes more to power supply noise than that in larger fanout gates, because lower fanout gates switch much faster and trigger their sub gates more within the early period of the clock cycle.

The maximum power supply noise in nanometer ICs is not only dependent on the maximum instantaneous current, but also on the $\mathrm{d}i/\mathrm{d}t$ component. According to Observations 1～3, fanout cone load, transition time, and gate fanout are the most important factors that affect power supply noise. Therefore, the novel GLMP model under input vector p is formulated as below:

$$\text{Metric\_GLMP}(p) = \sum_{t_i \in [0, T_{\text{th}}]} \sum_{g \in \text{circuit}} \varphi(g)\chi(p, t_i) \tag{3}$$

where T_{th} is set as the maximum of 1/3 of the critical path delay and is 1.5ns in this paper, $\chi(p, t_i)$ has the same definition in Eq. (2), and $\varphi(g)$ equals 1 if $\text{EAT}(g) < T_{\text{th}}$ and otherwise is 0. $\text{EAT}(g)$ is the earliest arrival time of gate g, obtained by static timing analysis[6].

Compared with traditional models, the novel model captures both the IR drop and $\mathrm{d}i/\mathrm{d}t$ effects and it gives a more accurate power supply noise estimate faster due to reduced searching space, as validated by the experimental results in Section 4. It should be noted that this novel model is general and independent of optimization algorithms used to search the maximum power supply noise vector pair.

2.3 Critical primary input factor model (PICF)

Next, a critical primary input factor model is proposed to improve the efficiency of traditional simple genetic algorithm-based power supply noise estimation. This is due to the fact that some primary inputs have a much larger impact on power supply noise. Based on Observations 1～3, each primary input's contribution to the maximum power supply noise is defined as below:

$$\text{CF}(i) = \sum_{g \in \text{FOC}(i)} \varphi(g)\left(1 - \frac{L(g)}{\text{Maxlevel}}\right) \tag{4}$$

where $\text{FOC}(i)$ is the ith primary input's fanout cone, $L(g)$ is the logic level of gate g, Maxlevel is the circuit's maximum logic level, and $\text{CF}(i)$ is the ith primary input's critical factor.

Algorithm CPI-NGA PSN estimation

1: Rearrange primary inputs based on PICF
2: Partition primary inputs into critical and minor set
3: For $j = 0$ to MAX_GA_NUM do
4: GLMP based fitness evaluation
5: Fitness linear scaling
6: PICF model based fitness sharing
7: Stochastic universal selection
8: One-point crossover & adaptive mutation
9: end for
10: Transistor level simulation by HSPICE under input vector p (V1/V2) with the highest fitness
11: Report PSN

Fig. 2　Genetic algorithm based maximum PSN estimation

Obviously, a larger critical factor value means that the primary input contributes more to the maximum power supply noise. Given T_{th}, primary inputs with high critical factor have more fanout cone gates with small loads since the gate delay is proportional to its loads[12]. The procedure aims at searching the proper vector pair to maximize the power supply noise, and thus it focuses on the most critical inputs based on our model. Experimental results in Section 4 will show the model's effectiveness and efficiency.

3 Niche genetic algorithm based power supply noise estimation

A novel niche genetic algorithm-based power supply noise estimation framework is illustrated in this section, which adopts both GLMP and PICF models. Figure 2 shows our algorithm flowchart, (thereafter denoted as CPI-NGA), involving coding strategy, crossover, mutation, fitness function, and selection.

3.1 Coding strategy

Low state, high state, low-to-high transition, and high-to-low transition are coded as {00, 11, 01, 10} in the chromosome string, respectively. Primary inputs are encoded in their critical factor in descending order, and this coding scheme is effective and efficient from schema theorem perspective[14]. Assuming that $p = \{(s_1, s_2, \cdots, s_N)\}$ is the optimal schema, schema with high fitness are likely to survive because critical primary inputs are grouped. Otherwise, one-point crossover will

frequently disrupt long schemas.

3.2 Crossover and mutation

Separating critical primary inputs from minor ones also has advantages in crossover and mutation operations. As previous work[3] demonstrated, it is common for large spike current to occur, mainly due to several critical primary input changes. Taking primary inputs in an equal manner, simple genetic algorithm crossover fails to realize effective exploitation. On the other hand, one point crossover in the proposed algorithm is quite suitable due to considering critical factor information. Furthermore, to enhance the searching efficiency in a genetic algorithm, a one-bit mutation is used for critical primary inputs, and a two-bit operator is used for minor ones. In this paper, the crossover rate is set as 0.8 and the mutation rate is set as one bit for the critical PIs and two bits for the minor PIs.

3.3 Fitness definition and fitness sharing

To accelerate search efficiency, a fitness function is defined based on the GLMP model, and a linear scaling function adjusts an individual's raw fitness[14]. To prevent the genetic algorithm-based exploration from being trapped in local optima, fitness sharing is used to extend the simple genetic algorithm.

Nonetheless, choosing a proper dissimilarity threshold δ_{sh} remains the major challenge for the fitness sharing technique[15]. Setting δ_{sh} as the string length of the candidates makes searching inefficient because fitness sharing in minor primary inputs has little impact. Therefore, a method that adopts diversity control only on critical primary inputs is proposed, which is further validated by the experiments in the next section.

4 Experimental results

CPI-NGA is implemented in C++ on a Solaris platform. The population size is set twice as large as the critical primary input number. Thereafter all experimental results are the average values of 10 simulations. All input vector pairs acquired from the gate level model are validated by the transistor level simulation for exact comparison, which is done by HSPICE simulation using

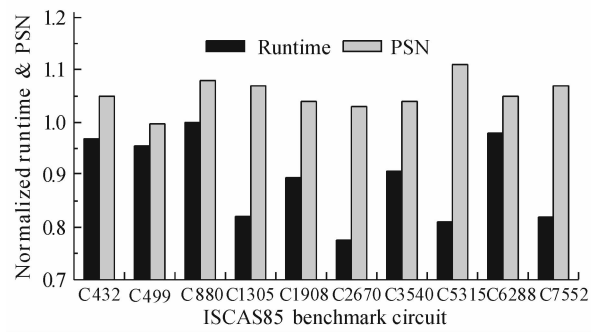

Fig. 3 PICF-based SGA improvement over MIC-based SGA on runtime & PSN

0.18μm TSMC technology, and the typical rise/fall time value of input signals is 100ps. In this section, the effectiveness and efficiency of the GLMP model in capturing both IR drop and di/dt noise is presented first, and then the superior performance of the proposed novel genetic algorithm.

4.1 GLMP model effectiveness and efficiency

Figure 3 is an accuracy comparison and runtime comparison of the GLMP model-based simple genetic algorithm (SGA) and traditional model-based SGA on ISCAS85 benchmark circuits. Both runtime and maximum power supply noise are normalized to that of the traditional approach.

As demonstrated in Fig. 3, the novel model improves the maximum power supply noise estimation by 5.3% on average and 11% at maximum. The improvement makes sense because the GLMP model captures di/dt noise as well as the IR drop component. In addition, Figure 3 also illustrates the speed advantage of the novel model over the traditional model. On average, about 10.7% simulation reduction is observed. Simulation time is reduced by up to 22.5% for the circuit C5315, which has deep logic level and unbalanced primary input critical factor distribution. This is because the novel model only considers gates whose earliest arrival time occurs in the specific threshold of the early period of the clock cycle. By eliminating gates whose earliest arrival time is unsatisfactory, the GLMP-based fitness evaluation can be done much faster.

4.2 PICF model-based niche genetic algorithm

In this section, the proposed CPI-NGA is

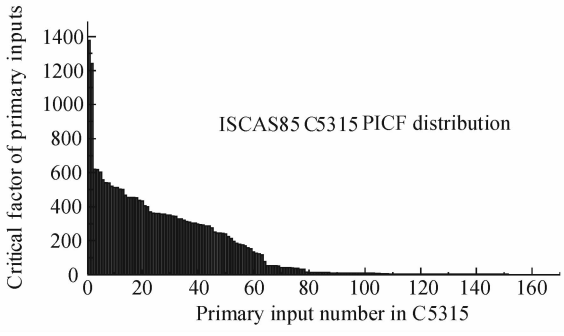

Fig. 4　C5315 primary input CF distribution

compared with the SGA[13] and general niche genetic algorithm (NGA) using equal primary input sharing techniques. All fitness functions are calculated based on the GLMP model. Here is an experiment on ISCAS85 circuit C5315. Figure 4 is its histogram of primary input critical factors. Primary inputs can be can be partitioned into 64 critical and 114 minor ones.

With a population size of 128 and 50 generations, we make a test on C5315 using different methods. PSN values and its trend by CPI-NGA, SGA, and NGA are plotted in Fig. 5. Obviously SGA is prone to be trapped in local optima before 40 generations. The improvement of NGA and CPI-NGA from the 45th generation to the 50th generation is less than 0.5% and 1.0% respectively, and therefore setting the number of generations to 50 is enough. With better tradeoff in evolutional selection and diversity control, there are improvements of 10.3% for NGA and 17.8% for CPI-NGA in maximum power supply noise estimation separately. In addition, Figure 5 also shows that CPI-NGA with diversity control on critical primary inputs converges to the final solutions much faster than the other two approaches.

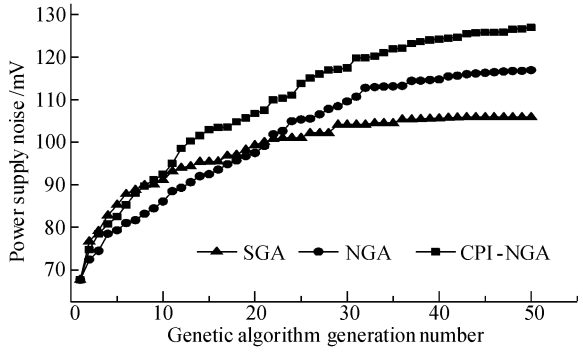

Fig. 5　CPI-NGA versus NGA and SGA on C5315

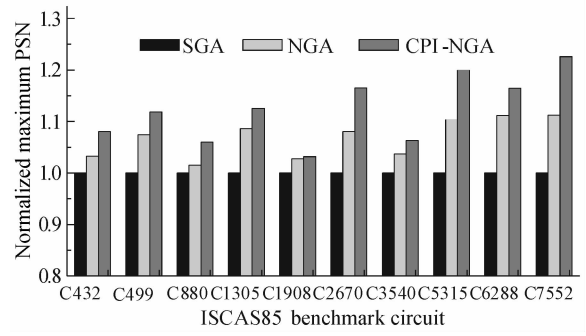

Fig. 6　ISCAS85 PSN estimation by SGA, NGA and CPI-NGA

The following are the experimental results of different maximum power supply noise estimation strategies on ISCAS85 benchmark circuits. Setting the population size at twice the critical primary inputs, the evolutionary algorithms will not stop until there have been no further improvements within 5 generations or the generation number reaches 50. All results are normalized to those of simple genetic algorithm method.

Figure 6 shows that the proposed algorithm improves power supply noise estimation on ISCAS85 benchmark circuits by 13.8% on average and 19.0% at maximum over the simple genetic algorithm. Since the proposed algorithm deploys a sharing scheme only on part of the primary inputs, it aims at more promising subspaces than a general sharing scheme in a niche genetic algorithm. The poor performance in C1908 is due to the fact that the difference between critical and minor primary inputs is not large enough, and therefore CPI-NGA degenerates to NGA.

It should be noted that the proposed algorithm has advantages in circuits with a large number of primary inputs and unbalanced critical factor distribution, which is the real case in many general designs. For example, C7552 has over 200 inputs and dramatically different critical factors. In this case, the niche genetic algorithm improves PSN estimation by only 8.1%, while the proposed algorithm achieves 19.0% improvement.

5　Conclusions

The power supply noise problem is becoming even more important with the continuous supply voltage scaling down in nanometer designs. In this

paper, a novel gate level model that captures both IR drop and di/dt noise and a primary input critical factor model that reflects the input's possible contribution to maximum power supply noise are proposed. Based on these models, an efficient estimation framework based on niche genetic algorithms is implemented. The proposed novel genetic algorithm improves the maximum power supply noise estimation by 13.8% in average cases and up to 19.0% in the best case over the simple genetic algorithm. The models and algorithm tools can be used to deal with reliability challenges in chip verifications. Future work will focus on deploying this method on power supply grid design and optimization.

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基于最大电源噪声门级模型的遗传算法电源噪声估计*

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摘要：提出一种能够综合考虑 IR drop 和 di/dt 噪声的门级电路模型. 实验表明，利用这种模型进行电源噪声估计，可以比传统模型提高 5.3%的精度，同时运算时间降低 10.7%. 根据输入信号对最大电源噪声的影响，还提出了关键输入信号模型. 实验表明，在进行电源噪声估计中，基于这些模型的遗传算法，能够比传统的遗传算法提高最多 19.0%的精度，并且收敛更加迅速.

关键词：电源噪声；门极模型；小生境遗传算法

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