Design and Implementation of an Optoelectronic Integrated Receiver in Standard CMOS Process*

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Abstract: A wideband monolithic optoelectronic integrated receiver with a high-speed photo-detector, completely compatible with standard CMOS processes, is designed and implemented in 0.6μm standard CMOS technology. The experimental results demonstrate that its performance approaches applicable requirements, where the photo-detector achieves a −3dB frequency of 1.11GHz, and the receiver achieves a 3dB bandwidth of 733MHz and a sensitivity of −9dBm for $\lambda = 850$nm at BER $= 10^{-12}$.

Key words: photo-detector; optoelectronic integrated receiver; CMOS; active inductor
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1 Introduction

In recent years, research of transceivers (non-optoelectronic integrated) based on CMOS has made much progress[1,2], where OC-192 chips (10Gb/s) have been obtained by 0.13μm CMOS technology[3]. But for considerations of cost reduction and performance improvement, much more attention should be attached to monolithic CMOS optoelectronic integrated receivers, because the cost of receiving modules and packaging will be significantly lowered, and the parasitic elements due to bonding pads and wires between the photo-detector and the receiving circuit will be eliminated if present optical receivers are integrated into single CMOS chips.

Much research about CMOS optoelectronic integrated receivers has been reported by foreign institutions. A 1Gb/s optoelectronic integrated receiver with a 0.04A/W responsivity and a −6dBm sensitivity for $\lambda = 850$nm in a 0.35μm standard CMOS process was first reported by Bell laboratory[4], and a 1Gb/s receiver with a 0.08A/W responsivity in a 0.1μm standard CMOS process was also presented in Ref. [5], but their sensitivity is far below the application requirement, which is usually less than −10dBm. Rooman *et al.*[6] reported a −18dBm optical receiver, but its data rate of 250Mb/s cannot satisfy high-speed requirements. For photo-receivers applicable in fiber communication systems, a 1Gb/s data rate and a 0.48 responsivity receiver at a sensitivity of −15.4dBm was obtained in Ref. [7], but too many modifications were made to the low-cost standard CMOS process. Reference [8] also reported a completely applicable optical receiver by utilizing an analog equalizer in a standard 0.18μm CMOS process, which achieves a 3Gb/s data rate and a −19dBm sensitivity for $\lambda = 850$nm. But the application of low-gain amplifiers and excessive equalizing devices sacrifices too much gain, signal to noise ratio (SNR), area and power. Furthermore, it seems that capacitors used in the analog equalizer are off-chip, which is inconsistent with monolithic integration.

Though short gate length processes can improve speed to some extent, they result in increased cost, lower junction depth and responsivity of photo-detector, and also decreased sensitivity. Therefore, we have designed and implemented a monolithic optoelectronic integrated receiver in a low-cost 0.6μm standard CMOS process to improve sensitivity and speed. The design of a high-

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speed photo-detector and the circuit-level design of a wideband receiver are presented, and the receiver is implemented.

2 Design of wideband CMOS optoelectronic integrated receiver

The limitations of optical receiver bandwidth can be broken into two components: intrinsic bandwidth of the photo-detector and circuit electrical bandwidth, where the former is related to the physical speed (that is limited by diffusion and drift of carriers) at which optically generated carriers are collected by the photo-detector, and the latter is mainly determined by the photo-detector's capacitance and the input impedance of the preamplifier. To acquire an applicable high-speed optical receiver operating at gigabits per second, a high intrinsic bandwidth photo-detector must be implemented first, which will be discussed in section 2.1. Then a high-sensitivity and wideband receiving circuit, which is needed for sensing and amplifying a photo-generated current signal, is given is section 2.2. The block diagram of the wideband optoelectronic integrated receiver system is shown in Fig. 1.

2.1 Design of high-speed photo-detector in standard CMOS process

In conventional n-well/p-substrate CMOS photo-detectors, the physical bandwidth is limited by the −3dB frequency of the p-substrate diffusion current, formed by the diffusion of carriers generated in the substrate which reach the junction many nanoseconds and several microseconds later. To eliminate the slow carriers' diffusion effect, a fingered dual-photodiode is designed[9], which is composed of an operation diode (n-well/p+) and a shield diode (n-well/p-substrate), as shown in Fig. 2. When the detector works, the shield diode is reversed. Therefore, the carriers generated in the substrate cannot diffuse to the zone of the operation diode and do not contribute to the current in the n-well/p+ junction. Furthermore, the pn junction depletion zone of the operation diode is maximized by the fingered p+ structure, which enhances the speed greatly. However, the elimination of slow carriers also costs much responsivity.

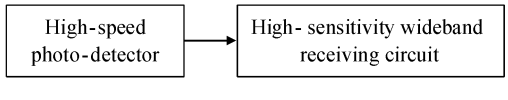

Fig. 1　Block diagram of the wideband optoelectronic integrated receiver system

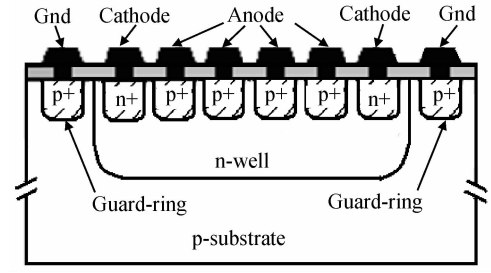

Fig. 2　Cross section of the fingered dual-photodiode

The designed fingered dual-photodiode is implemented in a CSMC 0.6μm CMOS process. Figure 3 is the experimental optic frequency response characteristic for a 40μm × 40μm fingered dual-photodiode, which achieves a −3dB frequency of 1.11GHz. The experimental results also indicate that the 40μm × 40μm photo-detector shows a 0.95pF junction capacitance and a 0.0378A/W responsivity.

2.2 Circuit design of wideband CMOS optoelectronic integrated receiver

Considering the low responsivity characteristic of the high-speed photo-detector, sensitivity improvement should be the main design point in the receiving circuit. Usually, it can be enhanced greatly by applying a high input impedance transimpedance amplifier, but this also contributes to a much bigger time constant because the photo-detector has a very large pn junction capacitance, which is the usual tradeoff between sensitivity and

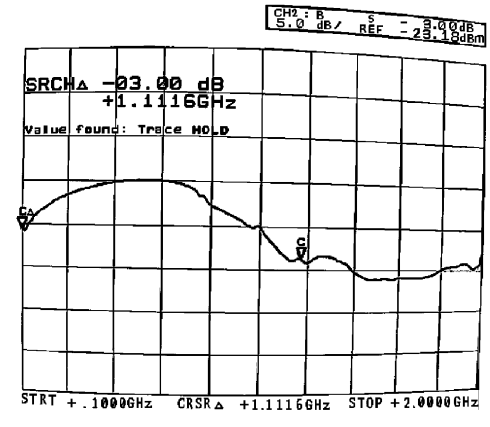

Fig. 3　Optic frequency response curve

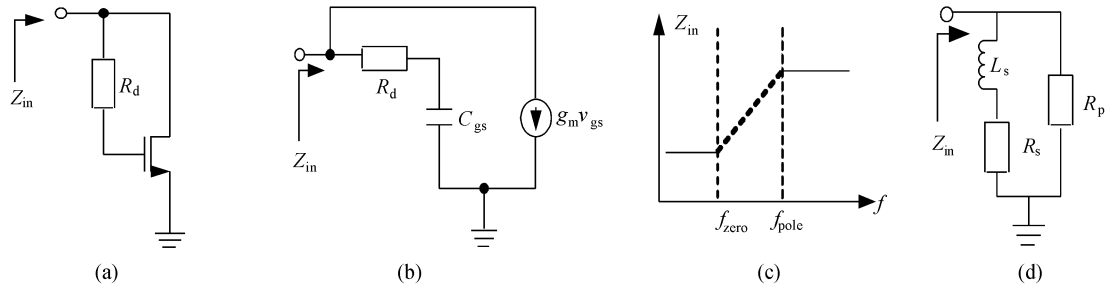

Fig. 4 A folded active inductor

bandwidth. To improve bandwidth, the inductive shunt peaking technique is generally applied[10,11]. Nowadays, an on-chip spiral inductor can be implemented in RFCMOS processes, which is provided by many semiconductor foundries. Compared to an off-chip inductor, an on-chip spiral inductor's performance is worse due to limitations of area and process, and its inductance value is usually less than tens of nanohenry, which is quite small and can only satisfy the requirements of high frequency circuits. In the domain of intermediate frequency, active inductors are generally used to replace spiral inductors for frequency compensation because they occupy much less area and achieve much higher inductance values.

The realization of a folded active inductor, composed of an nMOS transistor and a resistor[10], is shown in Fig. 4(a). Figure 4(b) is the small signal equivalent circuit of Fig. 4(a) when $f < f_T/2$ (f_T is the cut-off frequency of the MOS transistor). Figure 4(c) is the characteristic curve of the input impedance Z_{in} versus frequency. When $f_{zero} < f < f_{pole}$, Figure 4(b) is equivalent to Fig. 4(d), where $L_s = (C_{gs} R_d^2)/(g_m R_d - 1)$, $R_s = R_d/(g_m R_d - 1)$, and $R_P = R_d$.

The designed receiver with photo-detector and active inductor is shown in Fig. 5, which contains one transimpedance input stage, four amplifying stages and one output stage. In Fig. 5, I_s and C_d are the photo-generated current and the pn junction capacitance of the photo-detector, respectively, and they comprise the equivalent circuit of the photo-detector. In each amplifying stage, including the transimpedance input stage, an active inductor and parallel resonant peaking technique are applied to extend bandwidth, where

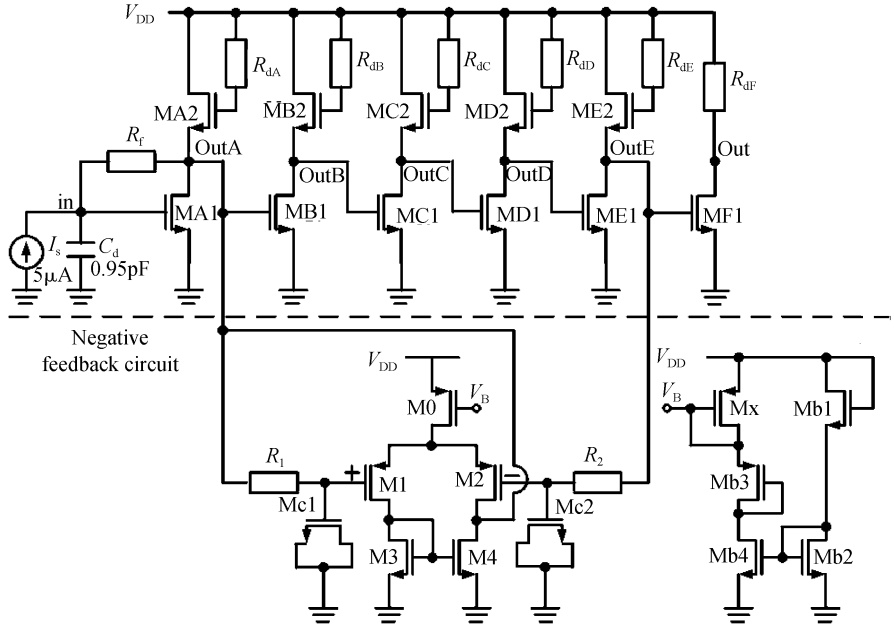

Fig. 5 A CMOS optoelectronic integrated receiver

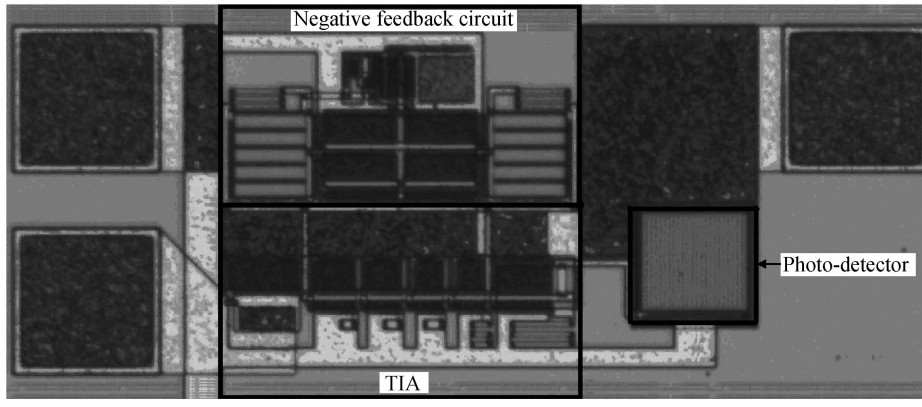

Fig. 6　Die photograph of the CMOS optoelectronic integrated receiver

the parallel resonant loop is comprised of an active inductor, an output resistor, and the input capacitor of the next stage, and the peaks formed in every stage intersect in the frequency domain to get maximal bandwidth. Furthermore, a direct current negative feedback technique is also applied to overcome the instability caused by temperature drift and supply power variation. The negative feedback circuit is shown as the part of the circuit below the dashed line in Fig. 5, where the circuit, comprised of Mx, Mb1, Mb2, Mb3 and Mb4, supplies bias voltage V_B.

3　Experiment results

The proposed CMOS optoelectronic integrated receiver has been implemented in a low-cost standard 0.6μm CMOS process. Figure 6 shows the die photograph, where a 40μm × 40μm fingered dual-photodiode designed in section 2.1 is applied and the supply voltage is 5V. The core area is 0.15mm^2.

Figures 7 and 8 are the simulated and measured frequency response characteristic curves, respectively, where the transimpedance gain in dBΩ equals the output voltage V_{out} in dB minus the photo-generated current I_s in dB. The measured results show that a 733MHz 3dB bandwidth is achieved where the input photo power is −5dBm at a wavelength of 850nm, which matches the simulated −3dB frequency demonstrated in Fig. 7. Figure 9 shows that the total equivalent input noise current at the input port is 626nA from zero up to −3dB frequency, which means a sensitivity of −9.4dBm can be achieved under the limitation of a 10^{-12} bit error rate (the calculation method of sensitivity is described in detail in Ref. [12]). The measured eye diagram has been depicted in Fig. 10 under −8dBm 1Gb/s input photo signal at 850nm wavelength, and the measured output signal amplitude is 163mV.

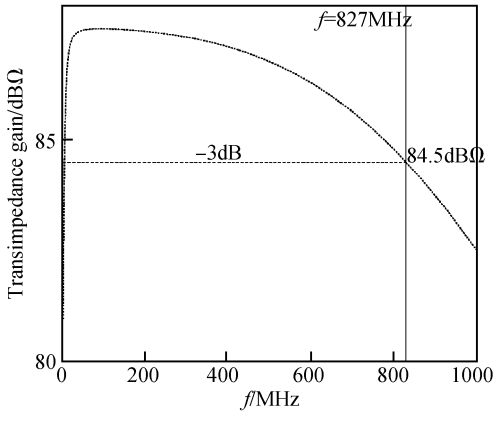

Fig. 7　Simulated transimpedance versus frequency characteristic

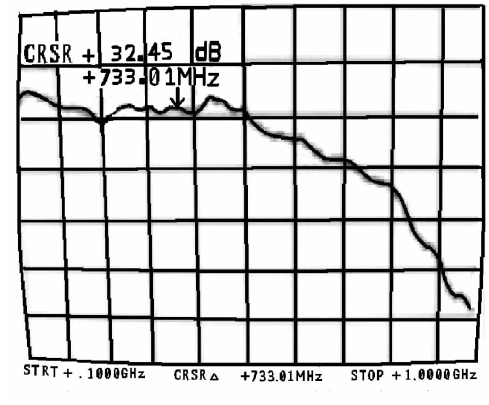

Fig. 8　Frequency response with −5dBm input photo power

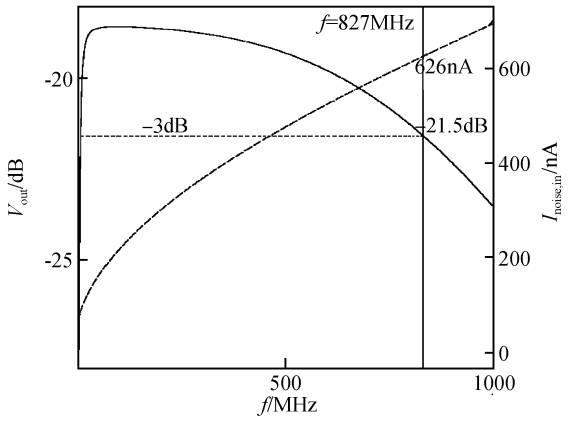

Fig. 9 Simulated output voltage and equivalent input noise current versus frequency characteristic

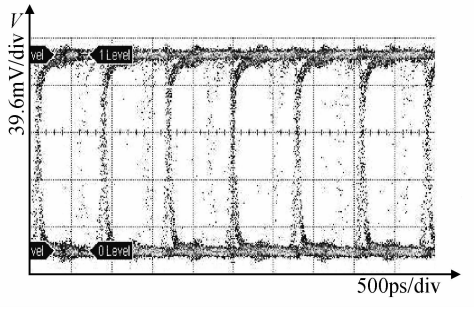

Fig. 10 Eye diagram for −8dBm 1Gb/s input photo signal

4 Conclusions

The integration of a photo-detector and a receiving and amplifying circuit in a single CMOS chip not only reduces the cost of the receiver effectively, but also greatly improves the performance of the receiver because of the elimination of parasitic capacitors and inductors caused by bonding pads and wires between the photo-detector and the receiving and amplifying module. This paper describes the design of an optoelectronic integrated receiver that is completely compatible with standard CMOS technology and the implementation of it in a CSMC 0.6μm standard CMOS process. The experimental results indicate that it achieves a 733MHz 3dB bandwidth and a −9dBm sensitivity for $\lambda = 850$nm at BER $= 10^{-12}$.

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一种与标准 CMOS 工艺兼容的光电集成接收机设计与实现*

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摘要：设计了一种与标准 CMOS 工艺完全兼容的高速光电探测器和宽带光电集成接收机，并采用 0.6μm 标准 CMOS 工艺流片.测试结果表明，该光电集成接收机的性能已接近实用要求.探测器的频率响应带宽为 1.11GHz，光电集成接收机的 3dB 带宽为 733MHz；在误码率为 10^{-12} 条件下，对波长为 850nm 的输入光信号，灵敏度达到 −9dBm.

关键词：光电探测器；光电集成接收机；CMOS；有源电感

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