CMOS Quadrature Modulator and Up-Conversion Mixer for 802.11a Wireless LAN Systems*

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Abstract: A quadrature modulator and an up-conversion mixer for an 802.11a wireless LAN system are designed and fabricated in 0.18μm gate length standard CMOS technology. A current feedback loop with a transconductor is used to improve the linearity of the quadrature modulator; An LC resonant tank is used as the load of the up-conversion mixer to improve its gain and increase the voltage swing. The measurement results show that the input P_{1dB} achieves -3.6dBm, the transducer power gain of the circuit is -3.6dB, and the current consumes about 45.8mA with a 1.8V power supply.

Key words: RFIC; CMOS technology; quadrature modulator; up-conversion mixer; Gilbert cell
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1 Introduction

Wireless LAN systems will evolve towards high data rate applications in the future. The IEEE 802.11a standard, which is based on orthogonal frequency division multiplexing (OFDM), provides nearly five times the data rate and ten times the overall system capacity as currently available 802.11b wireless LAN systems[1]. While radio frequency (RF) transmitters operate in the gigahertz range, a quadrature modulator is one of the key components. A CMOS analog quadrature modulator system using an analog four-quadrant multiplier and a phase shifter has been reported[2]. However, analog multipliers are difficult to realize using CMOS technology. A mixer is also an especially important building block in transceiver design because its dynamic range is often limited[3,4]. This paper introduces their basic designs. The designs are implemented in 0.18μm CMOS technology for the transmitter of an IEEE 802.11a system. The circuit contains two blocks: a quadrature modulator circuit and an up-conversion mixer, as shown in Fig. 1. The baseband I and Q signals are first mixed to 1GHz by a pair of image-rejected mixers, and then the quadrature 1GHz IF signal is converted to 5GHz by the up-conversion mixer (the divide-by-four circuit supplies 1GHz in-phase and quadrature signals).

2 Architecture and analysis of the quadrature modulator and up-conversion mixer

According to the IEEE 802.11a standard, the output power of the transmitter in the band of 5.15～5.35GHz must be lower than 40mW; In the 5.25 ～ 5.35GHz band, it must be lower than 200mW; And in the 5.725～5.825GHz band the maximal power is 800mW. The gain of the power amplifier is between 20 and 40dB. In the circuit,

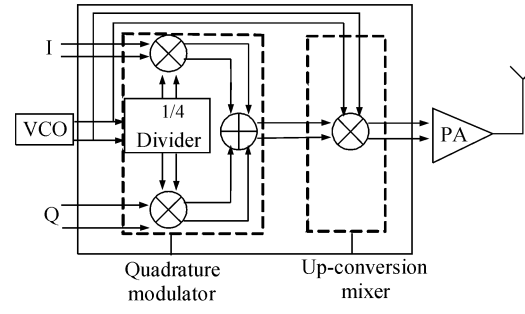

Fig. 1 Transmitter architecture of the WLAN IEEE 802.11a system

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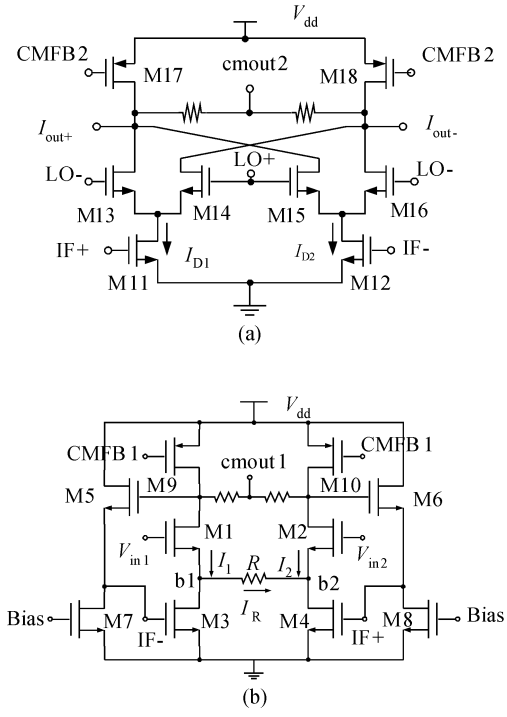

Fig. 2　Gilbert cell using current feedback loop transconductor stage　(a) Gilbert cell; (b) Transconductor stage

local oscillator (LO) signals are differential signals with frequency of 4GHz and voltage swing of about 400mV given by the VCO, and the voltage swing of the baseband I and Q signals is about 200mV. The output power of the up-conversion circuit we design is expected to be between −18 and 3dBm.

2.1　Quadrature modulator

The quadrature modulator shown in Fig. 1 consists of two identical modulators and a divide-by-four circuit. A schematic of one branch of the quadrature modulator (I/Q) is shown in Fig. 2. It includes the following circuit units: Gilbert cell, transconductor stage[5~7], and common mode feedback (CMFB) circuit.

The Gilbert cell is shown in Fig. 2(a). For its less harmonic and good port-to-port isolation, a double-balanced Gilbert cell is widely used in the mixers. Because the circuit is symmetric, the half-circuit method can be used to analyze its performance. For the single-balanced mixer, the output current can be derived as follows:

$$I_{D13} = K(V_{GS13} - V_{th})^2 \tag{1}$$

$$V_{GS13} = \sqrt{I_{D13}/K} + V_{th} \tag{2}$$

$$I_{D14} = K(V_{GS14} - V_{th})^2 \tag{3}$$

$$V_{GS14} = \sqrt{I_{D14}/K} + V_{th} \tag{4}$$

$$v_{LO} = V_{GS13} - V_{GS14} = (\sqrt{I_{D13}} - \sqrt{I_{D14}})/\sqrt{K} \tag{5}$$

As $I_{D13} + I_{D14} = I_{D1}$,

$$Kv_{LO}^2 = I_{D1} - 2\sqrt{I_{D13} I_{D14}} \tag{6}$$

$$4I_{D13} I_{D14} = (I_{D1} - Kv_{LO}^2)^2 \tag{7}$$

$$I_{out}^2 = (I_{D13} - I_{D14})^2 = (I_{D13} - I_{D14})^2 - 4I_{D13} I_{D14} = I_{D1}^2 - (I_{D1} - Kv_{LO}^2)^2 \tag{8}$$

Thus the output current can be expressed as (ignoring channel length modulation effect)

$$I_{out} = \sqrt{1 - (1 - \frac{v_{LO}^2}{I_{D1}/K})^2}\,\mathrm{sgn}(v_{LO})\, I_{D1} \tag{9}$$

where I_{D1} is the static current and $K = \mu_n C_{ox} W_n / 2L_n$.

If $V_{od} = V_{GS} - V_{th}$, $x = v_{LO}/V_{od}$, then one of the switch transistors will cut-off when $|x| > \sqrt{2}$, and thus the output current remains invariable. Therefore, when $v_{LO} \gg \sqrt{2}\, V_{od}$, M13 ~ M16 can be treated as switch transistors.

According to the above analysis, the output current of the double-balanced Gilbert mixer is given by

$$I_{out+} = I_{D1}\,\mathrm{sgn}(x) \tag{10}$$

$$I_{out-} = I_{D2}\,\mathrm{sgn}(x) \tag{11}$$

Obviously, because of the high order parasitics, the short-channel MOS no longer satisfies the square law of the long channel MOSFET, but the switch pairs are less sensitive to these effects than the transconductor. Therefore, the IIP3 of the Gilbert cell mixer is mainly determined by the IIP3 of the transconductors M11 and M12. In the circuit design, a current feedback loop is used to improve the linearity of the transconductor.

The transconductor stage is shown in Fig. 2(b). The input baseband signal is V_{in}, expressed as $V_{in} = V_{in1} - V_{in2}$. V_{gs1}, V_{gs2} are the gate-source voltages of M1 and M2. Then the source voltages of M1 and M2 are given by

$$V_{b1} = V_{in1} - V_{gs1} \tag{12}$$

and

$$V_{b2} = V_{in2} - V_{gs2} \tag{13}$$

The voltage of the resistor R can be expressed as

$$V_R = V_{b1} - V_{b2} = V_{in} - (V_{gs1} - V_{gs2}) \tag{14}$$

If $V_{gs1} - V_{gs2} = 0$, then $I_1 = I_2$, and the voltage of resistor R can linearly respond to the change of the input voltage. Thus the input signal V_{in1} is directly transferred to the resistor R, and the input

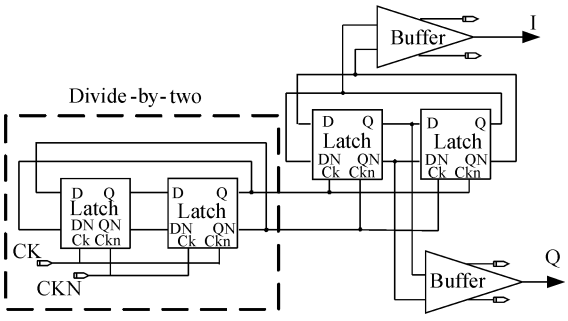

Fig. 3 Frame of divide-by-four

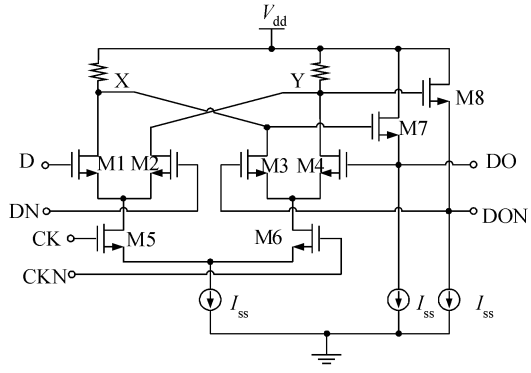

Fig. 4 One latch implemented with SCFL logic

signal voltage is translated into an input signal current $I_{in} = V_{in}/R$. Transistors M1, M3, M5, and M7 form a negative feedback loop to clamp the drain voltage of M3 in order to make the voltage of R linearly vary with the input voltage V_{in}. Through the current mirror M3, M4, M11, M12, a linear transconductance stage is formed.

Therefore, from Eqs. (10) and (11), the output current of the Gilbert cell is given by

$$\begin{aligned} I_{out} &= I_{out+} - I_{out-} = (I_{D1} - I_{D2})\mathrm{sgn}(x) \\ &= [(I_2 + I_R) - (I_1 - I_R)]\mathrm{sgn}(x) \\ &= 2I_R\mathrm{sgn}(x) = 2V_{in}\mathrm{sgn}(x)/R \end{aligned} \quad (15)$$

That is, the relation of I_{out} and V_{in} becomes linear.

Both the transconductor stage and the Gilbert cell use the CMFB circuit. There are two reasons for it: one is to supply a steady common mode (CM) level at the node of the output, and the other is to reduce the CM gain and improve the CMRR. In order to increase the dynamic output swing, the cascade of MOS between the power and the ground must be reduced. Therefore, the tail current is canceled in the Gilbert cell to increase the output swing, but this weakens the ability to restrict the CM signal. Thus, the CMFB circuit is used to compensate the drawback.

As for the divide-by-four circuit, it provides the in-phase and the quadrature signals of 1GHz, so its performance influences the I/Q mismatch directly. The circuit architecture of the divider is classified as the analog-divider and digital-divider. The structure, also called a Miller divider, operates at speeds exceeding half of the f_T of its constituent devices[8]. However, it will suffer from substantial phase noise and not supply the quadrature signals. As shown in Fig. 3, the divide-by-four circuit is composed of two divide-by-two units, which can be realized as two latches in a negative loop. One of the latches is shown in Fig. 4. M1 and M2, M3, and M4 are two differential pairs; when CK is high, M5 is "on" and M6 is "off", so D and DN transfer to DO and DON through M7 and M8, which function as source-followers. When CK is low, M3, M4 and M7, M8 constitute a DC feedback loop, and DO, DON are maintained. The buffers in the output commutate the signal and increase the drivability[9].

Considering the divide-by-two, its free frequency is set to half of the f_{CLK} while no clock signals working in order to reduce the loss.

2.2 Up-conversion mixer

In the front-end architecture, the cascade components influence the overall linearity. The overall IIP3 performance in the front-end is given by

$$\mathrm{IIP3} = \left[\frac{1}{\mathrm{IIP3}_1} + \frac{A_1^2}{\mathrm{IIP3}_2} + \frac{A_1^2 A_2^2}{\mathrm{IIP3}_3} + \cdots\right]^{-1} \quad (16)$$

The IIP3 magnitude and voltage gain of the n-th stage are given by $\mathrm{IIP3}_n$ and A_n, it shows that the linearity of the front-end is dominated by the ones located following the first stage of the front-end[3]. Consequently, the linearity of the whole circuit could be improved by enhancing that of the up-conversion mixer based on some gain. Resistive degeneration (depicted in Fig. 5) of the differential pair V-to-I converter improves mixer linearity[10], and indeed, the available dynamic range, at the expense of a higher noise figure which can be ignored in the up-conversion mixer.

As shown in Fig. 5, the core of the up-conversion mixer is also the Gilbert cell. But it is between the quadrature modulator and the power amplifier, and accordingly, it is easily interfered

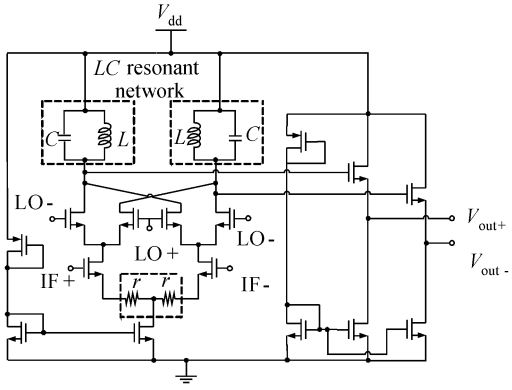

Fig. 5　Up-conversion mixer

with by the odd harmonic and the intense signals. In addition, since the output frequency of the up-conversion mixer is over 5GHz and the power supply is 1.8V, the output swings will decrease if pMOS or resistors are used as the load. Thus, an *LC* tank is used as the load in the Gilbert cell of the up-conversion mixer.

Because of the frequency selectivity characteristic of the load using the *LC* tank, not only does are the output voltage swings of the Gilbert cell and the gain of the up-conversion mixer improved at a frequency of 5GHz, but other odd high-frequency harmonics are also suppressed. The gain of the resonant network achieves the maximum at a frequency of 5GHz, and at the same time the frequency selectivity of the system is better.

However, the *LC* tank will consume more chip area, and a high *Q LC* tank is hard to achieve in CMOS technology due to large parasitics in the substrate.

In CMOS, the LO signal is more easily fed through the substrate into the output. Thus, the port-to-port isolation will be the most important part to consider.

3　Realization and measurement

3.1　IC fabrication

The circuit has been realized in a standard 0.18μm CMOS technology of TSMC. A chip microphotograph is shown in Fig. 6, which is completely symmetrical. The chip die size is 0.944mm $\times$0.995mm.

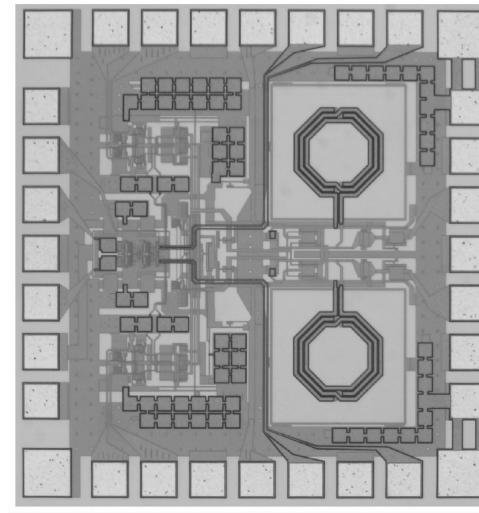

Fig. 6　Microphotograph of the circuit

3.2　Measurement

The quadrature signals are supplied by an Agilent E4438C, and the output spectrum of the modulated signals is measured by an Agilent E4440A. As shown in Fig. 7, while the spectrum should be a single side-band (SSB) modulated spectrum, the results show another side-band, which is because the signal source provides the quadrature and the differential signals have some mismatch. In addition, the measurement on bonding should increase the loss that has not been added to the results.

Even then, as Fig. 8 depicts, the following measurement results are achieved: The P_{1dB} (input 1dB compression point) is as high as -3.6dBm, the transducer power gain is -3.6dB, and the port-to-port isolation is less than -51dBm. The circuit consumes 45.8mA of current with a 1.8V

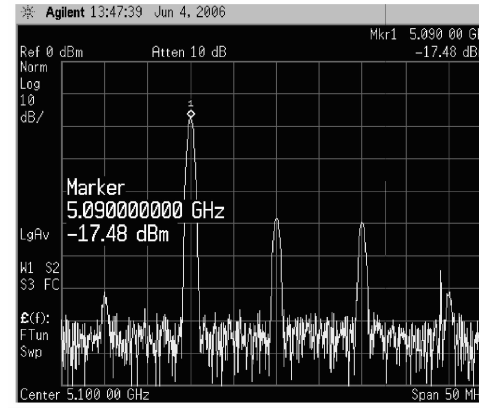

Fig. 7　Output spectrum of the mixer

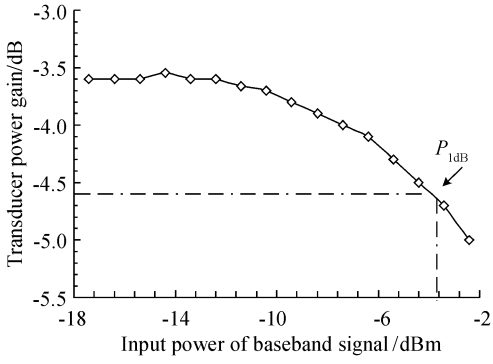

Fig. 8 Measurement of P_{1dB}

power supply. The measurement results accord with the performance we expected.

4 Conclusions

As depicted in the measurement results, the CMOS quadrature modulator and up-conversion mixer accomplished with differential pairs are designed successfully. For the behaviors of the circuit exhibiting a high performance, with relatively high linearity (P_{1dB} as high as -3.6dBm) and some transducer power gain, it could be suitable for WLAN applications.

References

[1] Zargari M, Su D K, Yue C P, et al. A 5-GHz CMOS transceiver for IEEE802.11a wireless LAN systems. IEEE J Solid-State Circuits, 2002, 37(12): 1688

[2] Song B S. CMOS RF circuits for data communications applications. IEEE J Solid-State Circuits, 1986, sc-21(2): 310

[3] Sullivan P J, Xavier B A, Ku W H. Low voltage performance of a microwave CMOS Gilbert cell mixer. IEEE J Solid-State Circuits, 1997, 32(7): 1151

[4] Chi Baoyong, Shi Bingxue. CMOS mixers for 2.4GHz WLAN transceivers. Chinese Journal of Semiconductors, 2003, 24(5): 472

[5] Orsatti P, Piazza F, Huang Q. A 20-mA-receive, 55-mA-transmit, single-chip GSM transceiver in 0.25-μm CMOS. IEEE J Solid-State Circuits, 1999, 34(12): 1869

[6] Liu T P, Westerwick E. 5-GHz CMOS radio transceiver front-end chipset. IEEE J Solid-State Circuits, 2000, 35(12): 1927

[7] Cui Fuliang, Ma Dequn, Huang Lin, et al. Low voltage CMOS Gilbert mixers for bluetooth transceiver. Chinese Journal of Semiconductors, 2004, 25(9): 1066

[8] Razavi B. RF microelectronics. Upper Saddle River, New Jersey: Prentice Hall PTR, 1998

[9] Dou Jianhua, Qian Liwang, Wang Zhigong, et al. Static frequency divider circuit design using 0.6μm standard CMOS process. Journal of Electronic Education, 2004, 26(1): 35(in Chinese)[窦建华, 钱立旺, 王志功, 等. 0.6μm CMOS 静态分频器电路设计. 电气电子教学学报, 2004, 26(1): 35]

[10] Li Q, Yuan J S. Linearity analysis and design optimization for 0.18μm CMOS RF mixer. IEEE Proc-Circuits Syst, 2002, 149(2): 112

基于 802.11a 标准的 CMOS 正交调制器和上变频器*

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摘要: 采用 0.18μm CMOS 工艺, 设计并实现了应用于 WLAN IEEE 802.11a 的正交调制器和上变频器. 正交调制器在传统的 Gilbert 单元基础上, 采用负反馈跨导放大器来提高线性度; 上变频器采用 LC 谐振网络作混频器负载来提高增益和电压输出摆幅. 测试结果表明, 在 1.8V 电源电压下, 谐振频率点的 1dB 压缩点 P_{1dB} 为 -3.6dBm, 功率转换增益为 -3.6dB, 电流消耗大约 45.8mA.

关键词: 射频集成电路; CMOS 工艺; 正交调制器; 上变频器; Gilbert 单元

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