A High Voltage BCD Process Using Thin Epitaxial Technology *

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Abstract: A high voltage BCD process using thin epitaxial technology is developed for high voltage applications. Compared to conventional thick expitaxial technology, the thickness of the n-type epitaxial layer is reduced to 9μm, and the diffusion processing time needed for forming junction isolation diffusions is substantially reduced. The isolation diffusions have a smaller lateral extent and occupy less chip area. High voltage double RESURF LDMOS with a breakdown voltage of up to 900V, as well as low voltage CMOS and BJT, are achieved using this high voltage BCD compatible process. An experimental high voltage half bridge gate drive IC using a coupled level shift structure is also successfully implemented, and the high side floating offset voltage in the half bridge drive IC is 880V. The major features of this process for high voltage applications are also clearly demonstrated.

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1 Introduction

The bipolar CMOS DMOS (BCD) process, which was introduced twenty years ago, is an important mixed technology that allows the integration on a single chip of bipolar linear, CMOS logic, and double-diffusion MOSFET (DMOS) power functions[1,2]. In recent years, the multiple discrete components in high voltage IC applications have been reduced through their integration into a BCD process. The integration of discrete elements provide improved performance, increased functionality, enhanced reliability, and compact solutions for applications in consumer, automotive, motor control, switched mode power supplies and medical use[3~7].

In this paper, a high voltage BCD process using thin epitaxial technology is realized for high voltage applications. High voltage double reduced surface field (RESURF) lateral double-diffusion MOSFET (LDMOS) with a breakdown voltage of up to 900V, as well as low voltage CMOS and npn-type BJT, are realized in this high voltage 1P1M (one poly one metal) BCD process. Compared to our previous work[8~10], the thickness of the n-type epitaxial layer is reduced from 23 to 9μm, and the up-and-down diffusion processing time needed for forming junction isolation diffusions is substantially reduced with this thin epitaxial technology. The isolation diffusions have a smaller lateral extent and take up less chip area, so the chip cost is improved. An As-bury layer mask is added in order to increase high side punch-through voltage and avoid the CMOS latch-up effect for inductive load applications, and a p-well is used as down diffusion for forming junction isolation diffusion with p-bury. Using this 1P1M high voltage BCD process, an experimental half bridge gate drive IC using a coupled level shift structure is also successfully implemented, and the high side floating offset voltage in the half bridge drive IC is 880V.

2 Device structures and process

A schematic cross section of the principal de-

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vices is shown in Fig. 1. Double RESURF LDMOS is adopted in this process, and the breakdown voltage of the LDMOS is 900V. For higher voltage, a higher substrate doping concentration is very important. The breakdown voltages of the low voltage nMOS and pMOS are 21 and −22V, respectively. To achieve nMOS and pMOS with a breakdown voltage of more than 25V, a lightly doped drain (LDD) or a double-diffused drain (DDD) structure is used. An npn type BJT is also available in this BCD process. A p-well or p-top can be used to form the p-base region of the npn, which provides two BJTs with different performances. The p-well and the p-bury form the junction isolation through the up-and-down diffusion for different voltage applications. An As-bury layer is used to increase high side punch-through voltage and avoid the CMOS latch-up effect. Circuit integration is accomplished through a combination of junction isolation for the LDMOS, bipolar and CMOS device epitaxial islands and self-isolation between CMOS devices for high density integration.

The process flows of the designed high voltage BCD process are shown in Table 1. The BCD process starts on p-type silicon, where buried layers of boron and arsenic are applied by implantation. After the growth of a 9μm thick n-type epitaxial layer, p-well and p-top are implemented by implantation and drive-in, then the junction isolations are formed by p-well and p-bury. The high pressure oxidation technology is used to form the active region, and the thickness of the field oxide is about 1400nm. Then an 80nm gate oxide is grown, the polysilicon is deposited, doped, and patterned, and thus the poly electrode can be shaped. This is followed by masked implantation of an n-type S/D and a p-type S/D. Subsequently, pre-metal dielectric (PMD) is deposited, in which contact windows are defined. Finally, Al-Si-Cu is deposited and patterned, and a passivation layer is applied.

Table 1　Process flows of the designed BCD process

1. p-type silicon
2. p-bury layer and As-bury layer formation
3. Epitaxial growth
4. p-well and p-top formation
5. LOCOS formation
6. Gate formation
7. LDD or DDD formation
8. S/D formation
9. Contact
10. Metallization
11. PAD

3　Results and discussion

3.1　High voltage LDMOS

The high voltage double RESURF LDMOS, shown in Fig. 1, is realized using this high voltage BCD process. The thickness of the n-type epitaxial layer is reduced, and the p-top layer is introduced for forming a double RESURF device. The p-well and p-bury form the isolation well for different voltage applications, and self-isolation LDMOS can be achieved. Two-dimensional simulations are implemented by MEDICI[11]. Figure 2 (a) shows the simulated breakdown voltage in relation to the concentration of the n-type epitaxial layer. Figure 2 (b) shows the simulated breakdown voltage in

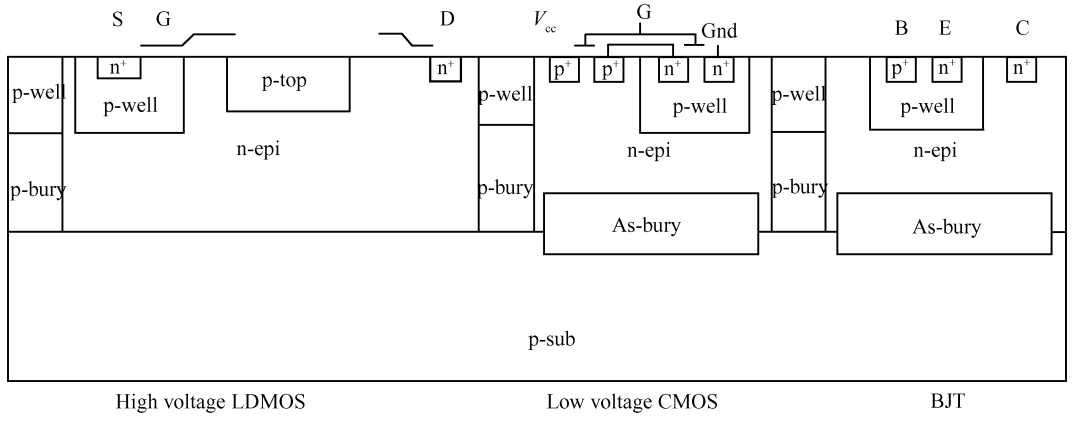

Fig. 1　Schematic cross section of the principal devices

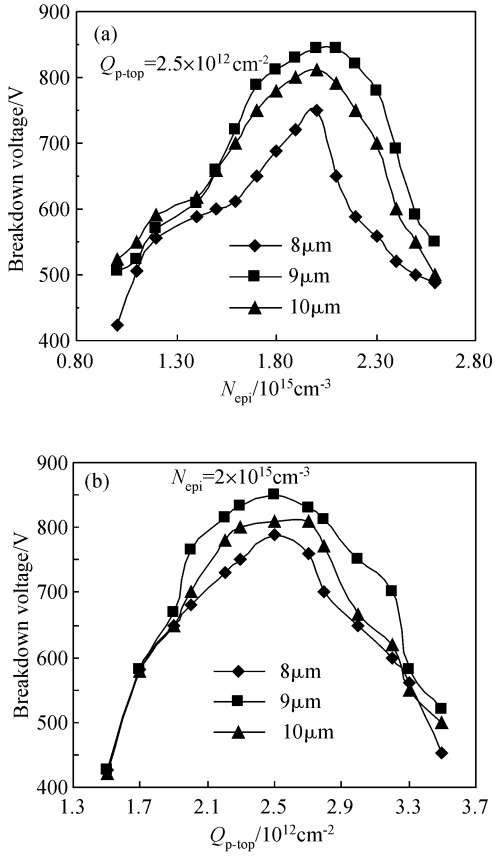

Fig. 2 (a) Breakdown voltage in relation to the concentration of the n-type epitaxial layer; (b) Breakdown voltage in relation to the implant dose of the p-top layer

relation to the implant dose of the p-top layer. As can be seen from Fig. 2, the optimum parameters for 9μm epitaxial layer are that the concentration of the n-type epitaxial layer is around 2×10^{15} cm^{-3}, and the implant dose of the p-top layer is 2.5×10^{12} cm^{-2}. Figure 3 shows the microphotograph and the experimental breakdown curve of

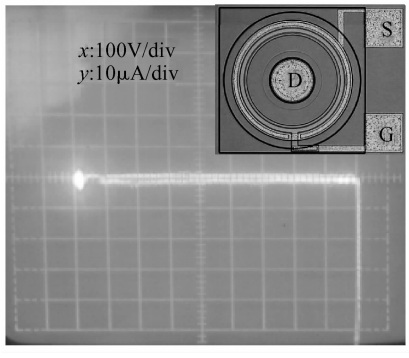

Fig. 3 Microphotograph and experimental breakdown curve of the high voltage double RESURF LDMOS

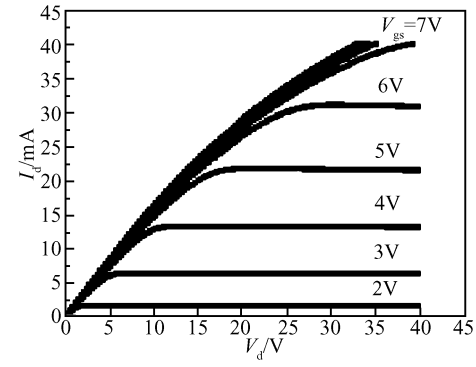

Fig. 4 I_d-V_d curves of the high voltage double RESURF LDMOS

the designed high voltage double RESURF LDMOS. The breakdown voltage of the LDMOS is 900V, and the leakage current is very small before the breakdown occurrence of the LDMOS. Figure 4 shows the measured output curves of the high voltage double RESURF LDMOS.

3.2 Low voltage CMOS

The cross-sectional views of the low voltage nMOS and pMOS, fabricated by this high voltage BCD process, are also shown in Fig. 1. The low voltage pMOS is realized in the n-type epitaxial layer, which is simultaneous with the drift region of the high voltage double RESURF LDMOS. The low voltage nMOS is fabricated in the p-well, which is simultaneous with the channel region of the high voltage LDMOS formed by boron implantation and drive-in. The threshold voltages of the MOS devices are 1.3V for nMOS and −1.3V for pMOS. The breakdown voltages are 21V for nMOS and −22V for pMOS. The measured output curves of the low voltage nMOS and pMOS are shown in Fig. 5 and Fig. 6, respectively. To achieve nMOS and pMOS with the breakdown

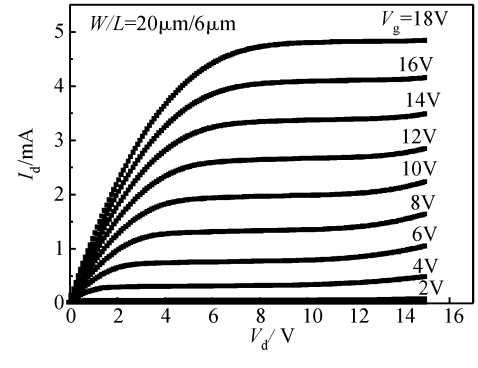

Fig. 5 I_d-V_d curves of the low voltage nMOS

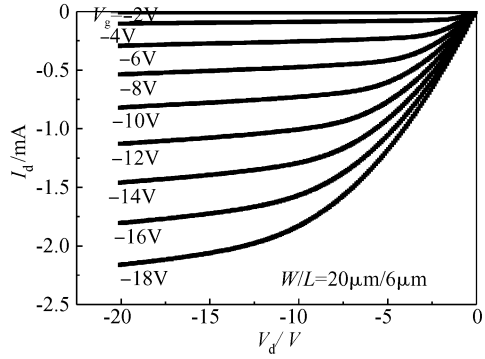

Fig. 6　I_d-V_d curves of the low voltage pMOS

voltage of above 25V, an LDD or DDD structure can be used. The threshold voltages of the MOS devices are 1.3V for the LDD nMOS and −1.3V for the LDD pMOS. The breakdown voltages are 28V for the LDD nMOS and 42V for the LDD pMOS.

3.3　Low voltage BJT

An npn-type BJT is also fabricated using this high voltage BCD process. The doping and the junction depth of the base region will affect the current gain and the breakdown voltage. A p-well or p-top can be used to form the p-base region of the npn, which provides two BJTs with different performances. The emitter and collector regions are formed using the implantation of n-type S/D. Figure 7 shows the I_c-V_{ce} curves of the low voltage BJT with the p-well base region and the p-top base region. Figure 7 shows that the npn-type BJT is rated to operate at more than 20V, which is the typical maximal requirement for gate drive voltage.

4　Application

Many integrated circuits are possible with the presented 600V thin epitaxial BCD process. One of the most important applications for this process is for power control circuits. Therefore the CMOS and bipolar devices are rated to operate at up to 20V, which is typically required for the maximum gate drive voltage of power MOSFET or IGBT. Thus, the nMOS and pMOS with LDD or DDD structures must be used in the power control circuit design. Figure 8 shows a schematic diagram of a typical high voltage half bridge drive IC designed by us. The logic input signal is compatible

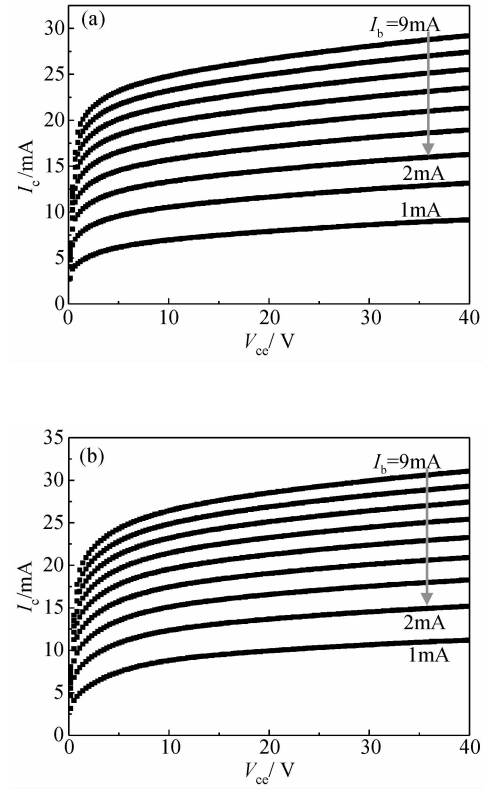

Fig. 7　I_c-V_{ce} curves of the low voltage BJT with p-well base region (a) and p-top base region (b)

with 3.3, 5, and 15V. The dead-time circuit prevents the synchronous conduction of the high side and low side power MOSFET or IGBT. Two double RESURF LDMOS devices used for level shift are controlled by pulse signals generated from the pulse-generation circuit. Figure 9 shows the microphotograph of the high voltage half bridge drive IC developed with this high voltage thin epitaxial BCD process. Two LDMOS devices using coupled level shift structures are adopted for transferring low voltage logic signals to high voltage control parts[10], and high side circuit and low side circuit are in different epitaxial islands. Table 2 shows the main measured results of the IC realized in the presented BCD process. The high side floating offset voltage (V_s) in the half bridge drive IC is 880V using a coupled level shift structure, and the detrimental effect of the high voltage interconnection metal line can be avoided[9,10]. The gate drive supply range is from 10 to 20V. The undervoltage lockout circuit will turn off the gate drive if V_{CC} is below 6.55V. This protects the power MOSFET or IGBT from going into a high dissipation mode. The output currents of the circuit are

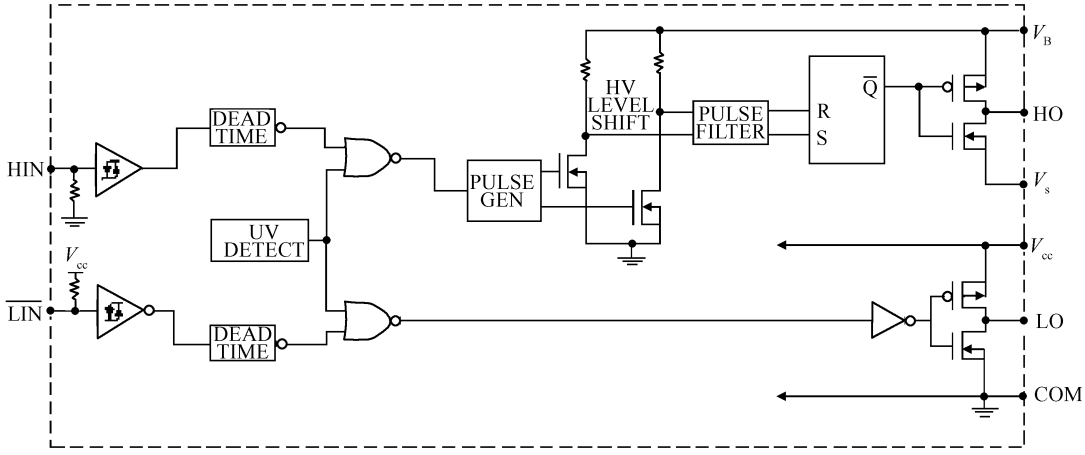

Fig. 8 Schematic diagram of a typical high voltage half bridge drive IC

420mA for nMOS and 210mA for pMOS when V_{CC} = 15V. The quiescent V_{CC} supply current (I_{QCC}) is 220μA, and the quiescent V_{BS} supply current (I_{QBS}) is smaller than 1μA.

5 Conclusions

A high voltage BCD process using thin epitaxial technology has been developed for high voltage applications. High voltage double RESURF LDMOS with a breakdown voltage of up to 900V, as well as low voltage CMOS and npn-type BJT, have been achieved using this high voltage 1P1M BCD process. An experimental high voltage half bridge gate drive IC using a coupled level shift structure is also successfully implemented.

Table 2 Measured results of the high voltage half bridge drive IC

V_{OFFSET}	880V	$I_O^{+/-}$	210mA/420mA
V_{CCUV-}	6.55V	V_{CCUV+}	7.45V
Deadtime	1.15μs	V_{OUT}	10～20V
I_{QCC}	220μA	I_{QBS}	＜1μA

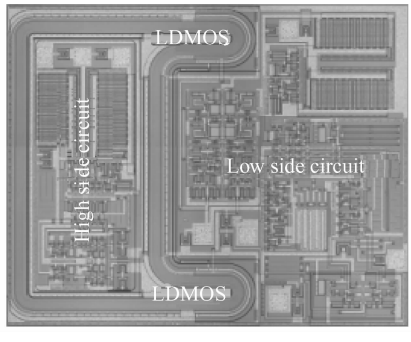

Fig. 9 Microphotograph of the high voltage half bridge drive IC

The high side floating offset voltage of the designed IC is 880V, and the detrimental effects of the high voltage interconnection metal line can be almost ignored with this high voltage 1P1M BCD process. The process technology enables monolithic solutions for a wide range of applications. The major features of this process for high voltage applications have been clearly demonstrated.

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基于薄外延技术的高压 BCD 兼容工艺*

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摘要：针对高压应用领域，开发了一种基于薄外延技术的高压 BCD 兼容工艺，实现了 900V 高压双 RESURF LDMOS 与低压 CMOS，BJT 器件的单片集成. 与传统厚外延技术相比，工艺中 n 型外延层的厚度减小为 9μm，因此形成 pn 结对通隔离的扩散处理时间被极大减小，结隔离有更小的横向扩散，节约了芯片面积，并改善了工艺的兼容性. 应用此单层多晶、单层金属高压 BCD 兼容工艺，成功研制出一种基于耦合式电平位移结构的高压半桥栅极驱动电路，电路高端浮动偏置电压为 880V.

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