A Ka-Band PHEMT MMIC 1W Power Amplifier*

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Abstract: The performance of a microwave monolithic integrated circuit (MMIC) amplifier with high output power in the Ka-band is presented. Using 75mm 0.25μm GaAs PHEMT technology provided by the Hebei Semiconductor Research Institute, this three-stage power amplifier, with a chip size of 19.25mm^2 (3.5mm × 5.5mm), on 100μm GaAs substrate achieves a linear gain of more than 16dB in the 32.5～35.5GHz frequency range, with an average output power at 1dB gain compression of P_{1dB} = 29.8dBm and a maximum saturated output power of P_{sat} = 31dBm.

Key words: Ka-band; power amplifier; PHEMT; MMIC
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1 Introduction

Millimeter-wave monolithic integrated power amplifier circuits are key components in future communication and smart munitions applications that require components that have light weight, good reliability, high volume, and low cost. High output power and other good properties have been demonstrated by a number of microwave monolithic integrated circuit (MMIC) amplifiers[1～5]. Excellent gain and efficiency performance have been achieved due to the recent developments of pseudomorphic high electron mobility transistor (PHEMT) technology at millimeter-wave frequency. This paper describes the development of a Ka-band 1W power MMIC amplifier that has a peak gain of 11dB at 34.5GHz, a gain higher than 10dB, and a power added efficiencies (PAE) higher than 15% in the 32.5 to 35GHz frequency range.

2 PHEMT process technology

The amplifier MMIC was fabricated using a 0.25μm gate-length PHEMT process on 75mm wafers, which are epitaxial wafers fabricated by MBE. The T-gate definition was obtained by electron-beam lithography. This process provides high gain and high current density, which are necessary for efficient power amplification. The etch stops result in uniformity and high yield. The circuits utilize 80μm-thick substrates, 50Ω/□ TaN thin film resistors, and 330pF/mm^2 MIM silicon nitride capacitors.

3 Device model

Statistically average linear and nonlinear device models were developed to meet the high volume production requirements for systems. Extensive DC and RF measurements were done over different bias conditions under both active and cold FET conditions[6]. Figure 1 shows the modified Materka large signal equivalent circuit[7]. Aimed at the effects of traps and self-heating caused by the current dispersion of the drain and source, Gao *et al*.[8] extracted a large signal model through taking some measurements of the gate current of a pulse, the drain current of a pulse, modified cold S parameters, and S parameters about the load line. The benefit of conducting step by step measurements and extractions was to reduce the number of extractions and also to enhance the precision. We verify the measurements of the gate current of a pulse, the drain current of a pulse, modified cold S parameters, and S parameters about the load line. The benefit of conducting step by step measurements and extractions

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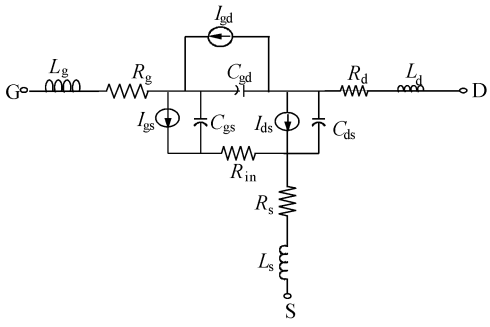

Fig. 1 Modified Materka large signal equivalent circuit

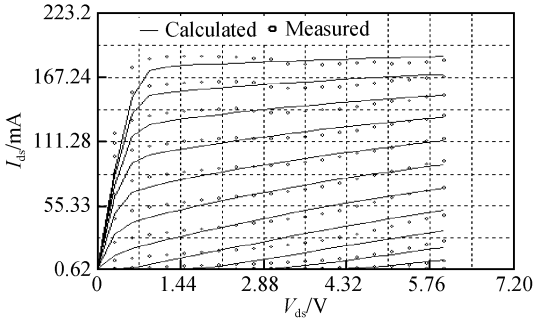

Fig. 2 DC-IV curves of the 400μm device

was to reduce the number of extractions and also to enhance the precision. We verify the foundry model by some tests. The pulsed DC-IV data were fitted by the modified Materka nonlinear model equations, as shown in Fig. 2. Figures 3 and 4 show a comparison of the small signal-parameters obtained from the nonlinear model at low power input bias of V_{ds} = 5V and I_{ds} = 60mA.

4 Circuit design

The amplifier was designed by utilizing small

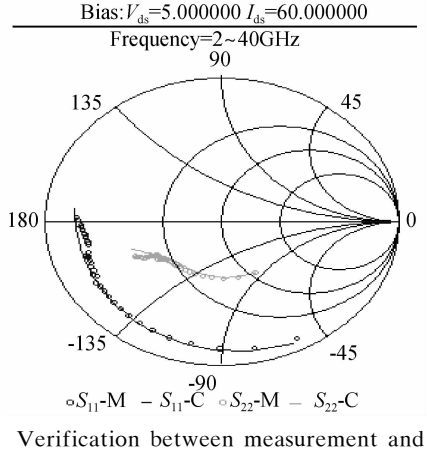

Fig. 3 Verification between measurement and calculation of S_{11} and S_{22}

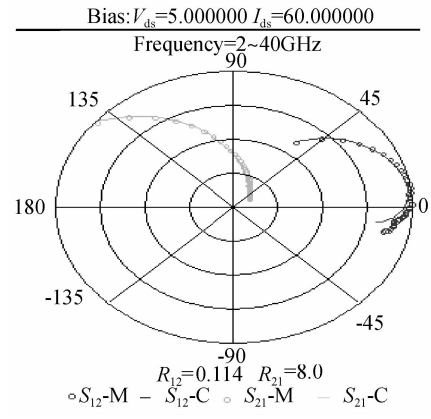

Fig. 4 Verification between measurement and calculation of S_{12} and S_{21}

signal models, optimum load, and optimum source data. The matching networks for input, interstage, and output of the amplifier were designed considering small signal response and power transfer to the optimum source or load impedance simultaneously[2]. After examining the power gain and the output power of the circuit, the periphery of the PHEMTs for each stage is $2 \times 400\mu$m, $4 \times 400\mu$m, and $8 \times 480\mu$m, respectively, with 0.25μm gate length. Prior to optimizing the circuit, appropriate matching topologies and passive structures were selected. The topology structure of the whole amplifier, including the first two driver stages and the output power stage, is shown in Fig. 5.

Recognizing that problems can arise due to inadequate bias line isolation, several decoupling structures were developed with increasing current handling capability[5]. Gate and drain bias networks employed MIM capacitors and parallel resistors with slot vias placed closer to the matching circuit side to maintain high isolation from 10 to 50GHz. In the first stage, a high and low impedance structure was developed to reduce the influ-

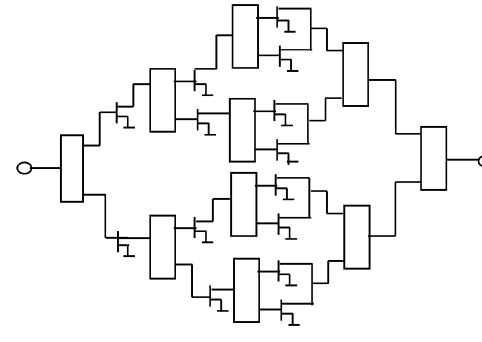

Fig. 5 Topology of the power amplifier

ence between bias and the primary transmission lines. The extended stubs with resistor in the output stage could flatten the output power. Considerable effort was expended on making sure the amplifier was stable. Some of the schemes that were used here include resistor termination, inductive gate matching networks, series parametric oscillation suppression resistors (implemented in ohmic metal), open stubs with resistors to reduce out-of-band gain, parallel structure with resistor and MIM capacitor for stability, and odd mode resistors for odd mode stability enhancement. Finally, all the bias lines carrying considerable current were analyzed for voltage drop and decreased for electron migration, especially for the third drain line.

5　MMIC description

The three-stage MMIC PA consists of two 400μm cells that drive four 400μm cells and then drive the output-stage eight 480μm cells for a total gate periphery of 3840μm. The matching networks for the amplifier were designed considering small signal response and power transfer to the optimum source or load impedance simultaneously. The first step in the design process is to design the output matching network to transfer maximum output power from PHEMTs to the 50Ω film[5]. The micro-strip line-width is sized appropriately for current handling and constrained during the optimization. MIM capacitors are used in several places to capacitively load transmission lines and reduce their length as well as to provide some impedance transformation. Also the power capability of the capacitors will be considered. The aim of the output network is optimized for matching to the optimum load of the device. The second step in the design process is to design the inter-stage networks to match the output of the driver stage to the input of the power stage in order to lower the mismatch loss. This network is a compromise between small signal gain and large signal power transfer. As a rule, the drain of the first stage is poorly matched to the optimum load, and the inter-stage must have a good gain match to insure that the output stage reaches saturation. The final step in the initial design process is to design the input network. This network provides a perfect match at 34GHz for maximum gain and increases mismatch towards the low end of the band to provide some gain slope compensation, since the amplifier is intended for use in a balanced configuration. After the initial design of the three networks is completed, these are optimized to account for the non-unilateral characteristic of the large transistor periphery. During this process, stability is analyzed, and the resistor and MIM capacitor values are adjusted. Since dimensions were constrained appropriately in the design process, changes were reduced during the layout process. Based on these essential matching networks, an optimization and EM simulation were performed to achieve the required circuit performance. Figure 6 shows a photograph of the power amplifier.

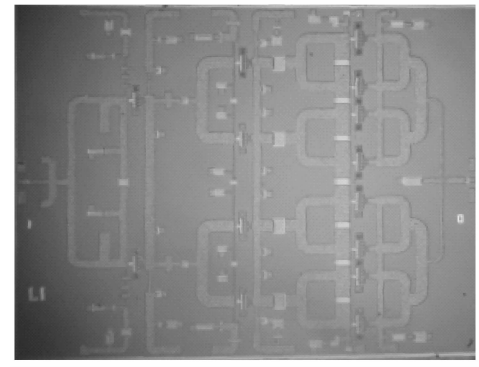

Fig. 6　Photograph of the power amplifier (3.5mm × 5.5mm)

6　Measurement result

The MMIC amplifier was tested using a continuous wave (CW) signal for small signal S parameters. Figure 7 shows the small signal power gain and the input return loss of the MMIC amplifier into a 50Ω system measured with an Anritsu 54169A network analyzer using a self-made test tong. The setup was calibrated with a SOLT calibration. The highest power gain of the MMIC was obtained for an amplifier bias of V_d = 5V and I_{ds} = 1.4A. In the 32.5 to 35.5GHz frequency range, the small signal power gain of the MMIC was measured to be more than 16dB, the input return loss was estimated to be 10dB, and the 1dB gain compression output power was measured at V_d = 5～6V and I_{ds} = 1.4A, as shown in Fig. 8.

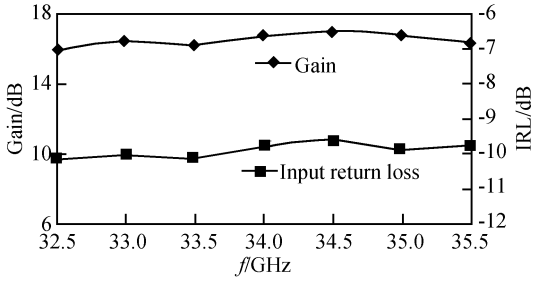

Fig. 7 Measurement of the chip in the fixture for small signal power gain and input return loss

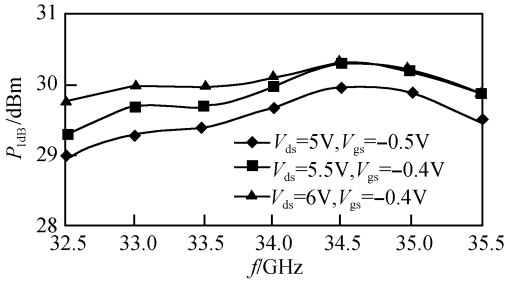

Fig. 8 Measured P_{1dB} of the test fixture Ka-band PA at 32.5～35.5GHz

The input power versus output power characteristic of the MMIC power amplifier at 34GHz measured into a 50Ω system is shown in Fig. 9. The maximum output power of the MMIC amplifier was measured at $V_d = 6V$. Figure 10 shows the saturation output power of the MMIC amplifier above 30dBm from 33.5 to 34.5GHz. The PAE of P_{1dB} and P_{sat} in the 33.5 to 34.5GHz range are all above 15%, as shown in Fig. 11.

7 Conclusions

This paper reports the first domestic realization of a Ka-band MMIC power amplifier with a maximum saturation output power above 31dBm, using 75mm 0.25μm GaAs PHEMT technology provided by the Hebei Semiconductor Research Institute. Its output power, bandwidth, and efficiency are superior to the previously domestic reported results.

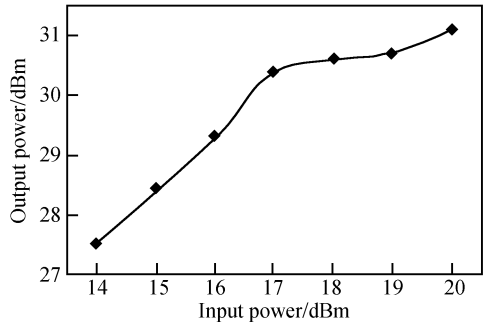

Fig. 9 Output power versus input power at 34GHz input power from 14 to 20dBm

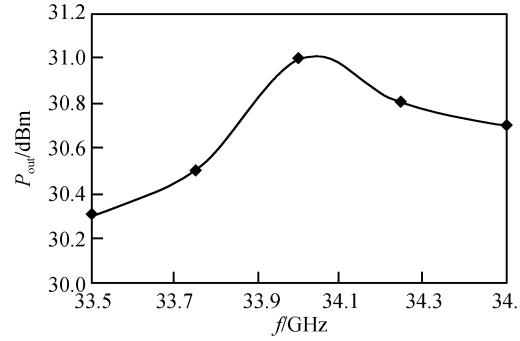

Fig. 10 Saturation power from 33.5 to 34.5GHz

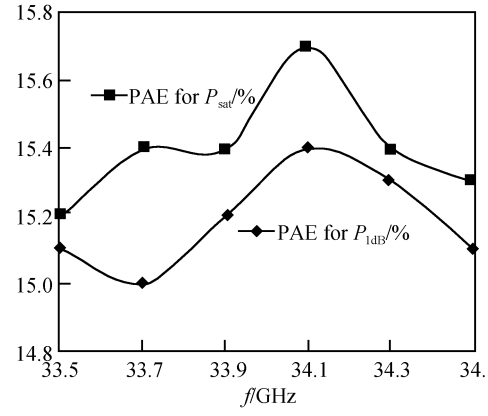

Fig. 11 PAE of P_{1dB} and P_{sat} at 33.5 to 34.5GHz

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Ka 频段 PHEMT 1W 功率单片放大器*

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摘要：设计制作了 Ka 频段高输出功率的单片功率放大器. 基于河北半导体研究所的 0.25μm 栅长的 75mm GaAs PHEMT 工艺制作的三级功率放大器，芯片尺寸为 19.25mm^2(3.5mm×5.5mm). 在 32.5～35.5GHz 的频率范围内，小信号线性增益大于 16dB，带内平均 1dB 增益压缩点输出功率为 29.8dBm，最大饱和输出功率为 31dBm.

关键词：Ka 频段；功率放大器；MMIC；PHEMT

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