Low Power Design Orienting 384×288 Snapshot Infrared Readout Integrated Circuits

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Abstract: This paper presents a low power design for a 384×288 infrared (IR) readout integrated circuit (ROIC). For the character of IR detector ($r_o \approx 100k\Omega$, $I_{int} \approx 100nA$), a novel pixel structure called quad-share buffered direct injection (QSBDI) is proposed and realized. In QSBDI, four neighbor pixels share one buffered amplifier, which creates high injection efficiency, a stable bias, good FPN performance, and low power usage. This ROIC also supports two integration modes (integration then readout and integration while readout), two selectable gains, and four window readout modes. A test 128×128 ROIC is designed, fabricated, and tested. The test results show that the ROIC has good linearity. The peak to peak variance of the sub array is about 10mV. The power of pixel stage is only 1mW, and the total power dissipation is 37mW at a working frequency of 4MHz.

Key words: IR ROIC; QSBDI; IWR; ITR; low power; windowing
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1 Introduction

IR ROIC is an important part of IR focal plane arrays (FPA) and has been developed fast. The snapshot IR ROIC requires a large format, a small pixel area, and low power usage. Meanwhile, more and more customer friendly functions have been integrated in FPAs, such as IWR, selectable gains, and windowing readout[1~4].

The ROIC is always divided into 3 parts: the pixel stage, the column amplifier stage and the output buffer stage. The pixels receive the photocurrent signals and store them on the capacitor. The column amplifier carries the signal from the pixels to the output. The output buffer drives large off-chip capacitance.

Detailed pixel circuit design depends on the performance of the IR detector. When the detector's output resistance is low and the output resistance changes with the bias voltage, the pixel circuit is required to provide high injection efficiency and a stable bias for the detector. Meanwhile, snapshot ROIC pixel area is precious and a complex circuit cannot be tolerated. The direct injection structure should be simple, but the efficiency will decrease as the low detector output resistance decreases and varies with its bias voltage, though buffered direct injection (BDI) can provide high injection efficiency. But, for 384×288 ROICs, placing an amplifier in every pixel will result in a heavy power burden. In shared BDI (SBDI) structures, every row shares one amplifier to reduce power dissipation. For the format of 384×288, SBDI disperses the buffered amplifier over a long distance, which leads to poor symmetry and worsens the fixed pattern noise (FPN).

In this work, a novel practical pixel structure called quad-share buffered injection (QSBDI) is proposed. In this new structure, four neighbor pixels share one buffered amplifier. The QSBDI provides high injection efficiency, stable bias, and low power usage. Local matching brings improved FPN performance.

A 128×128 test ROIC with a QSBDI pixel structure is designed and fabricated with a CSMC 0.5μm DPTM process. Test results show that QSBDI works well. Power from the pixel is only about 1mW and the FPN of every sub array is about 10mV. IWR, selectable gains, and windowing readout are all integrated on the chip.

2 Overview of 384×288 ROIC

2.1 Architecture

Figure 1 shows the block diagram of the ROIC. The ROIC is composed of a 384×288 pixel array, a column amplifier stage, an output buffer, and some control circuits.

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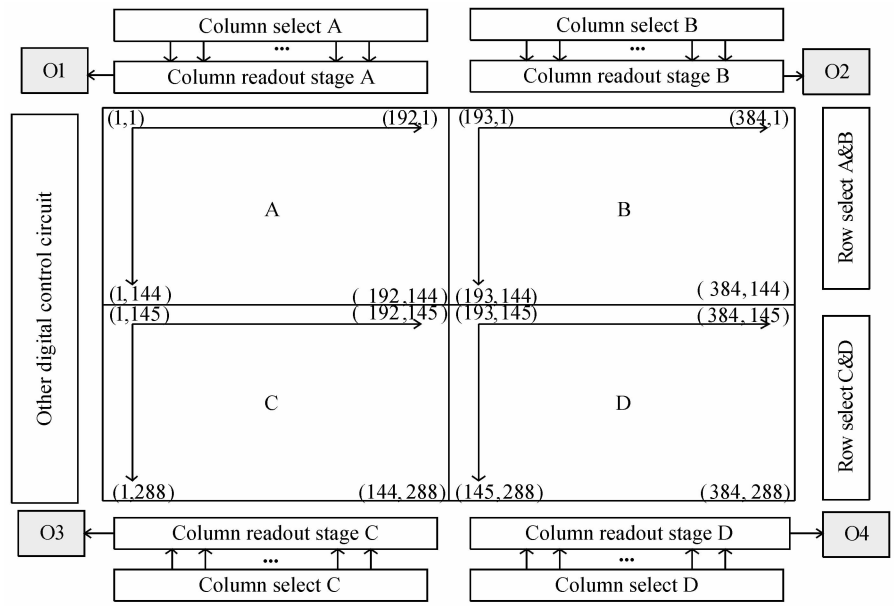

Fig. 1 Architecture of 384×288 ROIC

The pixel array has been divided into four sub arrays: A, B, C and D. The format of every sub array is 192×144. Corresponding to the four sub arrays, four output buffers are laid on the corner of the pixel array. The control circuits generate digital signals, such as row select signals and column select signals, to ensure that the chip works properly.

A charge sensitive amplifier (CSA) is chosen for the column readout amplifier. The CSA removes the need for a column bus parasitical capacitor and FPN that comes from the mismatch of integration capacitors in every pixel.

2.2 Operation timing

Figure 2 shows the ITR timing diagram of the readout circuit. The period of every frame is divided into two phases: the integration phase and the readout phase. When clock INT becomes "high", the integration phase begins. After the integration phase, the signal of each pixel is read out row by row. When clock row(i) is "high", the pixel signal charge of the first row is fed into the column amplifier . The signal is set up and stored on the column amplifiers, waiting to be multiplexed to the output amplifier buffer.

The column amplifiers are connected to the output buffer by the column switches. The signal stored on the column amplifiers is transferred column by column. The column readout amplifier is reset once each row with the control of the rst-CSA.

This ROIC also has IWR integration mode. When ROIC works in IWR mode, integration and readout can be processed simultaneously, increasing the frame frequency.

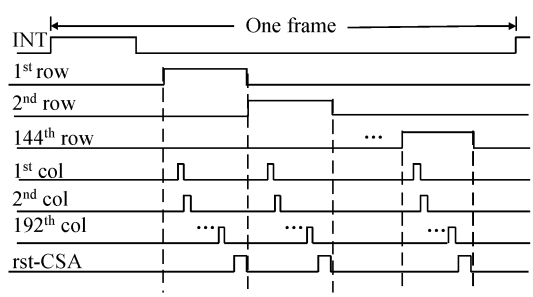

Fig. 2 Timing diagram of readout circuit

3 Quad-share BDI circuit

3.1 Quad-share BDI structure

Figure 3 shows the circuit of QSBDI. Four pixels share the same feedback amplifier. Considering the limited pixel area, a simple differential amplifier is adopted. Mp and Mn build the common branch, and Mp1-MN1, Mp2-Mn2, Mp3-Mn3, Mp4-Mn4 are the branches of each pixel individually. The IR detector, injection MOSFET, and integration capacitor are also shown in Fig. 3

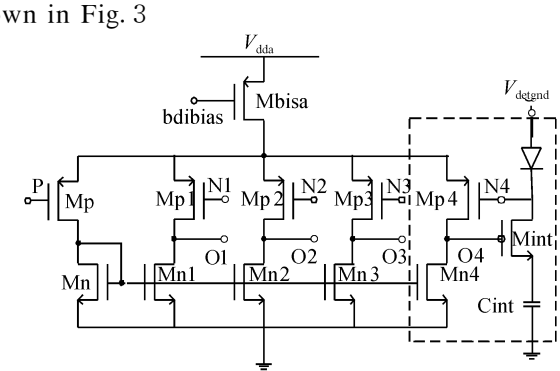

Fig. 3 Circuit of QSBDI

3.2 Operation principle

QSBDI's injection efficiency is as high as BDI and SBDI. This efficiency is expressed by[5,6]

$$\eta = \frac{Ag_m r_d}{1 + Ag_m r_d} \tag{1}$$

where g_m is the transconductance of the Mint, A is the gain of the shared buffering amplifier, and r_d is the output resistance of the detector. The gain A in Eq.(1) is larger than 100, so the injection efficiency is about unity.

Using the virtual ground of the feedback amplifier, QSBDI offers a stable DC bias.

3.3 Power dissipation

There are five differential branches in four pixels, so the average power dissipation of each buffer in the QSBDI input stage can be calculated as

$$P_{\text{pixel1}} = \frac{5}{4} I_d V_{dda} \tag{2}$$

where V_{dda} is the power supply, and I_d is the current of every differential branch.

Meanwhile, there are two differential branches in BDI pixel structures. The power dissipation in the BDI is $2I_d V_{dda}$. With an identical I_d, the QSBDI can save more than 30% of the power dissipation of the BDI. Moreover, the QSBDI also reduces the number of MOSFETs in the pixel and saves area, which can be used for capacitance to enlarge the charge storage capability and SNR. of course, the power of the SBDI is about $I_d V_{dda}$ when $N \gg 1$, where N is the number of pixels in the row. Table 1 shows the detailed comparison.

3.4 FPN performance

FPN is another important indicator of the readout circuit. The FPN refers to the random and time-invariant noise source associated with the fabrication process of detectors and readout circuits[1]. Due to the FPN, the outputs will be different even when the inputs are the same.

The FPN of the BDI structure comes from parameter variance of the inject MOSFET and the input offset voltage of the buffering amplifier. Those two sources can be transferred to the positive input terminal of the buffering amplifier and the small signal equivalent circuit, as shown in Fig. 4.

The injection current variation from the FPN can be written as

Table 1　Comparison of power and area

	BDI	QSBDI
Power	$2I_d V_{dda}$	$\frac{5}{4} I_d V_{dda}$
Amplifier's area	2 braches	Equivalent 1.25 braches

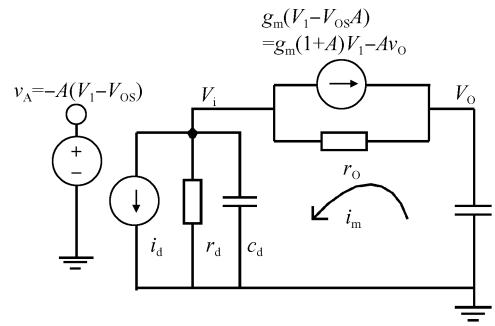

Fig.4　Small signal equivalent circuit for FPN analysis

$$\Delta I = \frac{Ag_m}{1 + Ag_m} \times \left(\frac{1}{A} V_{os.di} + V_{os}\right) \tag{3}$$

where $V_{os.di}$ represents the parameter variance of Mint and V_{os} stands for the input offset voltage of the buffering amplifier[4]. $V_{os.di}$ comes from the global mismatch. Because of the feedback of buffering amplifier, the effect of $V_{os.di}$ has been decreased to $1/A$. Assuming the gain of amplifier is infinite, the FPN is decided only by $V_{os.di}$. $V_{os.di}$ is the input offset voltage, which mainly stems from the mismatch of the parameter of input differential pairs and comes from the local mismatch. The input differential pairs are always required to be deposited as near as possible and they require high symmetry[7]. Some mismatches stem from long-range variations called gradients. The magnitude of gradient-induced mismatches depends on the separation between the effective centers, or centroids, of the matched devices. The variation ΔP in parameter P between two matched devices equals the product of the distance d between the centroids. The gradient ∇P along a line connecting the two centroids is[8]:

$$\Delta P = d \nabla P \tag{4}$$

The distance d will affect offset voltage directly. Table 2 is the comparison between the QSBDI and SBDI assuming the pixel area is $30\mu m \times 30\mu m$. In the SBDI, the whole row shares one buffer amplifier and N is the number of pixels in the row.

The length of one row in the SBDI is $30N(\mu m)$. On the other hand, careful layout design makes the distance of matching devices in the QSBDI about $40\mu m$. The matching of the QSBDI is better than the SBDI and the FPN.

4 IWR/ITR, selectable gains and windowing

4.1 IWR and TR

Based on the principle of the QSBDI, an actual

Table 2　Comparison of matching devices' distance

	SBDI	QSBDI
$d/\mu m$	$30N$	about 40

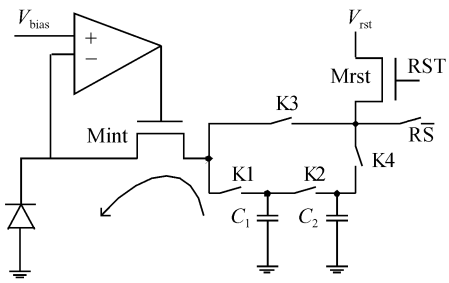

Fig. 5 Pixel structure to realize IWR and ITR

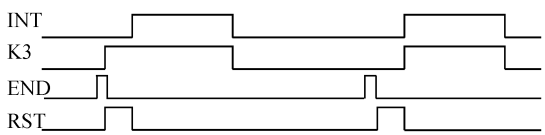

Fig. 6 Timing diagram of ITR mode

pixel with IWR and ITR has been designed and is shown in Fig. 5. An equivalent BDI is shown to illustrate the function of IWR and ITR instead of the QSBDI.

In ITR mode, the reading of the pixel will be executed after the integration completed. K1 remains open while K4 remains closed. K2 will control the gain of the pixel, which is set by the user. When K3 closes, integration begins. After the last pixel has been read out, signal END will be shown. RST closes and reset will be executed. Figure 6 shows the timing diagram of ITR mode.

In IWR mode, the reading of the pixels will occur during the next integration, as shown in Fig. 7. RST and K1 remain closed to prevent the nonlinearity that comes from setting up a buffered amplifier[9]. Before integration, K3 closes and resets C_1, then K3 opens and current begins to integrate on C_1. At this time, K2 is open and C_2 still holds the voltage of the previous frame. After the last pixel of the previous frame has been read out, the circuit will give a flag signal: END to flag the end of the previous frame. After the END, K4 closes and resets C_2. Then K2 closes to connect C_2 and C_1. At the end of the integration K2 opens and C_2 disconnects from C_1. The current frame voltage is held on C_2.

4.2 Two selectable gains

384 × 288 ROIC can work with two different gains by adjusting the gain control bit: GN. GN only

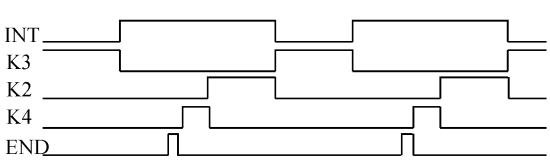

Fig. 7 Timing diagram of IWR mode

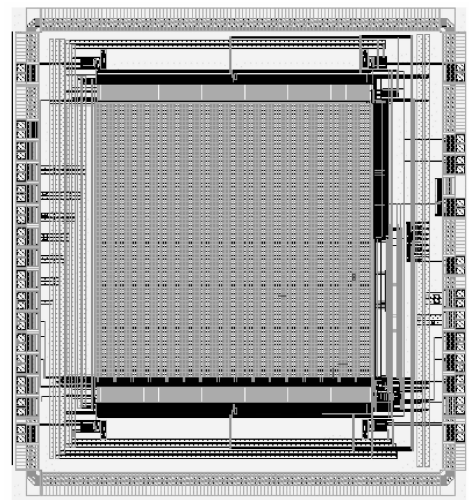

Fig. 8 Layout of 128×128 ROIC

works under ITR mode. Corresponding to different gains, the storage capacitor in the pixel and feedback capacitor in column readout stage are different.

4.3 Windowing readout

Window readout mode can help users readout the data they are interested in and can increase readout speed.

This ROIC full and default window size is 384 × 288. The ROIC also supports three windowing readout modes: 320×240, 160×120 and 128×128. These windows are centre asymmetric. To change the window mode, the ROIC preserves two window size control bits for users. By inducing the row select start signal and column select start signal in the right place, windowing can be realized.

5 Layout and test results

A test 128×128 ROIC has been fabricated with a CMSC 0.5μm DPTM process, packaged with PGA68 and tested with an Agilent 93000. Figure 8 is the layout of a 128 × 128 ROIC. Its size is 7.59mm × 6.35mm.

An electronic MOSFET called Mtest has been inserted in every pixel. In test mode, Mtest simulates the photo current before the ROIC is connected with the IR detector array. When the gate voltage of these electronic test MOSFETs is adjusted, ROIC's output

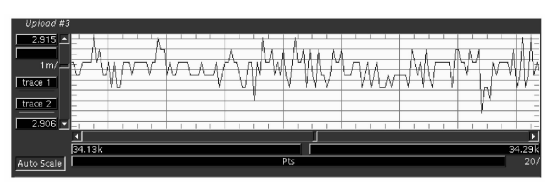

Fig. 9 Test result with Agilent

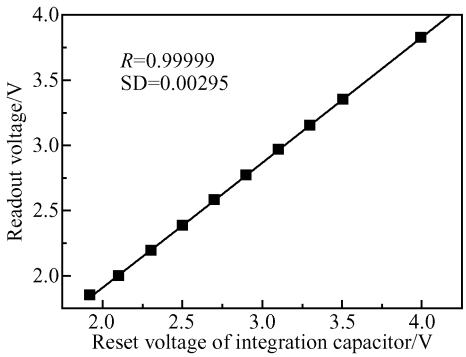

Fig. 10　Readout voltage versus reset voltage

changes. Shutting down the electronics test MOSFETs and varying the reset voltage of integration capacitors and integration time, ROIC's output changes again and shows good FPN performance. Figure 9 shows the test results, where the peak to peak variance of the sub array is about 10mV.

Linear fitting results of readout voltage versus reset voltage are displayed in Fig. 10 and show good linearity.

The power dissipation of the ROIC is about 37mW, and the consumption from the pixel stage is about 1mW. Test results show that the QSBDI has realized low power usage and good FPN performance.

IWR, selectable gains and windowing readout have been tested already and worked well. Table 3 lists the main features of the test ROIC.

Table 3　128×128 CMOS ROIC specifications

Array	128×128
Pixel structure	QSBDI
Pixel area	30μm×30μm
Storage charge	2.45pC
Voltage swing	2.6V
Integration mode	ITR and IWR
Window size	80×60, 64×64, 32×32
Gains	2 selectable gains
Outputs	4
Output rate	4MHz
Supply voltage	0～5V
Power	37mW
Chip area	7.59mm×6.35mm
Process	CSMC 0.5μm DPTM

6　Conclusion

A low power design for a 384×288 CMOS snapshot IR ROIC has been discussed. A high performance IR readout structure called QSBDI (Quad-share buffered direct injection) has been demonstrated and analyzed. Compared with the traditional BDI structure, the QSBDI saves the area and the power dissipation, which is a limitation of large format IR FPAs. When compared with the SBDI, the QSBDI decreases the offset of the buffering amplifier, which is the main source of the FPN, and increases the uniformity.

Using the QSBDI pixel structure, a 128×128 ROIC with IWR/ITR, selectable gains, and windowing readout has been designed and tested. Test results showed good linearity of 0.9999 and good sub array FPN performance of 10mV. The power dissipation from the pixel stage is 1mW, realizing low power design for the pixels. This test ROIC proved the low power schematic for 384×288 is valid and feasible.

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面向 384×288 面阵型红外读出电路的低功耗设计

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摘要：介绍了一种面向 384×288 CMOS 面阵性红外读出电路的低功耗设计.针对探测器的特点(输出阻抗约 100kΩ,积分电流约 100nA),新提出并实现了一种四像素共用 BDI 的 QSBDI(Quad-share BDI)像素结构.在 QSBDI 结构中,4 个相邻的像素共用一个反馈放大器,从而实现了高注入效率、稳定的偏置、较好的 FPN 特性和低功耗.另外该 384×288 读出电路还支持积分然后读出、积分同时读出功能,还有两个可选择的增益以及 4 种窗口读出模式.128×128 的测试读出电路已完成设计、加工和测试.电路使用 CSMC 0.5μm DPTM 工艺流片,测试结果表明在每个子阵列输出的峰峰差异仅为 10mV.在 4MHz 的工作频率下,像素级引入的功耗仅为 1mW,芯片的整体功耗也只有 37mW,实现了低功耗设计.

关键词：IR ROIC；QSBDI；IWR；ITR；低功耗；窗口

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