Low Power Polarity Conversion Based on the Whole Annealing Genetic Algorithm*

Wang Pengjun[†], Lu Jingang, Chen Ken, and Xu Jian

(*Institute of Circuits and Systems, Ningbo University, Ningbo 315211, China*)

Abstract: For an n-variable logic function, the power dissipation and area of the REED-MULLER (RM) circuit corresponding to each polarity are different. Based on the propagation algorithm of signal probability, the decomposition algorithm of a multi-input XOR/AND gate, and the multiple segment algorithm of polarity conversion, this paper successfully applies the whole annealing genetic algorithm (WAGA) to find the best polarity of an RM circuit. Through testing eight large-scale circuits from the Microelectronics Center North Carolina (MCNC) Benchmark, the SYNOPSYS synthesis results show that the RM circuits corresponding to the best polarity found using the proposed algorithm attain average power, area, and max delay savings of 77.2%, 62.4%, and 9.2% respectively, compared with those under polarity 0.

Key words: whole annealing genetic algorithm; REED-MULLER; low power; polarity conversion

EEACC: 1130

CLC number: TN302   **Document code:** A   **Article ID:** 0253-4177(2008)02-0298-06

1 Introduction

In recent years, the VLSI circuit has developed at a speed that Moore's Law could never foresee. As the scale and operating speed of IC increase, the power dissipation in circuits has become more significant. The on-going high power dissipation result in varied portable systems encountering not only power supply problem but also working invalidation and short life due mainly to the unacceptably high temperature in chips. Therefore, low power technology is considered one of the urgently needed technologies in modern IC designs[1].

The former low power technology is mainly used in circuits based on AND/OR or NAND/NOR gates of Boolean algebra[2]. The RM logic based on XOR/AND can not only express any kind of logic function, but also has many obvious superiorities in circuits such as arithmetic circuits, parity check circuits, and communication circuits compared to conventional logics based on AND/OR or NAND/NOR gates[3]. Generally, an RM expansion is derived from a given Boolean expression by applying a conversion approach such as coefficient-map, coefficient-matrix, or tabular techniques. As n-variable logic functions have 2^n fixed polarities and each polarity corresponds to different RM expressions, polarity is directly related to the power dissipation and the area of the circuit. An exhaustive search algorithm can be used to test every polarity to get the RM expression required in small scale circuits[4]. But, for large-scale circuits, because of the exponential relationship between variable and polarity and the increased time used to convert from one polarity to another, an exhaustive search algorithm is no longer appropriate. Thus, it is necessary to use an effective heuristic search algorithm to find the optimal or near-optimal polarity quickly and reliably.

The whole annealing genetic algorithm (WAGA) is a new genetic algorithm. It introduces annealing mechanisms to select operators and allows the father generation to take part in the competition, which solves the problem of a large search range but low convergence speed in conventional genetic algorithms, making it more robust and efficient[5]. Based on the polarity conversion of RM circuits, this paper successfully applies WAGA to find the best polarity of an RM circuit. Optimization of both power and area are obtained, for the cost function used in the algorithm contains factors of the power and area. Through testing eight large scale circuits from the Microelectronics Center North Carolina (MCNC) Benchmark, the SYNOPSYS synthesis results show that the RM circuits corresponding to the best polarity searched using the proposed arithmetic attain average power, area, and max delay savings of 77.2%, 62.4%, and 9.2% respectively, compared with those under polarity 0.

2　Power estimating model of RM circuit

In order to achieve low power in an RM circuit，a power estimating model of the RM circuit must first be established. Power dissipation in digital CMOS circuits is dominated by dynamic power dissipation，which results mainly from the charging and discharging of the node capacitances. For a circuit composed of n gates，its total dynamic power dissipation is[6]：

$$P = \frac{1}{2} V_{dd}^2 f_{clk} \sum_{i=1}^{n} C_L^i E_{sw}^i \tag{1}$$

where V_{dd} is the supply voltage，f_{clk} is the clock frequency，C_L^i is the output load capacitance of gate i，and E_{sw}^i is the average number of output transitions of gate i per clock cycle，which known as switch activity. In the process of logic synthesis，only the E_{sw}^i can be controlled and is in direct proportion to power dissipation. Thus，the value of switch activity directly reflects the power dissipation of circuits. The switch activity of a gate can be obtained from the output signal probability[7]：

$$E_{sw\_d}^i = 2P_{o,i} \tag{2}$$

$$E_{sw\_s}^i = 2P_{o,i}(1 - P_{o,i}) \tag{3}$$

where $P_{o,i}$ is the output signal probability，which can be obtained through the propagation algorithm of signal probability using the input signal probability. Equations （2） and （3） are the switch probability formulas implemented in dynamic logic and static logic，respectively. Besides the added pre-charge in dynamic logic，there is no essential difference between dynamic logic and static logic，and the latter is more commonly seen in CMOS circuits. Therefore，the computation of switch activity to be discussed in the following portion is based on static logic.

Any type of logical function can be expressed as follows[8]：

$$f(x_{n-1}, x_{n-2}, \cdots, x_0) = \bigoplus \sum_{i=0}^{2^n - 1} b_i \pi_i \tag{4}$$

where the subscript i can be expressed in a binary form as $i_{n-1} i_{n-2} \cdots i_0$，$\bigoplus\sum$ is the XOR operator，$b_i \in \{0,1\}$ indicates whether π_i is present in the expression，and π_i is the AND operator，which can be formulated as

$$\pi_i = \dot{x}_{n-1} \dot{x}_{n-2} \cdots \dot{x}_0, \quad \dot{x}_j = \begin{cases} 1, & i_j = 0 \\ x_j, & i_j = 1 \end{cases} \tag{5}$$

In a fixed polarity RM expansion with any fixed polarity $P = (p_{n-1} p_{n-2} \cdots p_0)$，every variable can only be either true or complemented，but not both. If an entry of P，p_j is 0 （or 1） then the corresponding variable is in the true （or complement） state. Therefore，there are 2^n fixed polarities and 2^n RM expressions
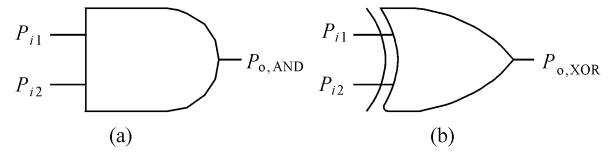

Fig. 1　Two-input AND gate （a） and XOR gate （b）

for an n-variable logical function.

Equation （4） shows that the power dissipation of RM circuit results primarily from AND gates and XOR gates. Prior to technology mapping，conventionally，all multi-input AND gates and XOR gates need to be decomposed into a tree of two input gates[4].

In an adequately long testing time，if the ratio between the time when $x = 1$ and the whole testing time is defined as the probability of signal x，noted as $P_{o,i}$，according to the propagation algorithm of signal probability mentioned in Ref.［7］，the output signal probabilities of the two-input AND gate shown in Fig. 1（a） and the two-input XOR gate shown in Fig. 1（b） can be defined as follows，respectively：

Two-input AND gate：

$$P_{o,AND} = P_{i1} P_{i2} \tag{6}$$

Two-input XOR gate：

$$P_{o,XOR} = P_{i1} + P_{i2} - 2P_{i1} P_{i2} \tag{7}$$

The output signal probability of the AND gate grows greater as the input signal probability increases，the low-power decomposition of multi-input AND gates is relatively simple，and a more desired result can be obtained using the Huffman algorithm[9].

The low-power decomposition of XOR is solved successfully through a new decomposition algorithm proposed in Ref.［10］ in which analysis is conducted on several optimizations developed at earlier stage. The processes of multi-input XOR gate decomposition are as follows：first，sort the input probabilities which are greater than 0.5；then，change the inputs whose probabilities are greater than 0.5 to their complements；finally，iteratively combine the two signals with the smallest probabilities until there is only one signal. A simple example demonstrates this algorithm. For three inputs (x_2, x_1, x_0) with corresponding signal probabilities of 0.31，0.72，0.93，respectively，Figure 2 shows the above algorithm applied to decompose a three-input XOR gate into a tree of two input XOR gates，and the switching activity is 0.92. But if we do not use this algorithm，the switching activity is 0.98.

According to above analyses，this paper establishes the following power estimation model of RM circuits. First，the Huffman algorithm is used to decompose a multi-input AND gate and the propagation algorithm of signal probability is used to get the output
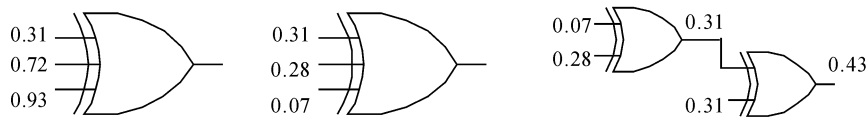
Fig.2 Low power multi-input XOR gate decomposition in static logic

signal probability of the two-input AND gate, where the output signal probability of the AND gate will be regarded as the input signal probability of the multi-input XOR gate. Then, the algorithm proposed in Ref. [10] is adopted to decompose the multi-input XOR gate, and the propagation algorithm of signal probability is used to get the switch activity of the two-input XOR gate. Finally, the switch activities of the AND gate and the XOR gate are summed to obtain the switch activity of the whole RM circuit, which reflects the power dissipation of the RM circuit.

3 Optimal polarity search based on WA-GA

3.1 Whole annealing genetic algorithm

The genetic algorithm is a probabilistic global search algorithm using a simple encoding technology and propagation mechanism to reflect complex phenomenon and solve very difficult problems[11]. It has been proven theoretically that genetic algorithms can converge to the optimal solution from the definition of probability. But, sometimes, algorithm performances are not satisfactory in application because of poor local search capability, premature convergence, etc.[12]. The simulated annealing algorithm demonstrates a good local search capability, which is the desired feature that genetic algorithms lack. Combining these two algorithms makes it possible to produce a high-performing new global search algorithm. The whole annealing genetic algorithm is a new genetic algorithm generated to achieve this desired result. It introduces an annealing mechanism to select the operator and allows the father generation to take part in the competition. Any individual generated by the new algorithm can converge to the global optimal solution with probability 1 at adequately high speed[13]. In this paper, the basic processes of the WAGA are as follows:

Step (1): Initialize the operating parameters, set the operating generation $t = 0$;

Step (2): Randomly generate the initial population $P(0)$;

Step (3): Calculate the fitness of the initial population $P(0) \leftarrow$ Evaluation $[P(0)]$;

Step (4): Perform the simulated annealing operation on the population
$P(t) \leftarrow$ Simulated Annealing $[P(t)]$;

Step (5): Perform the crossover operation on the population $P(t) \leftarrow$ Crossover $[P(t)]$;

Step (6): Perform the mutation operation on the population $P(t) \leftarrow$ Mutation $[P(t)]$;

Step (7): Calculate the fitness of the new population $P(t) \leftarrow$ Evaluation $[P(t)]$;

Step (8): Reserve the high fitness individuals of the father and offspring generation
$P(t) \leftarrow$ Reservation $[P(t)]$;

Step (9): Judge the termination condition; if the termination condition is not satisfactory, then

$t \leftarrow t + 1$ and skip to step (4); Otherwise, output the best individual and finish the algorithm.

3.2 Encoding and fitness function

In WAGA, encoding usually is the variable that needs to be optimized. This paper seeks the best polarity of the RM circuit, and the polarity is central to the RM conversion. Thus, the binary code of polarity can be directly designed as the algorithm encoding.

For an n-variable RM function, there are 2^n fixed polarities and each polarity corresponds to different RM expressions. Each RM expression has different areas and power dissipations, so the polarity is directly related to the power dissipation and area of circuit. However, the polarity is only a number and cannot reflect the performance by itself. But the area and power dissipation of the RM circuit corresponding to the polarity can reflect the quality of polarity. According to Eq. (4), the RM circuits are composed of XOR and AND gates. Thus, the number of AND and XOR gates can be used to measure the area of RM circuits, and the switching activity of AND and XOR gates can be used in the power dissipation of circuits. In order to find a good compromise of the area and the power, the number and switching activity of two-input XOR and AND gates obtained by low power decomposition of multi-input XOR and AND gates are used in our fitness function. The fitness function is defined as follows:

$$\text{fitness}(i) = (\alpha/\text{Area}(i) + (1-\alpha)/\text{Sa}(i)) \times \beta \quad (8)$$

where Area(i) and Sa(i) show the number and switching activity of two-input XOR and AND gates, respectively; α is the weight of the area and the power

dissipation，and $0 < \alpha < 1$；in order to facilitate the following operation，coefficient β is attached to prevent the fitness value from becoming too small.

In WAGA，the fitness value is usually required to be non-negative，and the larger it is the better the capability will be. But the better the polarity is the smaller the corresponding number and switching activity of XOR/AND gates. Thus，the number and switching activity of XOR/AND gates are engineered to be reciprocal in the fitness function.

3.3　Anneal operator

The WAGA allows the father generation to take part in the competition，which is a necessary and sufficient condition for convergence[13]. In order to make the algorithm more robust and efficient，the program is designed as follows. First，distribute N size storage space for the father and offspring generations（population size）respectively. Arrange the father and offspring generation according to their fitness value. Then，put together the 2/3 most superior individuals of father generation and the 2/3 most superior individuals of offspring generation to obtain a new father generation. Next，perform the simulated annealing operation on the new father generation，and select N individuals to enter the next crossover and mutation phase. If the fitness value of individual $i (i \in 4N/3)$ is $f(i)$，then the selected probability of i is

$$P(i) = \mathrm{e}^{f(i)/T_k} / \sum_{j=0}^{4N/3} \mathrm{e}^{f(j)/T_k} \quad (9)$$

where $\{T_k\}$ is the annealing temperature，which gradually approaches zero，and can be obtained by

$$T_k = 1/\ln(k/T_0 + 1) \quad (10)$$

where T_0 is the initial temperature，$k = 1,2,\cdots$

3.4　Crossover and mutation operator

In the crossover operation，uniform crossover is used. First，randomly select two individuals A and B from the father generation；Then，randomly produce the shielding binary code C which has the same length with A and B；Next，the offspring inherit the genes from the parents which are not shielded by the shielding binary code C. Two offspring can be generated in one crossover operation，and the detailed processes are shown in Fig.3.

Father generation	A	11101011
	B	01011101
S hielding code	C	10100111
Offspring generation	A'	11111011
	B'	01001101

Fig.3　An example of crossover

In the mutation operation，a basic bit mutation is adopted. If the original code equals 0，then changes it to 1，and vice versa. The detailed operating processes may be stated as follows. First，pre-define the chromosome selection probability（$P_{m1} = 10\%$）and gene mutation probability（$P_{m2} = 6\%$）. Then，enumerate the population's every chromosome and generate a random number $P_c (0 \sim 1)$. If this random number is smaller than the chromosome choice probability P_{m1}，then put this chromosome in the mutation pond. Next，enumerate every gene bit of the chromosome in the mutation pond and generate a random number P_g $(0 \sim 1)$. If this random number is smaller than the gene mutation probability P_{m2}，then change the value of the gene bit（namely change 0 to 1，vice versa）.

4　Experimental results

The proposed algorithm has been implemented in C and compiled by the GNU C compiler on the Linux operating system. In order to obtain convincing test results，we selected eight representative large-scale circuits from MCNC benchmarks to test the proposed algorithm. The following processes are made before testing. The MCNC benchmark circuits are in truthtable format，so they needed to be converted to RM format with the polarity conversion algorithm. The multiple segment technique proposed in Ref.［14］is more suitable for converting the large-scale logical function than existing polarity conversion algorithms. Thus，this polarity conversion algorithm is realized first，and then is unified with the WAGA to obtain the RM format circuits . In order to calculate the switching activity，twenty five input signal probabilities are generated under the random function，which are 0.86，0.18，0.69，0.97，0.70，0.28，0.41，0.05，0.58，0.07，0.37，0.68，0.32，0.78，0.58，0.43，0.31，0.25，0.81，0.82，0.58，0.52，0.79，0.57 and 0.84.

Table 1 shows the parameters used in our algorithm，and Table 2 shows the experimental results for eight circuits. To see the efficiency of the algorithm，the switching activity and the area under polarity 0 are also listed in the same table for comparison. In Table 2，column 1 shows the circuits' name while column 2 shows the number of inputs；columns 3，4 and 5 show the switching activity（SA），area（Area is the total number of XOR gates and AND gates），and the fitness under polarity 0，while the columns 6，7，8 and 9 show the best polarity，switching activity，area and fitness for the best polarity by using the proposed algorithm，respectively；the columns 10 and 11 show the percentage of the improvement for switching activity and area under the best polarity compared with the case of polarity 0.

Table 1　Parameters of WAGA

Circuit	Input	Population size	Generation size	α	β	T_0
alu4	14	50	20	0.8	1200	200
b12	15	70	25	0.5	50	250
duke2	22	300	60	0.9	1200	600
misex3	14	50	20	0.7	500	200
misex3c	14	50	20	0.6	5000	200
spla	16	90	30	0.9	500	1000
t481	16	90	30	0.5	100	300
table5	17	110	35	0.7	500	350

The percentage of improvement for switching activities is defined as follows：

$$Save_{SA} = \frac{SA_0 - SA_{WAGA}}{SA_0} \times 100\% \qquad (11)$$

While the area improvement is similarly defined in Eq.（12）.

$$Save_{Area} = \frac{Area_0 - Area_{WAGA}}{Area_0} \times 100\% \qquad (12)$$

Table 2 shows that the proposed algorithm is quite effective at finding the optimal polarity. The switching activities and area savings can be improved significantly for all eight circuits compared with those under polarity 0，and the improvement can be as high as 99.9%. The average reduction of switching activities is 90.1% while the average area reduction is 61.4% for all eight circuits.

In order to get the true power dissipation and area of the RM circuits corresponding to the two polarities mentioned above to further prove the validity of the algorithm，this paper uses the well-developed business software SYNOPSYS for synthetic purposes. The synthesis result is shown in Tables 3 and 4（transferring the model file in SYNOPSYS and the supply voltage is 1.8V），which proves that the RM circuits corresponding to the best polarity found using the proposed arithmetic achieve average power，area，and max delay savings of 77.2%，62.4%，and 9.2%，respectively，compared with those under polarity 0.

Table 2　Experimental results of polarity conversion based on WAGA

Circuit	Input	Polarity 0			WAGA polarity				Save/%	
		SA_0	$Area_0$ （XOR/AND）	Fitness	Polarity	SA_{WAGA}	$Area_{WAGA}$ （XOR/AND）	Fitness	SA	Area
alu4	14	145.69	938/5517	6.63	15375	22.10	419/2515	43.52	84.8	54.5
b12	15	12.33	13/33	2.57	19639	0.77	8/24	33.24	93.7	30.4
duke2	22	395.65	2535/21664	2.73	2032855	27.03	199/1700	40.02	93.2	92.2
misex3	14	58.59	447/2960	6.02	1039	11.23	300/1980	31.23	80.8	33.1
misex3c	14	559.79	2475/14730	5.48	1539	65.15	1558/10750	46.21	88.4	28.5
spla	16	605.17	8193/69633	0.74	64511	0.84	5/57	536.51	99.9	99.9
t481	16	23.91	40/68	2.55	39577	4.51	14/34	12.13	81.1	55.6
table5	17	107.45	863/7664	3.27	71272	0.96	23/256	365.12	99.1	96.7
Average save									90.1	61.4

Table 3　Synthesis results of SYNOPSYS

Circuit	Input	Polarity 0			WAGA polarity			
		Power/mW	Area(unit)	Max delay	Polarity	Power/mW	Area(unit)	Max delay
alu4	14	56.84	184685	4.17	15375	19.99	83629	4.69
b12	15	1.38	1547	1.55	19639	0.23	1038	1.67
duke2	22	212.10	656451	5.46	2032855	16.07	51517	4.81
misex3	14	27.59	95719	3.98	1039	15.10	64087	4.57
misex3c	14	178.18	491336	5.75	1539	83.77	343712	5.66
spla	16	548.44	2112674	5.55	64511	0.44	1627	2.44
t481	16	4.33	3932	2.09	39577	0.80	1583	1.94
table5	17	64.33	230206	4.78	71272	1.79	7340	3.25

Table 4　Reduction rations of power，area and max delay

Circuit	Input	Save/%		
		Power	Area	Max delay
alu4	14	64.8	54.7	−12.5
b12	15	83.3	32.9	−7.7
duke2	22	92.4	92.2	11.9
misex3	14	45.3	33.0	−14.8
misex3c	14	53.0	30.0	1.6
spla	16	99.9	99.9	56.0
t481	16	81.5	59.7	7.2
table5	17	97.2	96.8	32.0
Average save/%		77.2	62.4	9.2

5　Conclusion

By investigating the propagation algorithm of signal probability and the decomposition algorithm of multi-input XOR/AND gates，this paper proposed a new algorithm to find the best polarity based on WAGA. For the fitness function used in the algorithm containing the factors power and area，a good compromise between the power and the area is obtained.

The algorithm has been implemented in C. Through testing eight large-scale circuits from the MCNC Benchmark，the experimental results suggest that the RM circuit corresponding to the best polarity searched by the proposed algorithm has considerable advantage in saving power，area，and max delay. The algorithm is steady，effective，and is of great practicability.

References

［1］ Najm F N. A survey of power estimation techniques in VLSI circuits. IEEE Trans VLSI Syst，1995，2(4)：446

［2］ Rabaey J，Ammer J，Otis B，et al. Ultra low power design. IEEE Circuits and Devices Magazine，2006，22(4)：23

［3］ Wang Pengjun，Chen Xiexiong. Tabular techniques for OR-coincidence logic. Journal of Electronics，2006，23(2)：269

［4］ Xia Yinshui，Wu Xunwei，Almaini A E A. Power minimization of FPRM functions based on polarity conversion. Journal of Computer Science and Technology，2003，18(3)：325

［5］ Wang Xia，Zhou Guobiao. Strong convergence of global annealing genetic algorithm. Mathematica Applicata，2003，16(3)：1

［6］ Starzyk Janusz A，He Haibo. A novel low power logic circuit design scheme. IEEE Trans Circuits Syst II：Express Briefs，2007，54 (2)：176

［7］ Wu Xunwei，Sheng Fashen，Pedram M. Probability algorithm of multiple-valued behavior in power estimation. Journal of Hangzhou Institute of Electronic Engineering，2000，20(6)：1

［8］ Jaroslaw F B，Claudia L C，Susanto R. Column polarity matrix algorithm for ternary fixed polarity reed-muller expansions. Journal of Circuits，Systems and Computers，2006，15(2)：243

［9］ Tsai C，Marek-Dadowska M. Multilevel logic synthesis for arithmetic functions. ACM/IEEE Design Automation Conference，Las Vegas，USA，1996：68

［10］ Zhou H，Wong D F. Optimal low power XOR gate decomposition. ACM/IEEE Design Automation Conference，Las Angeles，USA，2000：104

［11］ Ren Qingsheng，Ye Zhongxing，Zeng Jin，et al. Analysis of genetic operators. Acta Electronica Sinica，2000，28(5)：113

［12］ Xu Lu，Tu Chengyu. A new improved genetic algorithm and it s property analysis. Acta Electronica Sinica，2001，29(7)：902

［13］ Zhang Jiangshe，Xu Zongben，Liang Yi. Whole annealing genetic algorithm and necessary & sufficient conditions for convergence. Science in China (Series E)，1997，27(2)：154

［14］ Wang L，Almaini A E A. Efficient polarity conversion for large boolean functions. IEE Proc-Comput Digit Tech，1999，146(4)：197

基于整体退火遗传算法的低功耗极性转换[*]

汪鹏君[†]　陆金刚　陈　恳　徐　建

（宁波大学电路与系统研究所，宁波　315211）

摘要： 针对 *n* 变量逻辑函数在不同极性下所对应 REED-MULLER (RM) 电路功耗和面积不同的特点，对信号几率传递算法、多输入 XOR/AND (异或/与) 门的低功耗分解算法和多成份极性转换算法进行了深入研究，成功地将整体退火遗传算法 (whole annealing genetic algorithm，WAGA) 应用于 RM 电路最佳极性的搜索. 通过对 8 个 MCNC Benchmark 测试表明，算法搜索到的最佳极性，其所对应 RM 电路的 SYNOPSYS 综合结果，与极性 0 时相比，功耗、面积和最大延时的平均节省分别达到了 77.2%，62.4% 和 9.2%.

关键词： 整体退火遗传算法；REED-MULLER；低功耗；极性转换

EEACC： 1130

中图分类号： TN302　　　　**文献标识码：** A　　　　**文章编号：** 0253-4177(2008)02-0298-06