A Novel Verification Development Platform for Passive UHF RFID Tag*

Chen Liying, Hou Chunping, Mao Luhong†, Wu Shunhua, Xu Zhenmei, and Wang Zhenxing

(*School of Electronic Information Engineering, Tianjin University, Tianjin 300072, China*)

Abstract: This paper introduces a novel verification development platform for the passive UHF RFID tag, which is compatible with the ISO/IEC 18000-6B standard, operating in the 915MHz ISM band. This platform efficiently reduces the design and development time and cost, and implements a fast prototype design of the passive UHF RFID tag. It includes the RFID analog front end and the tag control logic, which is implemented in an Altera ACEX FPGA. The RFID analog front end, which is fabricated using a Chartered 0.35μm two-poly four-metal CMOS process, contains a local oscillator, power on reset circuit, matching network and backscatter, rectifier, regulator, AM demodulator, etc. The platform achieves rapid, flexible and efficient verification and development, and can also be fit for other RFID standards after changing the tag control logic in FPGA.

Key words: verification development platform; passive UHF RFID; tag; FPGA
PACC: 8630; 7280C; 7230
CLC number: TN402 **Document code**: A **Article ID**: 0253-4177(2007)11-1696-05

1 Introduction

In recent years, radio frequency identification (RFID) is rapidly expending with applications such as drug anti-counterfeiting, supply chain management, logistics, automation toll collection system, access to control buildings, airport baggage, and aviation security[1~3]. As an automatic way for data transaction in object identification without human intervention or error, RFID technology has become very popular.

Current RFID systems commonly use several frequency ranges, including LF (125kHz, 135kHz), HF (13.56MHz), UHF (860 ~ 960MHz), and microwave (2.45GHz). UHF band is used worldwide for its long read range and low manufacturing cost in the distribution field. In North and South America, its center frequency is 915MHz, whereas in Europe, the Middle East, and the Russian Federation, it is mainly 866MHz. Asia and Australia use frequencies within the band from 866 to 954MHz. Korea made an allocation at 908.5 ~ 914MHz (bandwidth 5.5MHz)[1~6]. The RFID application systems often have customized requirements, which generally take a long time to design and have low tolerance for changes in specification[4]. As a result, the RFID tag, reader, relevant database and software must be specifically designed for each particular application, and must be physically modified or re-designed each time when the specification for the current application is adjusted, which increases the design and development time and cost.

This paper presents a novel verification development platform for the passive UHF RFID tag which is compatible with the ISO/IEC 18000-6B standard, operating at the 915MHz ISM band, and can be easily customized to work under other standards and proprietary commands in the desired application. The verification development platform efficiently reduces the design and development time, and implements the fast prototype design of the passive UHF RFID tag. It includes the RFID analog front end (AFE) and the tag control logic, which is implemented in an Altera ACEX FPGA. The RFID AFE, which is fabricated using a Chartered 0.35μm two-poly four-metal CMOS process, contains a local oscillator, power on reset circuit, matching network and backscatter, rectifier, regulator, AM demodulator, etc. The platform achieves rapid, flexible and efficient ver-

* Project supported by the National High Technology Research and Development Program of China (No. 2006AA04A109)
† Corresponding author. Email: tju_rfid@163.com
Received 17 May 2007, revised manuscript received 19 June 2007

ification and development by changing the tag control logic in FPGA. In addition to the ISO/IEC 18000-6B standard, the platform can also be fit for several RFID standards, such as the International Organization for Standardization (ISO) and the International Electrotechnical Commission (IEC) standard ISO/IEC 18000[5] and the EPCglobal™ standard EPC™ class-1 generation-2 (C1G2)[6]. The platform architecture and the operation of the different building blocks are described, respectively. The experimental results are presented and a conclusion is provided.

2 Architecture

The block diagram of the verification development platform is shown in Fig. 1. The RFID AFE and the tag control logic circuit of the diagram will be described in detail in the following paragraphs. The antenna, which receives the information and energy from the reader, can provide low loss and be matched to the input impedance of the rectifier by the matching network[7]. The AFE implements the energy transfer from the reader to the tag, the clock generation, and the data transmission in both directions. The FPGA-based control logic circuit performs the communication protocol and the anti-collision mechanism. The reset and the clock signals are supplied to the control logic as the system reset and clock, respectively. The Rx is the data signal received from the reader, and the Tx is the signal returned to the reader from the control logic. The Rx and Tx are enabled by the Dir signal of the control logic.

3 Design implementation

3.1 AFE design

The RFID AFE as shown in Fig. 1, which is fabricated using a Chartered 0.35μm two-poly four-metal CMOS process, contains a local oscillator, power on reset circuit, matching network and backscatter, rectifier, regulator, AM demodulator, etc. The matching network circuit, which is matched with the impedance of the antenna, is used to achieve maximum power transfer and better performance of the tag with the appropriate match. The received RF input signal power is converted to DC supply voltage by the rectifier. The regulator keeps the power supply at a proper level and provides the VDD supply with the tag control logic. The AM demodulator can extract the data from DSB-ASK, SSB-ASK, or PR-ASK modulation that are embedded in the carrier waveforms. The backscatter, which achieves ASK or PSK modulation, completes the return data link by adjusting the impedance of the AFE. The circuit of the power on reset (POR) generates the chip power on reset signal reset. Unlike an HF transponder, in UHF transponder the clock cannot be extracted directly from the carrier. The clock signal is created by the local oscillator, which is synchronized with the Rx by the control logic. Although the clock frequency varies slightly with the temperature, supply voltage, and the process parameter, the performance of the control logic circuitry will not be affected.

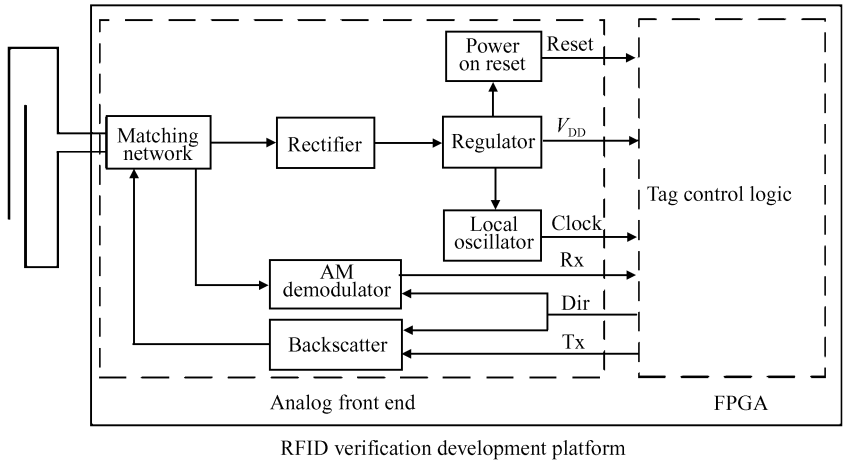

Fig. 1　Block diagram of the RFID verification development platform

3.2 Control logic design

The tag control logic is described in Verilog HDL at RTL level and implemented in the Altera ACEX FPGA. The main task of the control logic section is to treat the communication protocol. The international standard that establishes the way tags and readers communicate in the UHF spectrum is ISO 18000-6, which currently has three versions, i.e., ISO 18000-6A, 6B and 6C. In this paper, we implement the ISO 18000-6B standard. This standard defines the protocol for a UHF passive backscatter RFID system, featuring the following capabilities: identification and communication with multiple tags in the field, selection of a subgroup of tags for identification or communication, reading from and writing to or rewriting data many times to individual tags, user-controlled permanently lockable memory, data integrity protection, interrogator-to-tag communications link with error detection, and tag-to-interrogator communications link with error detection [5]. In the version of the prototype tag described below, all of the mandatory commands and a subset of the optional and custom commands defined by the ISO standard have been implemented.

Depending on their different logic function, the control logic is divided into six different modules, as shown in Fig. 2. The architecture is not only good for being implemented in FPGA, but also for being rapid, flexible and efficient verification and development with other RFID standards, such as the ISO standard 18000 series and the EPCglobal™ standard EPC™ C1G2. The Rx signal, which is performed by generating pulses that create a Manchester coding, is decoded by the decoder module. The Tx is the signal returned to the reader, which is encoded with the Manchester coding by the encoder module. The 16bit CRC-16 is calculated on all data bits received and transmitted by cyclic redundancy checks module. The control unit performs all the commands and controls. Also, the control unit controls the Dir signal, which enables the Rx and Tx. The module of the interface to memory implements the control of the memory, such as EEPROM, ROM and ferroelectric memory. This architecture is an advantage for implementing various kinds of RFID standards, and efficiently reduces the design and development time and cost. Figure 3 shows the time chart of the tag control logic.

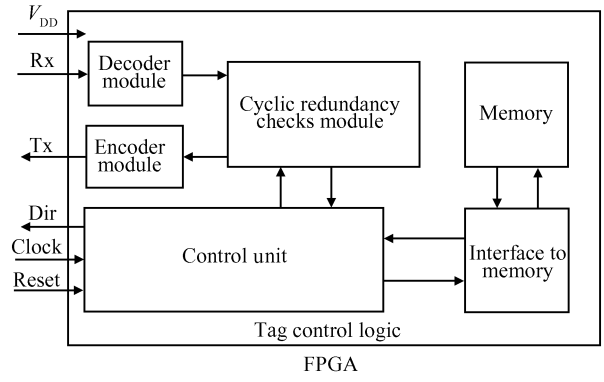

Fig. 2 Block diagram of the tag control logic implemented in FPGA

Although the local oscillator's output is stabilized, it is not enough to accurately sample a demodulated bit stream. To remedy the frequency error and synchronization problem, a synchronization algorithm is used. The demodulated data is encoded in Manchester code and all commands are followed by the preamble. The preamble is equivalent to 9bits of Manchester 0 in NRZ format[5], which is used to synchronize the Rx with the clock signal. The synchronization algorithm, which satisfies the bit rate accuracy of ±15% in the ISO/IEC 18000-6B standard with the local oscillator's output of 1.2MHz, is designed and optimized by an FPGA-based prototype design. Furthermore, the anti-collision scheme, the different tag functions and the communication protocols of the other standards, including EPC™ C1G2, are implemented in the prototype. The logic depth is reduced and the delay of each data path is balanced with the FPGA-based prototype, which improve the area and the power consumption of the RFID transponder IC chip.

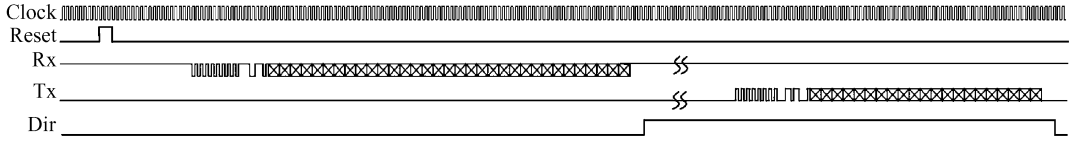

Fig. 3 Time chart of the tag control logic

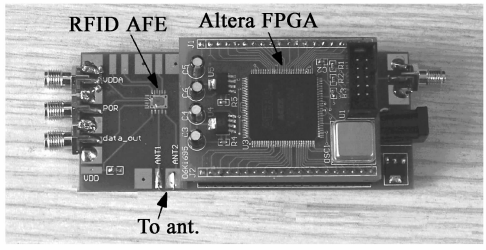

Fig. 4　Photograph of an assembled testing PCB of the verification development platform

4　Experimental results

A novel verification development platform for the passive UHF RFID tag is introduced. The platform includes the RFID AFE and the tag control logic, which is implemented in the Altera ACEX FPGA. Figure 4 is a photograph of an assembled testing PCB of the platform. The RFID AFE includes different building blocks, such as a local oscillator, power on reset circuit, matching network and backscatter, rectifier, regulator, AM demodulator. In normal applications, only two bonding wires are required to connect the antenna to the RFID tag. Figure 5 shows the testing results of the verification development platform. The demodulated waveform Rx is shown in Fig. 5 (b) and the backscattered signal Tx of the tag control logic is shown in Fig. 5 (c) with an Agilent 54642A oscilloscope by the UHF RFID reader of Model THM6BC1-915 (Tongfang Microelectronics Company, Beijing), which is compatible with ISO/IEC 18000-6B standard.

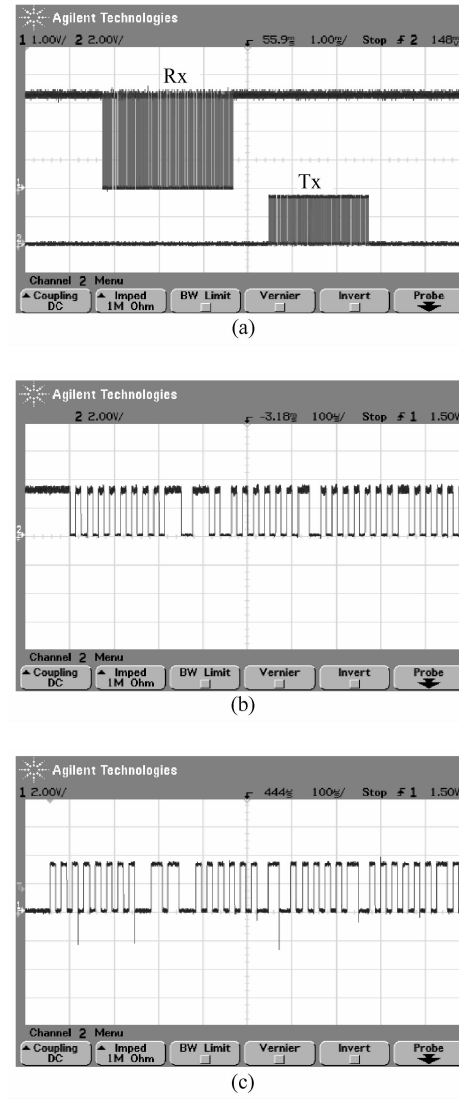

Fig. 5　(a) Demodulated waveform Rx of the RFID AFE and backscattered signal Tx waveform of the tag control logic; (b) Expanded demodulated waveform Rx; (c) Expanded backscattered signal Tx

5　Conclusions

This paper presents a novel verification development platform for the passive UHF RFID tag which is compatible with the ISO/IEC 18000-6B standard, operating at the 915MHz ISM band. The platform includes the RFID AFE and the tag control logic, which is implemented in the Altera ACEX FPGA. The RFID AFE is fabricated using a Chartered 0.35μm two-poly four-metal CMOS process. The verification development platform efficiently reduces the design and development time and cost, and implements the fast FPGA-based prototype design of the passive UHF RFID tag. Consequently, the platform achieves rapid, flexible and efficient verification and development by changing the tag control logic in FPGA. In addition to the ISO/IEC 18000-6B standard, the platform can be used for several RFID standards such as the ISO standard 18000 series and the EPCglobal™ standard EPC™ C1G2. It can also be easily customized to work with other standards and proprietary commands in desired applications.

Acknowledgements　The authors would like to thank Zheng Xuan and Li Yanming for their help in PCB designs and measurements, and Zheng Yujie in FPGA designs and measurements.

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一种无源 UHF RFID 电子标签验证开发平台*

陈力颖 侯春萍 毛陆虹† 吴顺华 徐振梅 王振兴

(天津大学电子信息工程学院，天津 300072)

摘要： 提出了一种符合 ISO/IEC 18000-6B 标准的无源 UHF RFID 电子标签验证开发平台，其工作在 915MHz ISM 频带下. 该平台有效减少了设计开发时间及成本，并实现了电子标签的快速原型设计. 该平台包括 RFID 模拟前端以及采用 Altera ACEX FPGA 实现的标签控制逻辑. RFID 模拟前端采用 Chartered 0.35μm 2P4M CMOS 工艺进行流片，包括本地振荡器、时钟产生电路、复位电路、匹配网络和反向散射电路、整流器、稳压器以及 AM 解调器等. 通过调整 FPGA 中的标签控制逻辑，该平台实现了快速、灵活而高效的 RFID 验证开发.

关键词： 验证开发平台；无源 UHF RFID；电子标签；FPGA

PACC： 8630；7280C；7230

中图分类号： TN402 **文献标识码：** A **文章编号：** 0253-4177(2007)11-1696-05

* 国家高技术研究发展计划资助项目(批准号：2006AA04A109)

† 通信作者. Email: tju_rfid@163.com

2007-05-17 收到，2007-06-19 定稿