Polysilicon Over-Etching Time Control of Advanced CMOS Processing with Emission Microscopy

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Abstract: The emission microscopy (EMMI) test is proposed as an effective method to control the polysilicon over-etching time of advanced CMOS processing combined with a novel test structure, named a poly-edge structure. From the values of the breakdown voltage (V_{bd}) of MOS capacitors (poly-edge structure), it was observed that, with for the initial polysilicon etching-time, almost all capacitors in one wafer failed under the initial failure model. With the increase of polysilicon over-etching time, the number of the initial failure capacitors decreased. Finally, no initial failure capacitors were observed after the polysilicon over-etching time was increased by 30s. The breakdown samples with the initial failure model and intrinsic failure model underwent EMMI tests. The EMMI test results show that the initial failure of capacitors with poly-edge structures was due to the bridging effect between the silicon substrate and the polysilicon gate caused by the residual polysilicon in the ditch between the shallow-trench isolation region and the active area, which will short the polysilicon gate with silicon substrate after the silicide process.

Key words: polysilicon over-etching; gate oxide reliability; emission microscopy
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1 Introduction

Silicon dioxide has been used as a gate dielectric of MOSFETs for more than 40 years since its excellent stability, uniformity, and easy fabrication process was introduced[1,2]. As the size of devices scales down for higher density and performance, the thickness of silicon oxide also scales down with Moore's law[3]. Based on the International Technology Roadmap for Semiconductor (ITRS), the equivalent oxide thickness (EOT) should be smaller than 1.5nm after 2005[4]. LOCOS isolation was developed in the early 1970s, and it remained for devices isolation until these technologies reached the 0.35 or 0.25μm generation[5]. However, for technology generations beyond 0.25μm, shallow-trench isolation (STI) replaced LOCOS. The drawback that LOCOS could not overcome was the field oxide bird's beak[6,7], which encroaches into the active areas of the chip, and the non-planer topography that results from thermally growing the semi-recessed filed oxide. Furthermore, due to processing, a ditch between STI and the active area will form[8]. After the polysilicon etching process, there will be some residual polysilicon in this ditch if the etching time is not well controlled[9]. Such residual polysilicon can degrade the reliability of the gate oxide. Thus, polysilicon over-etching time is a critical parameter for gate oxide reliability. In this paper, emission microscopy (EMMI) is proposed as an effective method to control the polysilicon over-etching time of advanced CMOS processing combined with a novel test structure, named a poly-edge structure, as shown in Fig.1. The breakdown voltage (V_{bd}) is selected as the evaluation criterion for the reliability of gate oxide, which is measured with the voltage ramp (V-ramp) method[10].

2 Experiment

The n- and p-MOS capacitors used in this study were with 3nm-thick oxides for low voltage device use, and used the poly-edge structure, as shown in Fig.1. These devices were prepared with a standard 0.18μm dual gate CMOS process. The breakdown voltages of the capacitors were measured on an HP

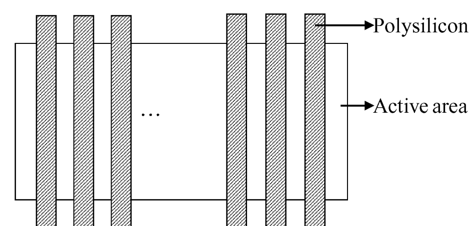

Fig.1 Illustration of poly-edge test structure

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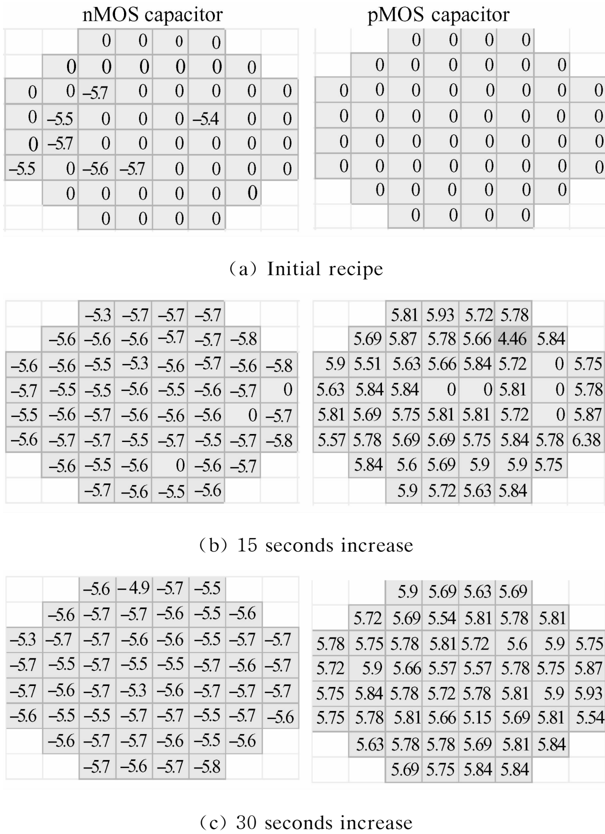

nMOS capacitor								pMOS capacitor							
		0	0	0	0					0	0	0	0		
	0	0	0	0	0	0			0	0	0	0	0	0	
0	0	-5.7	0	0	0	0	0	0	0	0	0	0	0	0	0
0	-5.5	0	0	0	-5.4	0	0	0	0	0	0	0	0	0	0
0	-5.7	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-5.5	0	-5.6	-5.7	0	0	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0			0	0	0	0	0	0	
		0	0	0	0					0	0	0	0		

(a) Initial recipe

		-5.3	-5.7	-5.7	-5.7					5.81	5.93	5.72	5.78		
	-5.6	-5.6	-5.6	-5.7	-5.7	-5.8			5.69	5.87	5.78	5.66	4.46	5.84	
-5.6	-5.6	-5.5	-5.3	-5.6	-5.7	-5.6	-5.8	5.9	5.51	5.63	5.66	5.84	5.72	0	5.75
-5.7	-5.5	-5.5	-5.6	-5.5	-5.6	-5.7	0	5.63	5.84	5.84	0	0	5.81	0	5.78
-5.5	-5.6	-5.7	-5.6	-5.6	-5.6	0	-5.7	5.81	5.69	5.75	5.81	5.81	5.72	0	5.87
-5.6	-5.7	-5.7	-5.5	-5.7	-5.5	-5.7	-5.8	5.57	5.78	5.69	5.69	5.75	5.84	5.78	6.38
	-5.6	-5.5	-5.6	0	-5.6	-5.7			5.84	5.6	5.69	5.9	5.9	5.75	
		-5.7	-5.6	-5.5	-5.6					5.9	5.72	5.63	5.84		

(b) 15 seconds increase

		-5.6	-4.9	-5.7	-5.5					5.9	5.69	5.63	5.69		
	-5.6	-5.7	-5.7	-5.6	-5.5	-5.6			5.72	5.69	5.54	5.81	5.78	5.81	
-5.3	-5.7	-5.7	-5.6	-5.6	-5.5	-5.7	-5.7	5.78	5.75	5.78	5.81	5.72	5.6	5.9	5.75
-5.7	-5.5	-5.7	-5.5	-5.5	-5.7	-5.6	-5.7	5.72	5.9	5.66	5.57	5.57	5.78	5.75	5.87
-5.7	-5.6	-5.7	-5.3	-5.6	-5.7	-5.7	-5.7	5.75	5.84	5.78	5.72	5.78	5.81	5.9	5.93
-5.6	-5.5	-5.5	-5.7	-5.7	-5.5	-5.7	-5.6	5.75	5.78	5.81	5.66	5.15	5.69	5.81	5.54
	-5.6	-5.7	-5.7	-5.6	-5.5	-5.6			5.63	5.78	5.78	5.69	5.81	5.84	
		-5.7	-5.6	-5.7	-5.8					5.69	5.75	5.84	5.84		

(c) 30 seconds increase

Fig.2　V_{bd} of nMOS and pMOS capacitors with different polysilicon over-etching times in one wafer

4071 semiconductor parameter analyzer system with the aid of PDQ-WLR software. The breakdown point was detected with the stress induced leakage current (SILC) method.

3　Results and discussion

Figure 1 shows the test structure used in this study, which is named a poly-edge structure. V-ramp measurements show that with the initial polysilicon etching recipe, almost all capacitors failed under the initial failure model (Fig. 2 (a)).

To understand the failure mechanism, the post-stressed sample with the initial failure model underwent an EMMI test. A voltage of 2.5V between the gate and the substrate was applied for the EMMI test. Figure 3 shows the EMMI picture of the sample. The leakage points concentrate at the edge of the test structure. The most likely reason for the initial failure is the bridging effect caused by poly residual in the ditch between the STI region and the active area. Figure 4 shows that there is a ditch between the STI and the active area. There is possibly some residual polysilicon in this ditch. Figure 5 shows the SEM photo of the STI ditch with the initial polysilicon etching time. In this figure, polysilicon residual in the ditch can be observed. After the silicide process, such residual polysilicon will short the polysilicon gate with the silicon substrate. Therefore, from the EMMI test, we find the leak current points at the edge of test structure, which was the joint interface of the STI and the active area. To prove our assumption, three lots with the different polysilicon over-etching time recipes were fabricated. The over-etching times were increased by 15 and 30s respectively. Figures 2 (b) and (c) show the V-ramp measurement results of these lots. As the over-etching time increased, more capacitors failed in the intrinsic-failure model. We found this phenomenon in both n-MOS and p-MOS capacitors. At the same time, an EMMI test of the normal intrinsic breakdown sample was also performed, as shown in Fig. 6. From the figure, we find that the failure points distribute randomly rather than gather at the edge of the test structure

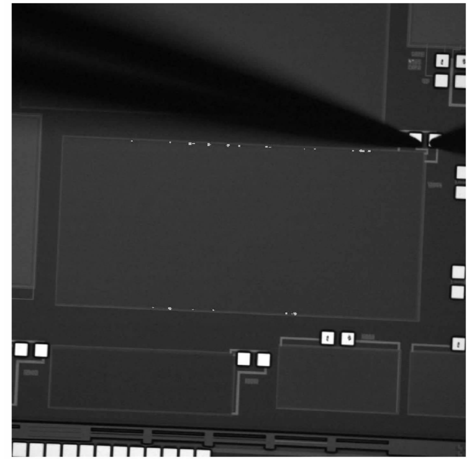

Fig. 3　Typical EMMI photo of MOS capacitor failed with initial failure model

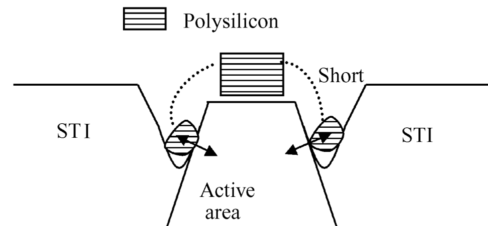

Fig. 4　Illustration of polysilicon residual-induced short between polysilicon gate and substrate

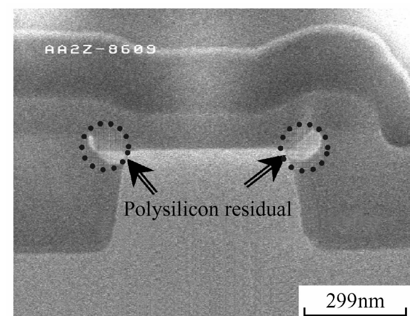

Fig. 5　SEM photo of SIT ditch with the initial recipe　The polysilicon residual can be observed.

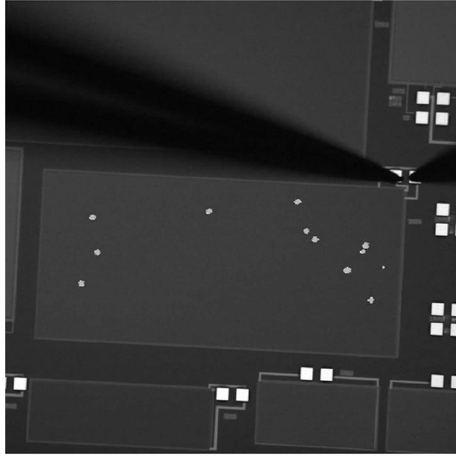

Fig.6 Typical EMMI photo of MOS capacitor failed with intrinsic failure model

like in the case of the initial failure sample. These experiments and results indicate that the most likely reason for the poly-edge structure's initial failure is the bridging effect caused by poly residual in the ditch between the STI region and the active area. The residual polysilicon can be removed by increasing polysilicon over-etching time. In summary, the initial failure of gate oxide can be eliminated by tuning the polysilicon over-etching time with the aid of EMMI tests combined with a poly-edge test structure.

4 Conclusion

In this paper, polysilicon over-etching time of a standard 0.18μm CMOS process has been controlled with an emission microscopy test combined with a novel test structure, named a poly-edge structure. Using the initial polysilicon etching-time, almost all capacitors (poly-edge structures) in one wafer failed under the initial failure model. After the polysilicon over-etching time was increased by 30s, no initial failure capacitors were found. The initial failure of capacitors with the poly-edge structure was due to the bridging effect between the silicon substrate and the polysilicon gate caused by the residual polysilicon in the ditch between the shallow-trench isolation (STI) region and the active area, which shorted the polysilicon gate with silicon substrate after the silicide process.

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用发光显微镜测试控制先进CMOS工艺的多晶硅刻蚀时间

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摘要：通过结合发光显微镜(EMMI)测试和poly-edge电容测试结构很好地控制了多晶硅刻蚀时间，避免了栅极氧化膜的早期失效．从栅极氧化膜击穿电压的测试结果可以看出，当刻蚀时间较短时，一个晶圆内几乎所有测试结构都呈现早期失效模式．通过延长刻蚀时间，早期失效数逐渐减少，最后可以完全消除早期失效，所有测试结构都为本征失效．为了分析多晶硅刻蚀时间和氧化膜失效模式的关系，对早期失效和本征失效样品进行了发光显微镜测试．Poly-edge电容结构的测试结果表明，过短的刻蚀时间导致了多晶硅在STI沟槽中的残留，硅化工艺后，这些多晶硅会使栅极和衬底短路，从而导致了栅极氧化膜的早期失效．通过延长刻蚀时间，可以有效地清除多晶硅的残留，从而保证栅极氧化膜的可靠性．

关键词：多晶硅刻蚀；栅氧可靠性；发光显微镜

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