Analysis and Design of a Low-Cost RFID Tag Analog Front-End

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Abstract: A new, low-cost RFID tag analog front-end compatible with ISO 14443A and ISO 14443B is presented. By substituting conventional multi-circle antenna with single-circle antenna, the package cost of the tag is greatly reduced. Based on this exasperate antenna performance, a new rectifier with high power conversion efficiency and low turn-on voltage is presented. The circuit is implemented in an SMIC 0.18μm EEPROM process. Measurement results show that with a 120kΩ load, the power conversion efficiency reaches as high as 36%. For a sinusoidal wave with magnitude of 0.5V, the output DC voltage reaches 1V, which is high enough for RFID tags. The read distance is as far as 22cm.

Key words: RFID; analog front-end; charge pump; low power; low voltage; single-circle antenna
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1 Introduction

RFID has been used in the markets of ticketing and supply chain management, and in the coming years it will be used to identify more kinds of goods in retail shops. But one of the bottlenecks against its far-ranging application is the cost. Although RFID tag LSIs have been developed to minimize costs, the costs of the tag fabrication and attaching it to products are even higher than the cost of the tag LSI itself, such as the high cost of antennas.

A feasible solution to this problem is applying smaller single-circle antenna to substitute for conventional multi-circle antenna. The cost of single-circle antenna is lower than conventional multi-circle antenna, but its performance suffers from much lower voltage and less power. Conventional tags with this proposed single-circle antenna cannot function properly. Thus, the analog front-end should be modified accordingly. In this paper, a new passive tag front-end operating at 13.56MHz and compatible with ISO 14443A and ISO 14443B is presented. The system power transmission theory is analyzed, and the performance of single-circle antenna and multi-circle antenna is compared. The architecture of this proposed analog front-end is also given.

2 Power transmission

An RFID system mainly comprises a reader and one or several tags. The passive tag is powered by the RF signals transmitted by the reader. To achieve a large operational range without error, the tag must have sufficient power over a long distance. The power transmission of an RFID tag is primarily determined by the following factors:

(1) The first is the impedance match between the antenna and the RF input ports of the tag. If the complex impedance of the antenna and resonant capacitor (Z_{antenna}) matches the complex impedance of the RF input ports (Z_{RF}), the chip can gain the maximum power. Thus, the ideal condition is:

$$Z_{\text{antenna}} = Z_{\text{RF}}^{*} \tag{1}$$

For different distances, the power received by antenna is different, so the power that circuit receives and the complex impedance of the RF input ports are all different. It is impractical and unnecessary to achieve a perfect match under all conditions. An impedance match is needed to optimize only when the tag is in the longest range, where the power is just sufficient to support the chip's steady work with no surplus. The antenna and resonant capacitor is evaluated in Eq. (2) to gain maximum voltage:

$$f = \frac{1}{2\pi\sqrt{L_{\text{tag}} C_{\text{resonant}}}} \tag{2}$$

where C_{resonant} is the summation of the additive capacitor C_1 and equivalent parasitic capacitor C_{P} in Fig. 1.

(2) The second is the power conversion efficiency (PCE). The other circuits (including the baseband, EEPROM, and other analog circuits) have more power (P_{L}, given by Eq. (3)) if the PCE of rectifier is higher.

$$P_{\text{L}} = P_{\text{antenna}} \eta_{\text{match}} \eta_{\text{rectifier}} \tag{3}$$

where P_{antenna} is the power received by antenna, η_{match} is the power transmission efficiency caused by imped-

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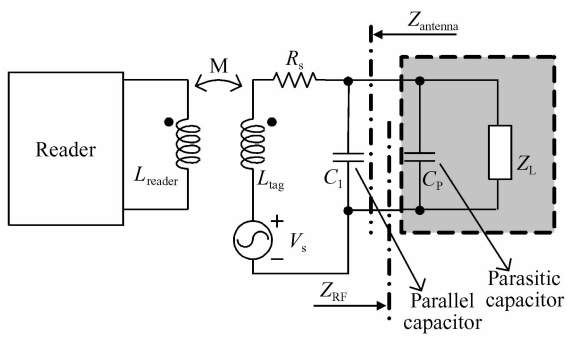

Fig. 1　power transmission in RFID system

ance matching, and $\eta_{rectifier}$ is the power conversion efficiency of the rectifier.

(3) The last is the power consumption of the whole circuit. The tag can function in the longer read/write range if the circuits consume less power. Therefore, it is necessary to minimize the power consumption of all the function blocks to optimize the read/write range.

3　Analysis of antenna performance

According to the electromagnetic theory and antenna theory, the energy received by antenna can be calculated by:

$$P_{tag} = \frac{n^2 A_{eff}^2 \omega^2 \mu^2 H^2}{R_{tag} + j\omega L_{tag} + \dfrac{R_L}{1 + j\omega R_L C_{resonant}}} \quad (4)$$

The voltage induced by antenna can be calculated by:

$$V_0 = n\omega\mu_0 H A_{eff} \quad (5)$$

where n is the circle number of antenna metal, A_{eff} is the equivalent effective area, and H is the operating magnetic field intensity.

We can estimate that, compared with multi-circle antenna, the power and voltage of single-circle antenna fall by approximate n multiples. This is the greatest challenge to this proposed design, so we need to ameliorate the analog front-end, especially the AC-DC rectifier and the power consumption by the other circuits.

4　Architecture

This proposed new architecture of the analog front-end is shown in Fig. 2. As analyzed above, compared with multi-circle antenna, the power and voltage fall markedly. Thus, a conventional rectifier, such as a bridge rectifier, cannot work with such low magnitude input. A conventional charge pump cannot work perfectly either because of its low power conversion efficiency. Thus, we designed a new charge pump with high power conversion efficiency and low

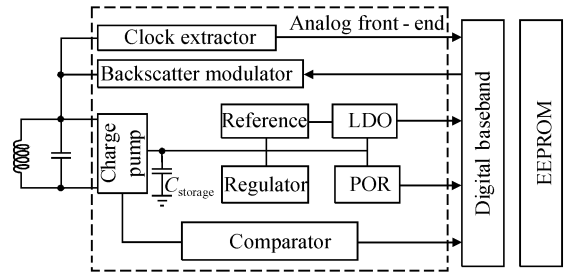

Fig. 2　Architecture of the analog front-end

turn-on voltage to implement the functions of a conventional rectifier and a demodulator. This can also reduce the parasitic capacitor, which negatively affects the resonant capacitor. The over-voltage protection (OVP) suppresses maximum applied voltage below the breakdown voltage to protect the circuits and the storage capacitor supplies the necessary energy when RF power shut off. The comparator converts the signal demodulated by the charge pump to a digital signal, and sends it to the baseband. The clock extractor extracts the carrier from the antenna and provides clock signal for the digital Baseband. The feedback signal is transmitted by changing the tag backscatter amplitude-Load modulation.

5　Building blocks

5.1　Charge pump

Figure 3 shows a conventional four-stage AC-DC charge pump with diode generating high voltage. The circuit is widely used in CMOS technology by substituting the diodes with diode-connected MOSFETs. We can increase the stage number to gain a high voltage output, but the power conversion efficiency falls as the stage number increases due to the existence of threshold voltage. The minimal input AC magnitude is limited by threshold voltage and the PCE is as low as 20%.

Recent research and applications choose Zero threshold or low threshold MOSFET or Schottky diodes to overcome this shortcoming[2]. Despite its low threshold, the reverse leakage current and the power consumption in the substrate increase, which nega-

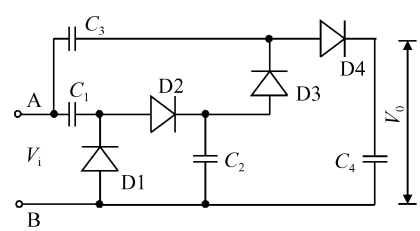

Fig. 3　Conventional charge pump

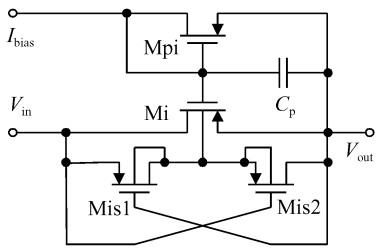

Fig. 4 Proposed CP_Cell

tively affect the PCE. The process adaptability is also restricted and cost rises. Reference [3] used an nMOS rectifier unit to reduce the influence of the V_{TH} drop by applying an external bias voltage. However, the efficiency is dependent on the external bias voltage, so the external bias voltage must be carefully adjusted according to the process variation. Reference [4] applied a large bias resistance to obtain bias voltage. However, the bias voltage drops rapidly as the input power decreases. Thus, the efficiency decreases under low input power.

In order to reduce the negative effect of the threshold voltage, the diode-connected MOSFET in a conventional charge pump is replaced by a new structure, as shown in Fig. 4. MOSFET Mi is the top-drawer charge-transfer transistor of this structure, and two auxiliary MOSFETs, Mis1 and Mis2 are introduced as switch transistors to update the body voltage of MOSFET Mi, reducing the body effect in substrate. Diode-connected pMOS Mpi is introduced to provide bias voltage V_{bias}, which is slightly lower than V_{TH}, for Mi to cancel the threshold voltage, so the voltage drop ΔV can be reduced in each stage. C_p is used to filter the high frequency components. If V_{in} is higher than V_{out}, Mi is on. The body is connected to V_{in}, and V_{bias} is the voltage difference between drain and gate. We obtain:

$$V_{GS} = V_{bias} + \Delta V \tag{6}$$

Oppositely, if V_{in} is lower than V_{out}, Mi must be cut off. The body is connected to V_{out} and V_{bias} is the voltage difference between source and gate. We get the range of V_{bias}:

$$V_{TH} - \Delta V < V_{bias} < V_{TH} \tag{7}$$

The voltage drop ΔV is the main cause of power consumption for each stage. Thus, ΔV must be minimized, which means V_{bias} should be close to V_{TH}. Furthermore, it must be optimized according to the equivalent load and input magnitude. At the same time, process and temperature variation should also be taken into account. Figure 5 shows the schematic of the proposed charge pump.

Bias block is a PTAT and provides current bias for odd stages. Even stages are biased by bias resistances (diode-connected MP1, 3, 5, 7), Switch block choose bias resistances (diode connected MP2, 4, 6, 8) according to the output voltage magnitude, to ensure the stabilization of bias voltage on the even stages. Figure 6 shows the schematic of the switch block (same as POR (power-on-reset) below).

As the output voltage of charge pump V_0 steadily rises, the voltage on C_i is:

$$V_i = \frac{iV_0}{N} \tag{8}$$

Thus, when

$$V_{i-1} + V_{in,m}\sin(\omega t) - V_i + V_{bias} > |V_{TH}| \tag{9}$$

this stage is on;

When

$$V_{i-1} + V_{in,m}\sin(\omega t) - V_i + V_{bias} < |V_{TH}| \tag{10}$$

this stage is off. Therefore, the opening critical time is:

$$t_0 = \frac{1}{\omega}\arcsin\left(\frac{\frac{V_0}{N} + |V_{TH}| - V_{bias}}{V_{in,m}}\right) \tag{11}$$

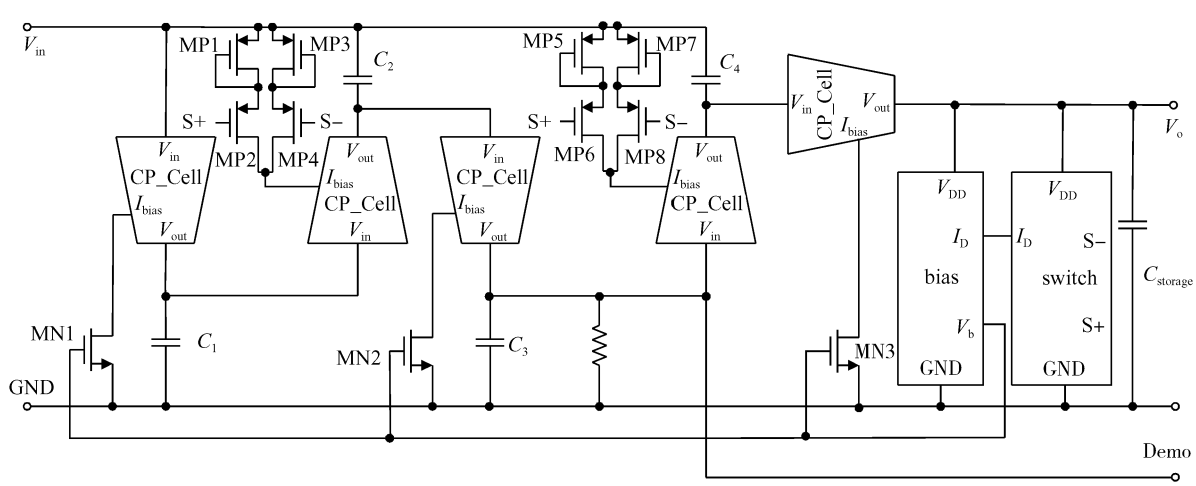

Fig. 5 Proposed charge pump

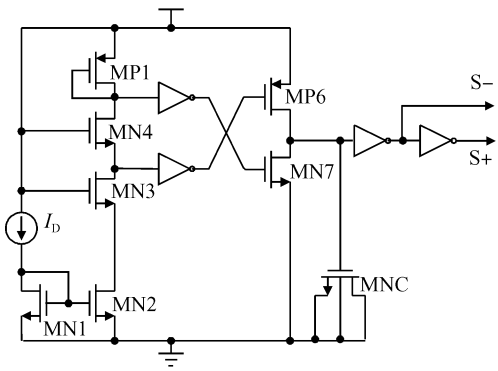

Fig. 6　Switch block

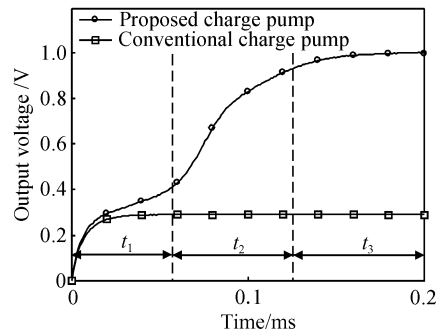

Fig. 7　Rising process simulation comparison results for conventional charge pump and proposed charge pump

Due to the existence of V_{bias}, the opening critical time t_0 is greatly reduced. Under ideal conditions, once V_0 has been set up steadily, the charge quantity stored on the capacitor is invariable. Thus

$$2\int_{t_0}^{\frac{T}{4}} I_{\text{D}}\,\mathrm{d}t = \int_0^T \frac{V_0}{R_{\text{eff}}}\mathrm{d}t \tag{12}$$

where R_{eff} is the equivalent load.

Therefore, the power conversion efficiency (PCE) is (ignoring the power consumption in substrate):

$$\eta = \frac{P_{\text{L}}}{P_{\text{L}} + N(P_{\text{i}} + P'_{\text{i}} + P_{C_{\text{GS}}}) + P_{\text{bias}} + P_{\text{switch}}} \tag{13}$$

where P_{bias} and P_{switch} are the static power consumptions of bias block and switch block, respectively.

Transient analysis shows that the rise process of output voltage resembles a positive feedback process. Figure 7 shows the output voltage rising process comparison, with 0.5V magnitude AC input, between this proposed charge pump and the conventional charge pump (as shown in Fig. 3), both with 5 stages. During the period t_1, when the output voltage of this proposed charge pump is not high enough to start the bias block, the charge-transfer transistors have no compensation voltage, so the charge pump operates as a conventional charge pump. During period t_2, once the output voltage is high enough (about 0.5V) to start the PTAT, the threshold voltage is canceled and the output voltage rises quickly until stabilization. The output voltage is 2.5 times higher than the conventional charge pump. The start-up voltage of the PTAT needs to be minimized in order to reduce the set-up time of the output voltage.

5.2　Voltage and current reference

A conventional PTAT is applied here to be the voltage and current reference, providing voltage and current reference for EEPROM, the comparator, POR (power-on-reset), and LDO. A start-up circuit without static power consumption is applied to start PTAT. Once PTAT is started, the start-up circuit is cut off and no current leaks.

5.3　POR (power-on-reset)

When a tag is in the operating field, the output voltage of the charge pump rises (up to 1V) high enough to support the other blocks and POR resets the baseband and starts the communication with reader. Once the tag leaves the operating field, the power voltage falls to 0.8V, and POR shuts off the baseband and terminates the communication. The schematic of this block is the same as the switch in the charge pump analyzed above, as shown in Fig. 6.

5.4　LDO

LDO is applied to provide a stable supply voltage (1V) for EEPROM, baseband, and some other analog blocks. The voltage and current reference are given by PTAT.

5.5　Comparator

As the tag is not fixed in the operating field, the signal amplitude demodulated by the charge pump is variable, so a hysteresis comparator, shown in Fig. 8, is applied to reduce the negative effect caused by noise and field fluctuations. As the demodulated signal varies at different distances, powering the comparator with a fixed voltage is unpractical. In this proposed analog front-end, the charge pump plays the roles of rectifier and demodulator. As the demodulated signal is generated in third stage of the 5-stage charge pump, the amplitude of the demodulated signal is always about 60% of the output DC voltage in all different conditions. An RC low pass filter is applied to generate a dynamic reference signal, preventing demodulation errors caused by noise or field fluctuation.

5.6　Clock extractor

Due to the single-circle antenna applied in this proposed tag, the amplitude of the carrier on the an-

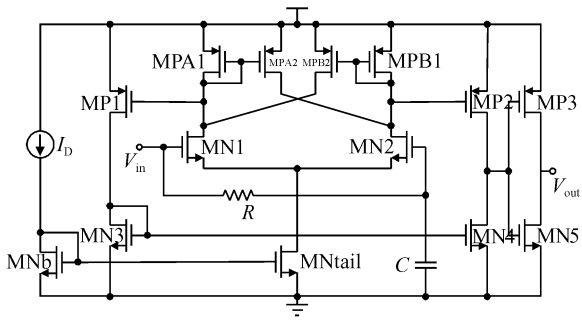

Fig. 8 Comparator schematic

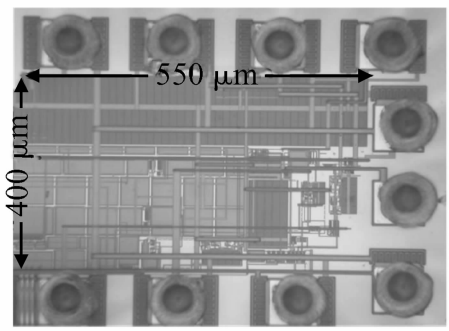

Fig. 10 Micrograph of the proposed analog front-end

tenna is about 100mV during backscatter load modulation, much lower than the threshold voltage V_{TH}. Thus, a conventional inverter or trigger cannot extract the clock signal for digital Baseband. A differential amplifier shown in Fig. 9 is applied here as a clock extractor. Serial resistors provide common-mode voltage for input transistor MN1 and MN2. The amplifier and buffer require careful design to optimize the power consummation.

5.7 Over-voltage protection (OVP)

When tag is near the reader, the magnetic field strength is very high and the output DC voltage of the charge pump is very high. OVP is applied to limit the power supply when the tag is near the reader to protect the other circuits, avoiding breakdown. When tag is far from the reader, OVP is cut off.

5.8 Load modulation

Load modulation is applied to transmit the signal from the tag to the reader and is implemented using a transistor and resistor. By turning on or off the transistor controlled by a digital signal that has been modulated with a sub-carrier, the impedance of the tag changes, leading to the equivalent impedance in reader antenna changes. The reader can demodulate the impedance change and achieve communication between reader and tag.

6 Experimental results

The whole RFID tag analog front-end is implemented in an SMIC 0.18μm EEPROM process. The micrograph of this proposed analog front-end is shown in Fig. 10.

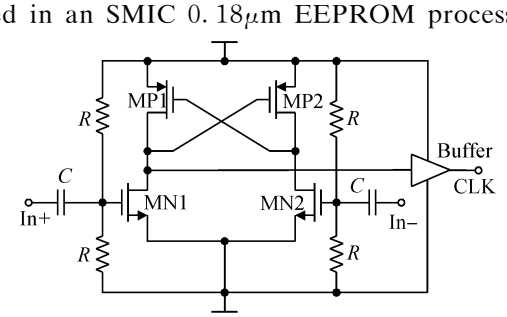

Fig. 9 Clock extractor

Figure 11 (a) presents the calculation, simulation, and measurement results of the proposed charge pump with a 120kΩ load. The output voltage rises with good linearity as the magnitude of the input sinusoidal wave rises. Measurement results shows that the turn-on magnitude of the charge pump is as low as 0.3V, 120mV lower than the threshold voltage, with 0.6V DC output voltage to power the chip. The measurement results show that the performance of this proposed charge pump successfully follows the theoretical analysis and simulation results. Figure 11 (b) presents the measured power conversion efficiency comparison between this work and several recent works. The efficiency of the proposed charge pump reaches 36% with −9.5dBm input power. Compared to Refs. [3, 4], the efficiency is stable between 26% and 36%, with a wide range of input power, especially

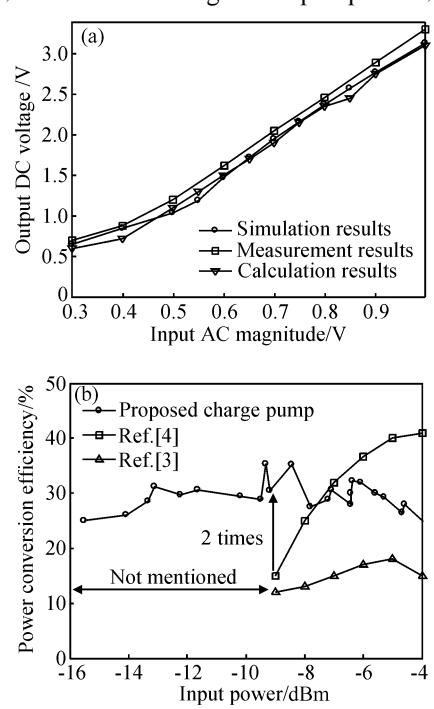

Fig. 11 (a) Calculation, simulation, and measurement results of output voltage with 120kΩ load; (b) Simulation and measurement results of PCE

ultra low input power. As RFID tags receive less power at longer distances, the high power conversion efficiency with ultra low input power is foremost for RFID tags.

The chip was tested with a 13.56MHz reader. The antenna size of this proposed circuit is 30mm × 30mm. The measuremental results show that the chip works well and satisfies the design target. The modulation index to be detected is 10%～100%. Compared with a 10～15cm read range for conventional tags, the read range of this proposed work reaches as long as 22cm. Measurement results show that the static current of the analog front-end is 3.2μA at a supply voltage of 1V, which matches the simulation results. Compared with conventional multi-circle antenna, this work with single-circle antenna can reduce the tag cost by 20%.

7 Conclusion

Implemented in an SMIC 0.18μm EEPROM process, a low cost RFID tag analog front-end with single-circle antenna is designed, which is compatible with ISO 14443A and ISO 14443B. Simulation and measurement results show that the chip has high power conversion efficiency, low voltage, low power, low cost, and high performance in an environment of noise and power fluctuation. The device satisfies the design target, agrees with the theoretical analysis, and meets the demands of ISO 10373.

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低成本射频识别标签模拟前端分析与设计

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摘要：提出一种新的低成本射频识别标签模拟前端，同时兼容 ISO 14443A 和 ISO 14443B 协议. 相比于传统模拟前端，本设计采用面积更小的单线圈天线代替传统大面积多圈天线，使得标签的封装成本大幅度降低. 考虑到单线圈天线的性能降低，设计了一个新的具有高效率低启动电压的电荷泵整流电路. 整体电路采用 SMIC 0.18 μm EEPROM 工艺实现，测试结果显示电荷泵驱动 120kΩ 等效负载时，整流效率达到 36%，输入交流幅度仅 0.5V 时，输出电压达到电路工作电压 1V. 标签的阅读距离可以达到 22cm.

关键词：射频识别；模拟前端；电荷泵；低功耗；低电压；单线圈天线

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