A Low Jitter Design of Ring Oscillators in 1.25GHz Serdes

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Abstract: A new configuration for delay cells used in voltage controlled oscillators is presented. A jitter comparison between the source-coupled differential delay cell and the proposed CMOS inverter based delay cell is given. A new method to optimize loop parameters based on low-jitter in PLL is also introduced. A low-jitter 1.25GHz Serdes is implemented in a 0.35μm standard 2P3M CMOS process. The result shows that the RJ (random jitter) RMS of 1.25GHz data rate series output is 2.3ps (0.0015UI) and RJ (1 sigma) is 0.0035UI. A phase noise measurement shows −120dBc/Hz@100kHz at 1111100000 clock-pattern data out.

Key words: Serdes; voltage controlled ring oscillator; low jitter
EEACC: 1205; 1230; 1280
CLC number: TN432 **Document code**: A **Article ID**: 0253-4177(2008)03-0490-07

1 Introduction

With the quick development of communication systems, serial data communication has emerged as a mainstream technology for Gb/s wirelines and optical links. Serdes stands for Serializer and Deserializer. As speeds reach gigahertz, jitter problems will emerge because the timing margin is stringent. There have been many attempts to lower jitter in high speed data communications, and some specific structures are presented in Refs. [1, 2]. Loop-parameter optimization based on a phase-locked loop is presented in Refs. [3, 4] to meet jitter specifications.

This paper brings forward a new configuration for a low-jitter ring VCO used in PLLs both for transmitters and receivers in 1.25GHz SerDes, which can be used as a physical layer in 1000 Base-T Ethernet networks. The design focuses on timing jitter because jitter is a main specification in series data communication.

2 Architecture

A serializer is time division multiplex. It consists of four parts, as shown in Fig. 1. Ten parallel data Tx〈9〉 to Tx〈0〉 at 125M data rate are latched in the register, and go out in series through shift registers at a rate of 1.25GHz clock provided by TX_PLL clock generator. The high speed data is transmitted into a cable, normally a 50Ω resister, through a line driver, which is used as a matching network.

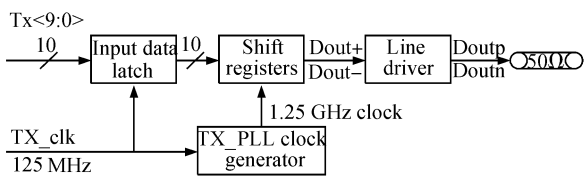

Fig. 1 Transmitter architecture in Serdes

The TX_PLL structure is shown in Fig. 2, where a third-order type 2 loop is used. This loop is commonly used because of its good performance for frequency steps.[5]

3 VCO block design

Ring VCOs have been widely used in a number of applications, such as clock and data recovery, which do not have as serious constraints on phase noise as radio applications. VCO design is decisive in PLL because system phase noise in PLL is equal to that in the VCO outside open-loop bandwidth. Furthermore, there is close relationship between jitter and phase noise. There are many critical issues surrounding the implementation of ring-oscillator VCOs. The realization of a VCO with low-jitter, low phase noise, good supply noise rejection, and high frequency capability requires trade off and careful attention, taking process, temperature, and power supply variation into

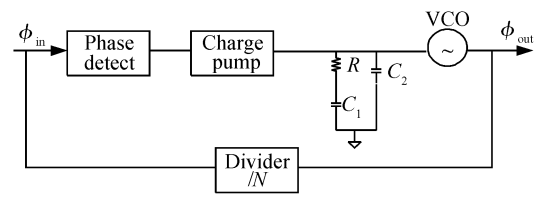

Fig. 2 TX_PLL structure and LPF

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Received 9 July 2007

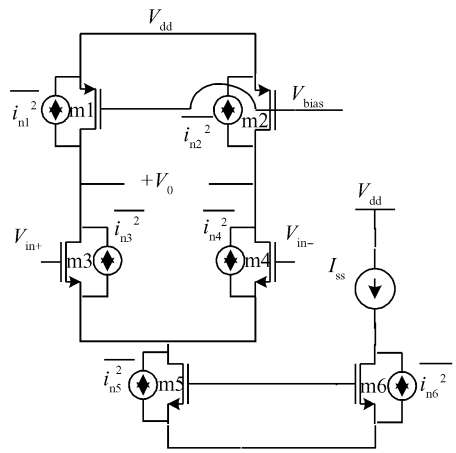

Fig. 3　Source-coupled differential delay cell[6]

consideration. This section introduces a new schematic such as a CMOS inverter delay cell, voltage-to-current (V2I) used in a ring oscillator VCO. Compared to source-coupled differential delay cell in Ref. [6], low-jitter and low power dissipation are obtained in CMOS inverter delay cells.

3.1　CMOS inverter delay cell

Many papers[6,7] have introduced timing jitter in ring oscillators. One stage of a source-coupled differential delay cell is given in Fig. 3. It is widely used because of its high speed and rejection of supply noise.

When designing a ring oscillator for Serdes, the parameter of interest is the jitter per cycle of oscillation, or cycle-to-cycle jitter. Reference [6] gave three methods for modeling circuit noise induced timing jitter. For suppression of inside bandwidth phase noise in PLL, $1/f$ noise in the ring oscillator can be omitted for the moment. All thermal noise of the transistor is shown in Fig. 3. For the first method in Ref. [6], a simplifying assumption, including constant noise sources, is made, so that the basic path from current noise to output voltage noise to timing jitter can be illustrated. The second method adds timing-varying effects, requiring more sophisticated methods like autocorrelation function analysis at the time domain. The third method presents a complete analysis using the same tools as the second method but takes inter stage amplification into consideration, and gives the output voltage noise for one stage and cycle-to-cycle jitter, which are:

$$\overline{v_n^2}(t) = \frac{KT}{C_L} \times \frac{a_v^2}{2}\xi_1^2 \tag{1}$$

$$\Delta\tau_{vco}^2 = \frac{kT}{I_{ss}} \times \frac{a_v \xi_1^2}{2(V_{GS} - V_T)} T_0 \tag{2}$$

where the ξ is the parameter concerning noise sources in Fig. 3, and the more noise sources, the larger the parameter ξ is. From a circuit design view, increasing

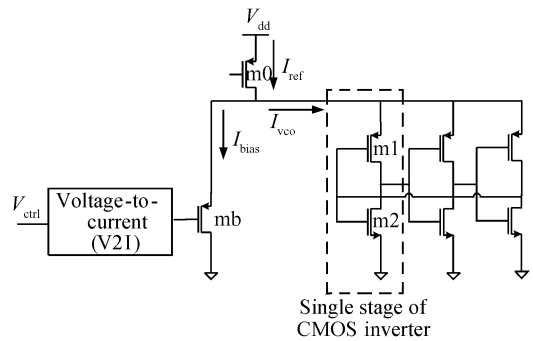

Fig. 4　Structure of VCO using CMOS inverter cell

static current I_{ss} and voltage room V_{dsat} can decrease timing jitter, but, in fact, increase the power consumption. The single stage voltage gain a_v in Eq. (2) comes from the effect of the inter stage influence, and a_v cannot be too small to make a ring oscillator function. Therefore, timing jitter is limited by the circuit itself.

A more competitive configuration adopted in this paper is shown in Fig. 4. Transistor m0 serves as a current mirror and provide reference current I_{ref}. Block voltage-to-current transfers voltage to current I_{bias}. The current flowing to CMOS inverters I_{vco} is I_{ref} minus I_{bias}, thus changing the delay time and the frequency of oscillator as I_{bias} changes.

The voltage controlled oscillator proposed in this paper has good PSRR due to transistor m0 in Fig. 4. The equivalent small signal current for the CMOS inverter with the current tail is shown in Fig. 5. Figure 5 is when the inverter is in the switching point where it is most vulnerable from noise when calculating timing jitter.

The current source is similar to the differential delay cell presented in Ref. [8], and PSR can be approximately expressed as

$$\frac{\Delta V_{O\text{-}DIFF}(s)}{\Delta V_{DD}(s)} \doteq \frac{1 + g_{m1} r_{ds}^2 C_p s}{g_{m2}^2 r_{ds}^2 + s g_{m1} r_{ds}^2 (C_p + C_o)} \tag{3}$$

Figure 6 shows the simulation results of the output PSR of a single stage inverter in Fig. 4.

3.2　Jitter analysis

A great deal of effort has been made to analyze

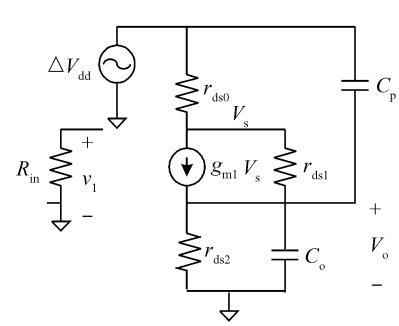

Fig. 5　Equivalent small signal circuit for inverter

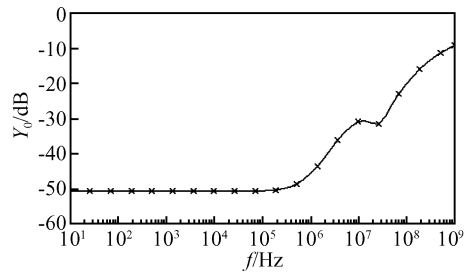

Fig. 6 Simulated PSR of CMOS inverter

timing jitter, especially random jitter. Mcneil[7,9], Weigandt[6] analyzed the jitter at the time domain, and the result matched the theory well. Due to a lack of analysis of CMOS inverter based delay cells, this section will extend the analysis of differential delay cell to inverters. Figure 7 (a) is a three stage inverter ring VCO. Reference [10] gave the theoretical analysis and empirical expression of the delay time of a single stage of inverter as follows:

$$t_d = \frac{t_f}{2} = \frac{t_r}{2} = \frac{h}{2} \times \frac{C_L}{\beta_n V_{dd}} \tag{4}$$

where h is the empirical parameter which is normally 10[10]. With the assumption that the load capacitor is dominated by the gate capacitor C_L, the oscillation frequency is

$$f_o = \frac{1}{2Nt_d} = \frac{\mu V_{ddi}}{NhL^2} \tag{5}$$

Oscillation frequency is proportional to V_{ddi} and is sensitive to ripples in voltage. But the configuration in Fig. 7 (a) avoids this problem as V_{ddi} is quite clean.

Before further analysis, it is worth noting that the timing jitter is noise superposed on the signal of the inverter output, as shown in Fig. 7 (b). We will analyze the output voltage noise of the second stage below. If V_{in} is above the threshold voltage of the inverter, the first stage inverter will discharge to V_{gnd} and the second will charge to V_{ddi}. Thinking that the noise of the first stage is amplified by the second

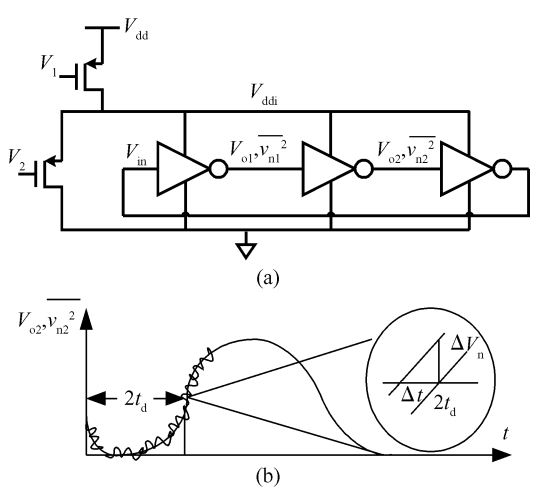

Fig. 7 (a) CMOS inverter VCO; (b) Signal and noise in three stage inverter

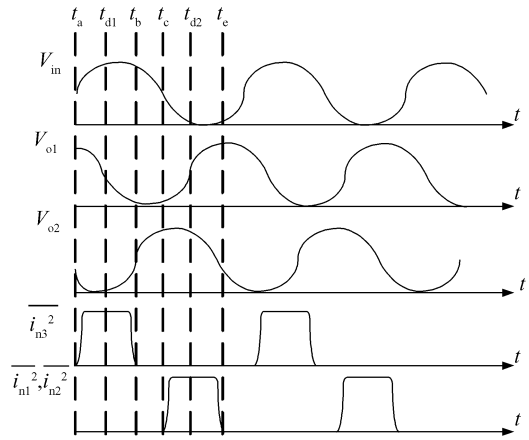

Fig. 8 Waveforms and 1st stage noise sources for the inverter cell delay cell

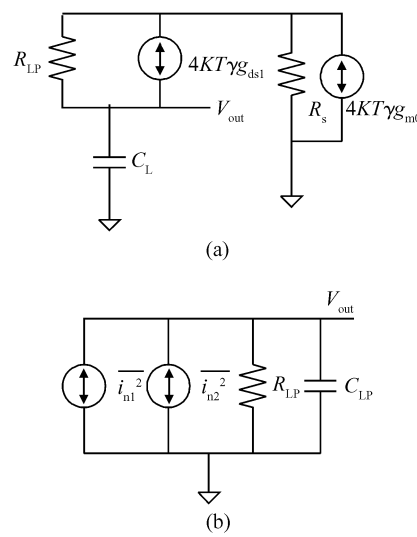

Fig. 9 Small signal equivalent circuits for the first stage at rising edge (a) Equivalent circuit for AC noise calculations; (b) Simplified AC noise calculations

stage, i. e., taking the inter stage influence into consideration, Figures 8～11 give waveforms and small signal equivalent circuits. Assuming the switching point happens at zero time, the ideal switching point for the output of the second stage is $2t_d$. But, random noise will force a deviation in the output voltage from the ideal switching point by Δt_d, the relationship of which is:

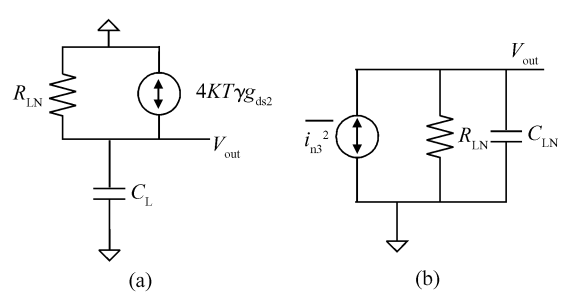

Fig. 10 Small signal equivalent circuits for first stage at falling edge (a) Equivalent circuit for AC noise calculations; (b) Simplified AC noise calculations

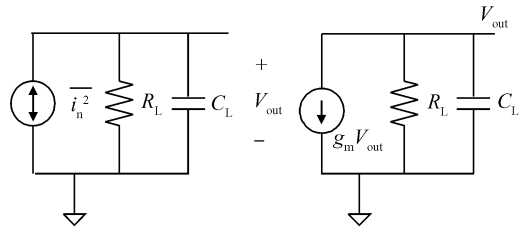

Fig. 11　Extended circuit model for the inter stage interaction

Table 1　Noise source of the first stage of delay cell

Noise generator	Region I ($t_a < t < t_b$)	Region II ($t_c < t < t_e$)
$\overline{i_{n1}^2}$	0	$4KT\gamma g_{m0}$
$\overline{i_{n2}^2}$	0	$4KT\gamma g_{ds1}$
$\overline{i_{n3}^2}$	$\overline{i_{n2}^2} = 4KT\gamma g_{ds2}$	0

$$\frac{\Delta t_{d,rms}}{t_d} = \frac{\Delta V_{n,rms}}{V_{ddi}} \tag{6}$$

This equation shows that the timing jitter per delay stage normalized to the time delay is equal to the RMS noise voltage at the output normalized to the voltage swing V_{ddi}.

Table 1 lists the noise source of the first stage of the delay cell in Fig. 7 (a). The deduction is similar to the Appendix in Ref. [6]. In this paper, complete results based on the third method are presented.

$$\overline{v_{n3}^2}(t) = \frac{KT}{2C_L} a_v^2 \gamma_2 R_{LP} g_{ds2} \lambda_{a1}(t) \tag{7}$$

$$\overline{v_{n1}^2}(t) + \overline{v_{n2}^2}(t) = \frac{KT}{2C_L} a_v^2 (\gamma_0 R_{LN} g_{m0} + \gamma_1 R_{LN} g_{ds1}) \lambda_{a2}(t) \tag{8}$$

$$\overline{v_n^2}(t) = \overline{v_{n1}^2}(t) + \overline{v_{n2}^2}(t) + \overline{v_{n3}^2}(t) \tag{9}$$

$$\lambda_{a1}(t) = 1 - [1 + 2at + 2(at)^2] e^{-2at} \tag{10}$$

$$\lambda_{a2}(t) = [1 + 2at + 2(at)^2] e^{-2at} \tag{11}$$

where $a = 1/R_L C_L$. Parameter γ is fairly close to the same parameter for devices in the triode region[12]. $\lambda_{a1}(t)$ and $\lambda_{a2}(t)$ are the factors that characterize the weight of the noise. Figure 12 shows the $\lambda_{a1}(t)$, $\lambda_{a2}(t)$ value at different V_{ddi}. When $V_{ddi} > 1.5$V, $\lambda_{a2}(2t_d) > 0.9$, which means $\overline{i_{n3}^2}$ contributes above 90% of the noise. This can be explained as the memory system, where the jitter in $2t_d$ is decided mostly by the noise source in the $t_a < t < t_b$ period in time-varying analysis.

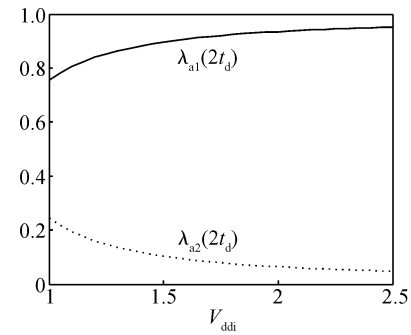

Fig. 12　λ factor versus V_{ddi}

If $R_{LP} = R_{LN}$, then $R_{LP} g_{ds2} = R_{LN} g_{ds1}$. Total voltage noise $\overline{v_n^2}(t)$ can be simplified by canceling Eq. (7) when adding Eqs. (7) and (8).

Therefore, the total output noise of the second stage can be expressed as

$$\overline{v_n^2}(t) = \frac{KT}{2C_L} a_v^2 \{\gamma + \gamma_0 g_{m0} R_{LN} \lambda_{a2}(t)\} \frac{KT}{2C_L} a_v^2 \xi_2^2 \tag{12}$$

Thus, parameter ξ can be obtained. Equation (13) is for CMOS inverter proposed in this work and Equation (14) for differential delay cells in Ref. [6].

$$\xi_2^2 = \gamma + \gamma_0 g_{m0} R_{LN} \lambda_{a2}(2t_d) \tag{13}$$

$$\xi_1^2 = 2\gamma_1 + 2\gamma_3 a_v \lambda_{a1}(2t_d) + \gamma_5 a_v \sqrt{2\alpha}(1+\beta) \lambda_{a2}(2t_d) \tag{14}$$

It is clear that $\xi_2 < \xi_1$ in these ways: (1) the differential delay cell has a symmetrical structure and good common mode noise rejection, but has twice the noise source of the CMOS inverter; (2) the CMOS inverter with current source degenerates g_{mp} and thus the noise source; and (3) If $R_{LP} = R_{LN}$, then $R_{LP} g_{ds2} = R_{LN} g_{ds1}$, canceling the $\lambda_{a1}(2t_d)$ item.

Table 2 summarizes the results of two different VCOs, which have similar forms for noise and RMS jitter of random noise. It can be deduced that RMS jitter in the proposed delay cell is one-tenth of that in the differential delay cell under the condition that V_{ddi} is 2V and $V_{gs} - V_t$ is 0.3V, and the other parameters in Table 2 are the same.

3.3　Voltage-to-current (V2I) block

The voltage-to-current circuit is quite important because it decides linearity, K_{vco}, and tuning range.

Table 2　Comparison between two VCO configurations

	Differential delay cell[6]	Proposed inverter delay cell
Voltage noise of one stage	$\overline{v_n^2} = \frac{KT}{2C_L} a_v^2 \xi_1^2$	$\overline{v_n^2}(t) = \frac{KT}{2C_L} a_v^2 \xi_2^2$
RMS jitter of VCO	$\Delta\tau_{vco} = \sqrt{\frac{KT}{\beta_n (V_{gs} - V_t)_5^2} \times \frac{a_v \xi_1^2}{2(V_{gs} - V_t)_3} T_o}$	$\Delta\tau_{vco} = \sqrt{\frac{KT}{\beta_n} \times \frac{h}{2} \times \frac{a_v^2 \xi_2^2}{2V_{ddi}^3} T_o}$

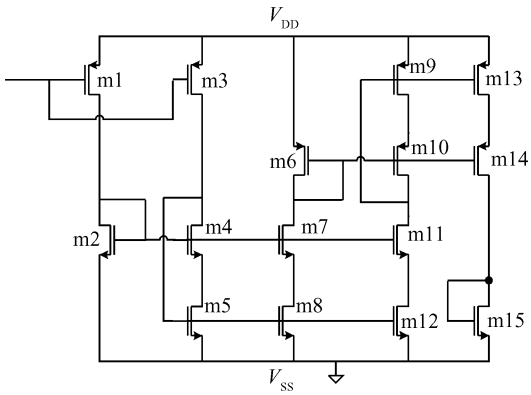

Fig. 13 Voltage-to-current circuit

K_{vco} influences phase noise by deciding the loop bandwidth. A large tuning range contributes to frequency stability if process and temperature variation are taken into consideration. The design of the V2I circuit shows trade off. The simplest implementation is one transistor because one single transistor serves as voltage to the current transformation. The simulation result in Fig. 14 (b) reveals that its K_{vco} is quite large, which deteriorates phase noise if the low pass filter noise cannot be ignored. Meanwhile, the linearity voltage range is 0.5～2.5V where oscillation frequency is linear. The K_{vco} around 1.25GHz is about 800MHz/V.

The proposed voltage-to-current circuit is shown in Fig. 13. One way to decrease K_{vco} is to design a V2I circuit that has a voltage gain that is smaller than one. The first and third stage of V2I uses diode connected transistors as load to increase linearity. The second stage uses a cascode configuration and the total gain is about 0.7. Figure 14 (a) shows the extension of the linearity range, which spans from 0 to 2.8V, while K_{vco} is about 600MHz/V at 1.25GHz. The tuning curve has different directions between Figs. 14 (a) and 14 (b) because of the three stages in the V2I circuit.

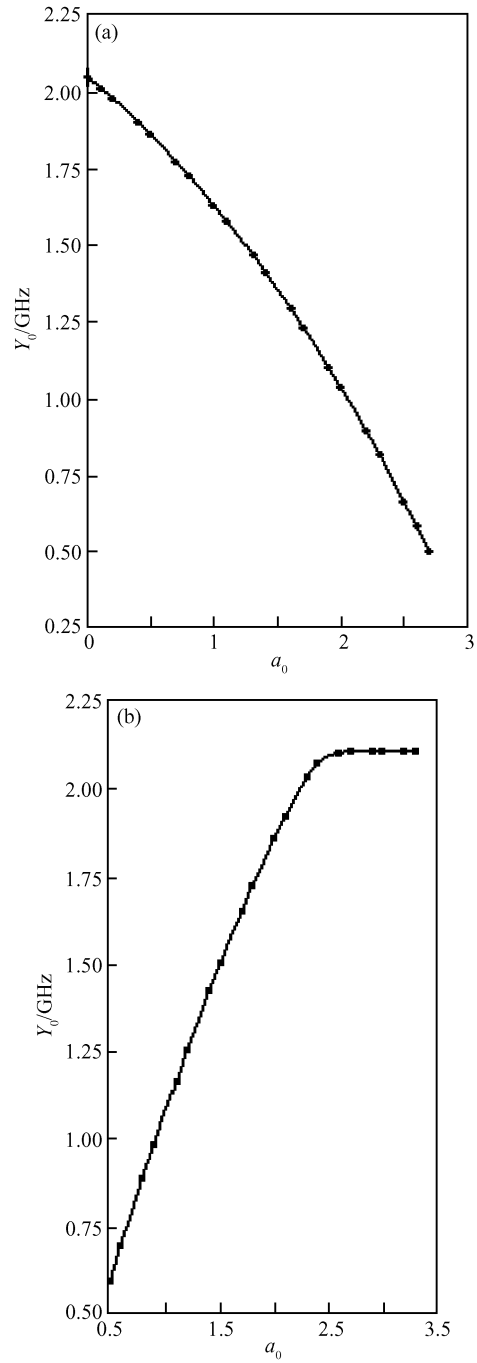

Fig. 14 Tuning curves of VCO (a) V2I block; (b) V2I single transistor

4 System considerations

In this section, we will introduce a new method to design the loop parameter in the TX_PLL. Bandwidth is the key parameter that determines phase noise and settling time and shows trade off in the design. The open loop transfer function can be expressed as

$$G(s) = \frac{K}{s}\left(1 + \frac{1}{s\tau_z}\right)\left(\frac{1}{1 + s\tau_z/b}\right) \quad (15)$$

$$K = RI_{cp}K_{vco}/(2\pi N) \quad (16)$$

$$\tau_z = RC_1 \quad (17)$$

where K can be approximately taken as the open loop bandwidth of PLL if b, the ratio of C_1 to C_2 in Fig. 2, is greater than 20. The phase margin is approximately:

$$PM = \arctan(K\tau_z) - \arctan(K\tau_z/b) \quad (18)$$

Combination of Eq. (19) makes sure of a 60° phase margin,

$$\begin{cases} b > 12 \\ \dfrac{b - \sqrt{b^2 - 12b}}{2\sqrt{3}} < K\tau_z < \dfrac{b + \sqrt{b^2 - 12b}}{2\sqrt{3}} \end{cases} \quad (19)$$

It should be also mentioned that $K\tau_z = (2\zeta)^2$, where ζ is damping factor in the second order system. Jitter peaking (JP) decreases with increasing $K\tau_z$ item, and a rough relationship between JP and ζ can be expressed as $20\lg JP = 2.172/\zeta^2$. If JP<1dB,

Table 3　Loop parameters

I_{cp}	R	C_1	C_2	JP
20μA	6kΩ	320pF	9pF	0.5dB
K_{vco}	N	BW	PM	
600MHz/V	10	2MHz	63°	

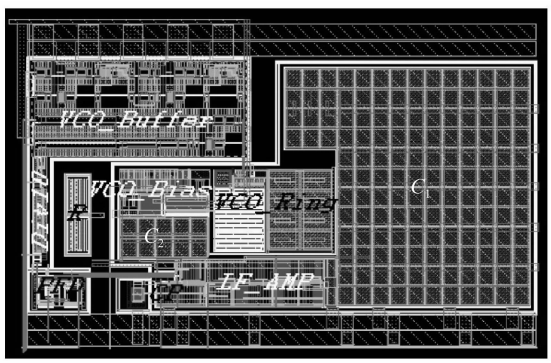

Fig.15　Layout of Tx PLL

$K_{\tau_z}=10$ should be insured. But at the same time, stability condition shows K_{τ_z} is limited by Eq.(19). To insure enough phase margin requirement, $b=35$ is also decided. The tough point here is how to decide value of bandwidth. Reference clock, 125MHz crystal oscillator has phase noise of -125dBc/Hz@100kHz and -140dBc/Hz@1MHz. Simulation shows 1.25GHz VCO output has phase noise of -65dBc/Hz @100kHz and -90 dBc/Hz@1MHz. Take trade off into consideration, 1MHz bandwidth is first confirmed. Then combine Eqs.(15)～(19), loop parameter is finally fixed on in Table 3.

5　Performance

Figure 15 shows the layout for the Tx PLL loop. Some layout methods, such as adding guard rings and coupling capacitance between V_{DD} and V_{GND}, and taking analog digital power input apart contribute to suppressing voltage coupling noise, thus compensating the drawback for single-ended ring oscillator.

Figure 16 is the serial output histogram measured at the end of 36″ SMA cables and 2″ trace connected to $D_{OUTp/n}$ with $R_p=147\Omega$ to gnd and ac-coupling cap

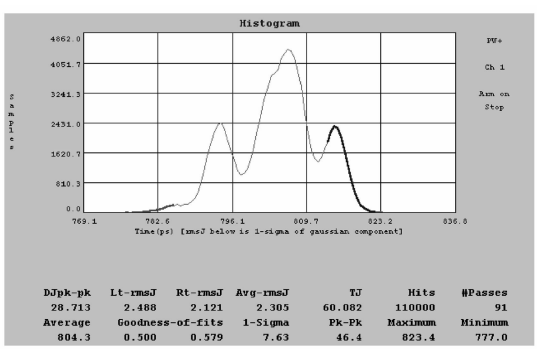

Fig.16　Histogram of series output

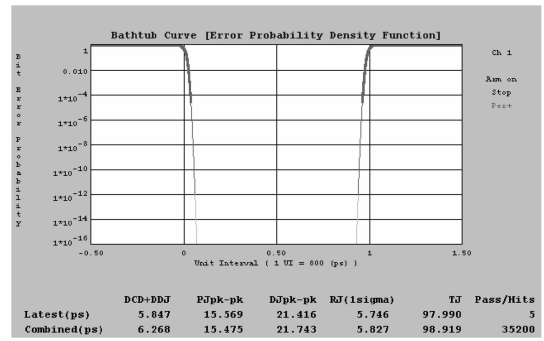

Fig.17　Output bathtub curve

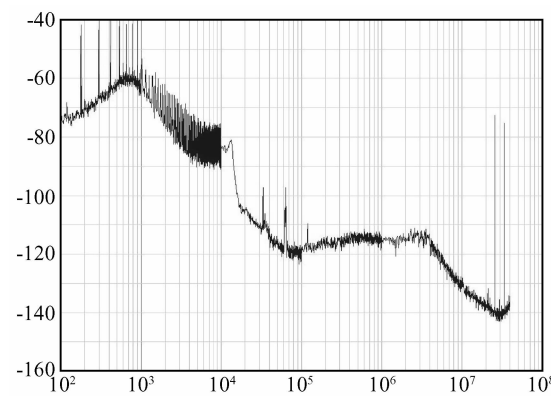

Fig.18　Phase noise of $D_{outp/n}$

$=0.1\mu$F, 1010101010 data pattern at 1.25GHz data rate. RJ RMS is 2.3ps (0.0015UI).

Figure 17 shows the serial output bath-tub curve measured in the same test environment and data out at 1×10^{-12} bit error probability. The test result shows that RJ (1 sigma) is 5.75ps (0.0035UI) with a single inverter stage $I_{avg}=290\mu$A, compared to 1-sigma $\sigma_x=$ 13ps(0.008UI) at $I_{EE}=400\mu$A in Ref.[7], which is implemented in a bipolar process and with a 622MHz center frequency.

Figure 18 shows the phase noise of $D_{outp/n}$ with a 1111100000 data pattern at 1.25GHz data rate. Measurement shows -120dBc/Hz@100kHz, compared to -124dBc/Hz @ 100kHz at 25MHz clock out in Ref.[14].

6　Conclusion

A comparison between a source coupled differential delay cell and a CMOS inverter is given, which shows many advantages for the inverter, especially with respect to RMS jitter and low power consumption. Voltage-to-current circuit design also reveals trades off between K_{vco} and the tuning range. The system considerations in section 4 are conductive for designing low-jitter PLL.

A low-jitter 1.25GHz Serdes was implemented in a 0.35μm standard 2P3M CMOS process. The results

Table 4 Performance comparison

Circuit	Process	Timing jitter	Area
Ref.[15]	0.35μm CMOS	11ps(RMS)	1mm×1mm
Ref.[16]	0.18μm CMOS	<7.2ps(RMS)	<0.3mm×0.8mm
Agilent Serdes	Bipolar	5.2ps(RMS)	——
This work	0.35μm CMOS	2.3ps(RMS)	0.7mm×0.45mm

shows good timing jitter and phase noise performance. Table 4 presents the performance comparison between 1.25GHz ring VCO based PLLs and shows that the configuration proposed in this paper is better for RMS timing jitter.

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用于 1.25GHz Serdes 的低时钟抖动的环振的设计

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摘要： 设计了一种新的用于电压控制振荡器的延迟单元，并与源级耦合差分延时单元的时钟抖动进行了比较. 提出了基于低时钟抖动的锁相环环路参数的优化技术. 在 0.35μm CMOS 工艺下进行 1.25GHz Serdes 流片，测试表明数据率为 1.25GHz 的高速串联输出的随机抖动均方根为 2.3ps(归一化为 0.0015UI)，随机抖动标准偏差为 0.0035UI. 在 1111100000 的数据输出时相位噪声为 −120dBc/Hz@100kHz.

关键词： 低时钟抖动；环振；电源噪声抑制；串并-并串转换

EEACC： 1205；1230；1280

中图分类号： TN432 **文献标识码：** A **文章编号：** 0253-4177(2008)03-0490-07

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2007-07-09 收到