A Near-1V 10ppm/℃ CMOS Bandgap Reference with Curvature Compensation*

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Abstract: A low voltage bandgap reference with curvature compensation is presented. Using current mode structure, the proposed bandgap circuit has a minimum voltage of 900mV. Compensated through the V_{EB} linearization technique, this bandgap reference can reach a temperature coefficient of 10ppm/℃ from 0 to 150℃. With a 1.1V supply voltage, the supply current is 43μA and the PSRR is 55dB at DC frequency. This bandgap reference has been verified in a UMC 0.18μm mixed mode CMOS technology and occupies 0.186mm^2 of chip area.

Key words: CMOS bandgap reference; low voltage; curvature compensation
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1 Introduction

Since introduced in 1970s by Widlar[1] and Brokaw[2], the bandgap reference is widely used in analog and mixed-mode integrated circuits, such as data converters and DC-DC power converters. In the CMOS bandgap reference design, low voltage and high precision are two important design criteria. Because of the common mode input voltage of the operational transconductance amplifier (OTA) and the bandgap voltage of silicon (about 1.25V), conventional CMOS bandgap reference usually has a minimum voltage of 1.8V. Several factors constrain the precision of the bandgap reference, such as non-linearization of the emitter-base voltage (V_{EB}) in BJT, the offset of the OTA, and the non-zero temperature coefficient of resistors. Thus, the temperature coefficient of the bandgap reference without curvature compensation is usually greater than 30ppm/℃. To solve the first problem, Jiang and Lee[3] replaced OTA with an operational trans-impedance amplifier; without the constraint of common mode input voltage of OTA, the circuit worked with a supply voltage of 1.2V. Banba *et al*. and Leung *et al*. presented two different current mode structures that transformed the addition of two voltages to an addition of two currents[4,5]. The reference voltage generated by the sum current is adjustable, breaking the constraint of the bandgap voltage. To improve the precision, several high order curvature compensations have been introduced. Leung *et al*.[6] developed a second-order curvature compensation using resistors with opposing temperature coefficients. Audy[7] further proposed a third order curvature compensation based on series and parallel combinations of two kinds of resistors. Malcovati *et al*.[8] introduced a new method, which generated a nonlinear current to compensate the nonlinear V_{EB} of BJT.

The bandgap reference presented in this paper adopts a current mode structure that can reduce supply voltage effectively. To obtain high precision, a V_{EB} linearization technique is applied to the bandgap reference. To reduce the systemic offset of the feedback OTA further, a symmetric OTA is chosen.

2 Principle and design challenges of CMOS bandgap reference

2.1 Principle of CMOS bandgap reference

The basic principle of a CMOS bandgap reference is to compensate the negative-temperature-coefficient V_{EB} of BJT with a positive-temperature-coefficient voltage. The difference of V_{EB} of BJTs with different current densities is proportional to absolute temperature (PTAT). A conventional CMOS implementation is shown in Fig. 1. The output reference can be written as:

$$V_{REF} = V_{EB1} + \left(1 + \frac{R_2}{R_1}\right)\frac{kT}{q}\ln n \qquad (1)$$

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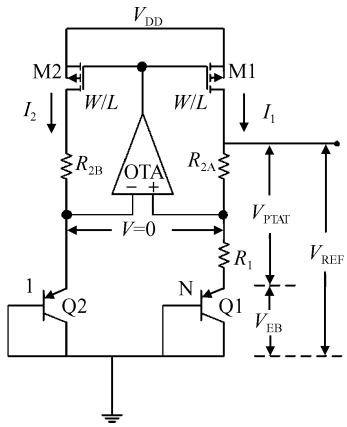

Fig. 1 Conventional CMOS bandgap circuit

where $R_{2A} = R_{2B} = R_2$, and n is the ratio of emitter areas of Q1 and Q2. If the resistor ratio is correct, the second term, which has a positive temperature coefficient, can cancel the negative temperature coefficient of V_{EB}.

2.2 Design challenges of a CMOS bandgap reference

The V_{REF} is about 1.25V when it is independent of temperature, so the minimum supply voltage is:

$$\min\{V_{DD}\} = V_{REF} + V_{SDsat1} \tag{2}$$

where V_{SDsat1} is the source-drain saturation voltage of transistor M1 in Fig. 1. The common mode input range of the OTA also decides the supply voltage. When the OTA has an nMOS input stage, the minimum supply voltage is[3]:

$$\min\{V_{DD}\} = V_{EB2} + V_{SDsat} + V_{R_2} \tag{3}$$

When the input stage is a pMOS, the minimum supply voltage is[3]:

$$\min\{V_{DD}\} = V_{EB2} + |V_{thp}| + 2V_{SDsat} \tag{4}$$

In fact, the V_{EB} of BJT is nonlinear[8]:

$$V_{EB} = V_G(T_r) + \frac{T}{T_r}[V_{EB}(T_r) - V_G(T_r)] + (\eta - m)\frac{kT}{q}\ln\frac{T_r}{T} \tag{5}$$

where T is the absolute temperature, T_r is a reference temperature, V_G is the bandgap voltage of silicon, η is a constant depending on doping level, and m is a constant depending on the temperature character of emitter current in BJT. Thus, the output reference cannot be purely temperature independent[5]. In CMOS technology, the offset of the OTA can reach 30mV, which cannot be neglected in circuit design. Including offset, the reference voltage becomes[9]:

$$V_{REF} = V_{EB1} + \frac{R_1 + R_2}{R_1}\left(\frac{kT}{q}\ln n - V_{OS}\right) \tag{6}$$

where V_{OS} is the input offset voltage of the OTA. Some other factors like non-ideal resistors, non-zero base current in BJT, and a mismatch between resistors also constrain the precision of the output reference[10].

3 Low voltage high precision bandgap reference

3.1 Current mode and VEB linearization

To meet the challenges described above, some new techniques must be applied to the conventional bandgap reference. A current mode structure is a simple and effective method to reduce the supply voltage, and also has the advantage of an adjustable output reference. The implementation is shown in the middle of Fig. 2[4,8]. Because of the feedback loop, the nodes A and B have the same voltage, so the difference between V_{EB} of Q1 and Q2 is applied to R_1. The current I_1 is PTAT. The current I_2 is proportional to V_{EB2}, which is approximately complementary to absolute temperature (CTAT). With a proper ratio of R_1 to R_2, the drain currents of M1～M4 are temperature independent. With a PTAT bias current, the V_{EB} of Q2 is[8]:

$$V_{EB2} = V_G(T_r) + \frac{T}{T_r}[V_{EB}(T_r) - V_G(T_r)] + (\eta - 1)\frac{kT}{q}\ln\frac{T_r}{T} \tag{7}$$

While the V_{EB} of Q3 is[8]:

$$V_{EB3} = V_G(T_r) + \frac{T}{T_r}[V_{EB}(T_r) - V_G(T_r)] + \eta\frac{kT}{q}\ln\frac{T_r}{T} \tag{8}$$

The current I_3 is nonlinear, and can be used to linearize V_{EB} further:

$$I_3 = (V_{EB2} - V_{EB3})/R_3 = -\frac{kT}{q}\ln(T_r/T)/R_3 \tag{9}$$

The output reference is the voltage drop of the sum current in resistor R_4:

$$V_{REF} = (I_1 + I_2 + I_3)R_4 = \left[\frac{kT}{q}\times\frac{\ln n}{R_1} + \frac{V_{EB2}}{R_2} - \frac{V_T\ln\left(\frac{T_r}{T}\right)}{R_3}\right]R_4 \tag{10}$$

A temperature independent current can be obtained through adjusting R_1～R_3, and the output reference is adjustable because the value of R_4 is variable.

3.2 OTA design

The feedback OTA is shown in the left of Fig. 2. To improve the stabilization of OTA, the bias current of OTA is a copy of the current in transistors M1～M4, which is independent of supply voltage and temperature. Reducing the offset is the most important objective in OTA design. Offset consists of two parts: systemic offset and random offset. For random offset, two methods can be used: a large input stage and a common-centroid layout design. For systemic offset,

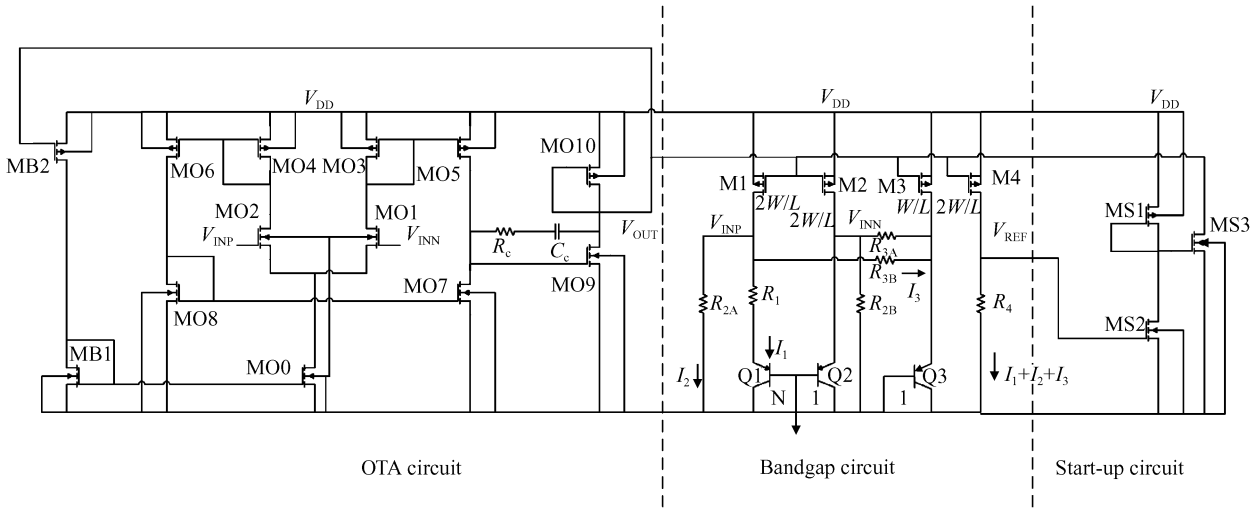

Fig. 2 Complete schematic of the proposed low voltage high precision bandgap reference

the only solution is to choose a better structure. In CMOS differential OTAs, a symmetric OTA has the least offset. Because in the symmetric OTA, two input transistors have the same load (a diode-connected transistor), so the difference of V_{DS} between input transistors is the smallest in all differential OTAs.

3.3 Resistor selection

Nonlinear behavior of V_{EB} leads to the finite temperature coefficient of V_{REF}. When resistors are implemented by lower-temperature-coefficient material, the term $\ln(T_r/T)\times kT/q$ in Eq. (5) is smaller, leading to a better V_{EB} stabilization[11]. Thus, the non-silicide n+ poly resistor is selected in this design.

3.4 Start-up circuit

To prevent bandgap circuit from working on the zero working point, a start-up circuit formed by MS1 ~ MS3 is needed, which is shown in the right of Fig. 2. When the circuit works on zero working point, V_{REF} is zero, the gate voltage of MS3 is $V_{DD}-|V_{thp}|$, which drives MS3 on, V_{OUT} is then pulled down, and the circuit starts up to the normal working point. When the circuit works on the normal working point, choosing proper sizes of MS1, MS2, the gate voltage of MS3 is lower than the threshold voltage, cutting off MS3, and the start-up circuit does not affect the working state of the bandgap circuit.

3.5 Output buffer

So as to drive a heavy load, an ideal voltage reference has a zero output resistor. In the presented bandgap reference, the output resistor equals R_4, which is several hundreds thousands Ohms. A simple method to reduce the output resistor is to add an output buffer to the bandgap reference. The output buffer consisted of an operational amplifier with voltage-voltage negative feedback and has an infinite input resistor and a near-zero output resistor.

4 Measuremental results

The presented bandgap reference has been fabricated in a UMC 0.18μm mixed-mode process. The threshold voltage of this process is V_{thn} = 0.31V, $|V_{thp}|$ = 0.46V at 0℃. The micrograph of the bandgap reference die is shown in Fig. 3. There are two bandgap circuits in this die, with the upper one for testing. Each bandgap circuit occupies 0.186mm^2 of chip area. The measured results of supply voltage dependences of the bandgap reference at 0, 30 and 100℃ are shown in Fig. 4. The line regulation is about 5.2mV/V in the worst case. The output reference varies with supply voltage because of the finite gain of the feedback OTA. When the voltage is higher than 2.6V, the gain falls rapidly, causing a large rise in reference voltage. The measured temperature dependences of the bandgap reference with different supply

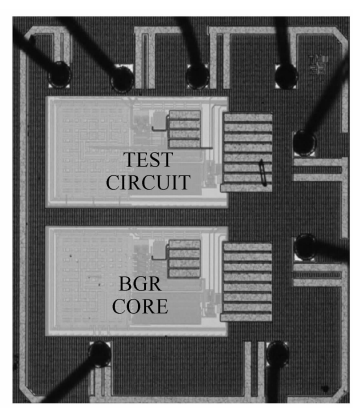

Fig. 3 Micrograph of the bandgap reference die

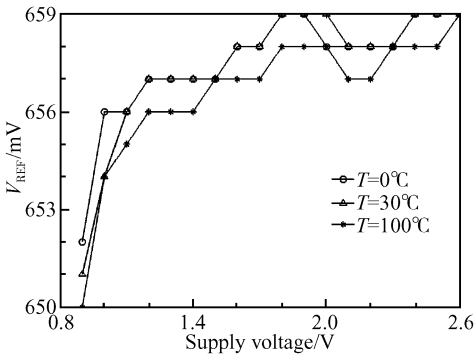

Fig. 4　Measured supply voltage dependences of the bandgap reference at 0, 30 and 100℃

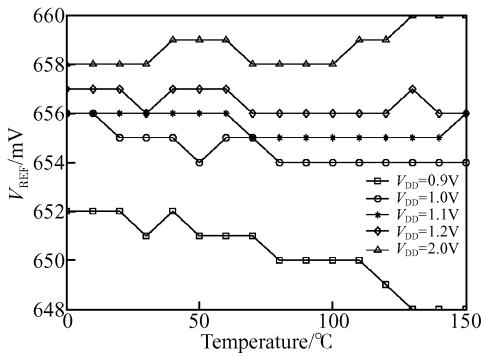

Fig. 5　Measured temperature dependences of the bandgap reference with different V_{DD}

voltages are shown in Fig. 5. In the range from 0 to 150℃, the best cases are when V_{DD} = 1.1V and V_{DD} = 1.2V, with a temperature coefficient of 10ppm/℃; the case of V_{DD} = 0.9V is the worst, with a temperature of 40ppm/℃; the cases of V_{DD} = 1.0V and V_{DD} = 2.0V are in the middle, the temperature coefficient of which is 20ppm/℃. The main reasons that output reference varies with temperature are the mismatch between resistors, non-ideal resistors, and the input offset voltage of the OTA.

The simulation and measurement performances are compared in Table 1, where PSRR is the power supply rejection ratio. Table 2 is a comparison with other reported low voltage, high precision bandgap references.

Table 1　Comparison of simulation and measurement performances

Performance	Simulation	Measurement
Temperature coefficient /(ppm/℃)	2～11	10～40
Line regulation/(mV/V)	1.6	5.2
PSRR/dB@DC	−60	−55
Power/μW	40	47

Table 2　Comparison of low-voltage high-precision bandgap references

	This work	Leung *et al*.[5]	Malcovati *et al*.[8]
Process	0.18μm CMOS	0.6μm CMOS	0.8μm BICMOS
Threshold voltage	V_{thn} = 0.31V, $\lvert V_{thp}\rvert$ = 0.46V	V_{thn} = 0.9V, $\lvert V_{thp}\rvert$ = 0.9V	–
Best case voltage /V	1.1	0.98	0.95
Supply current /μA	43	18	92
V_{REF}/mV	657	603	536
TC (best case) /(ppm/℃)	10	15	19

5　Conclusion

A near-1V 10ppm/℃ CMOS bandgap reference that is independent of supply voltage has been presented. Because of its high PSRR (−55dB) and low power (47μW), this bandgap reference is suitable for portable SOC applications. Since there is no special process used in this work, it is reproducible in any CMOS process. If needed, the supply voltage can be reduced further to $V_{EB} + \lvert V_{DSsat}\rvert$. To further improve the TC performance, careful optimization of the OTA design and layout is needed, and other high order curvature compensations can also be used.

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一个电压接近 1V 10ppm/℃带曲率补偿的 CMOS 带隙基准源*

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摘要：介绍了一个带曲率补偿的低电压带隙基准源.由于采用电流模结构,带隙基准源的最低电源电压为 900mV.通过 V_{EB}线性化补偿技术,带隙基准源在 0 到 150℃的温度范围内的温度系数为 10ppm/℃.在电源电压为 1.1V 时,电源电流为 43μA,低频的 PSRR 为 55dB.该带隙基准源已通过 UMC 0.18μm 混合信号工艺验证,芯片面积为 0.186mm^2.

关键词：CMOS 带隙基准源；低电源电压；曲率补偿
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