1. 0µm Gate-Length GaAs MHEMT Devices and SPDT Switch MMICs*

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Abstract: $1.0\mu m$ gate-length GaAs-based MHEMTs have been fabricated by MBE epitaxial material and contact-mode lithography technology. Pt/Ti/Pt/Au and Ti/Pt/Au were evaporated to form gate metals. Excellent DC and RF performances have been obtained, and the transconductance, maximum saturation drain current density, threshold voltage, current cut-off frequency, and maximum oscillation frequency of Pt/Ti/Pt/Au and Ti/Pt/Au MHEMTs were $502(503)\,mS/mm$, $382(530)\,mA/mm$, $0.1(-0.5)\,V$, $13.4(14.8)\,GHz$, and $17.0(17.5)\,GHz$, respectively. DC-10GHz single-pole double-throw (SPDT) switch MMICs have been designed and fabricated by Ti/Pt/Au MHEMTs. Insertion loss, isolation, input, and output return losses of SPDT chips were better than 2.93,23.34, and 20dB.

Key words: MHEMT; Pt/Ti/Pt/Au; Ti/Pt/Au; SPDT; MMIC

EEACC: 1350A; 2560S

1 Introduction

Lattice matched InP-based HEMTs have performance advantages over GaAs-based PHEMTs due to their high electron velocity and 2-DEG density^[1]. However, InP substrates are brittle, small, and expensive, and it is difficult to fabricate InP-based HEMTs at a high production level. GaAs-based MHEMTs were grown on semi-insulating GaAs substrates using a grading In content metamorphic buffer (M-buffer). MHEMTs have advantages of both InP-based HEMTs and GaAs substrates. Recently, GaAs-based MHEMTs by MBE material have emerged as an attractive, low cost alternative to InP-based HEMTs for high performance, low noise, and power applications^[2~5].

 $1.0\mu m$ gate-length GaAs-based MHEMTs have been fabricated and excellent DC and RF performances have been achieved. Pt/Ti/Pt/Au and Ti/Pt/Au were evaporated to form both gate metals. $G_{\rm m}$, $J_{\rm DSS}$, $V_{\rm T}$, $f_{\rm T}$, and $f_{\rm max}$ of Pt/Ti/Pt/Au and Ti/Pt/Au MHEMTs are $502\,(503)\,{\rm mS/mm}$, $382\,(530)\,{\rm mA/mm}$, $0.1(-0.5)\,{\rm V}$, $13.4\,(14.8)\,{\rm GHz}$, and $17.0\,(17.5)\,{\rm GHz}$, respectively. In addition, DC-10GHz SPDT switch MMICs have been designed and fabricated by Ti/Pt/Au MHEMTs. Insertion loss, isolation, and return loss

of SPDT switches were better than 2.93, 23.34, and 20dB. This is very helpful for the further investigation of MHEMT devices and MMICs.

2 Device fabrication

The epitaxial wafers grown on semi-insulting GaAs substrates by MBE technology were provided by the Institute of Physics, Chinese Academy of Sciences. The structure is composed of a 300nm GaAs layer, a 1000nm In composition grading M-buffer, an 18nm InGaAs channel (In composition is 0.6), a 4nm InAlAs spacer, a planar doping layer, an 18nm InAlAs Schottcky barrier layer, and a 20nm n⁺ InGaAs cap layer.

The source and drain electrodes of GaAs-based MHEMTs were fabricated by conventional evaporation and lift-off processes. After annealing, a typical ratio ohmic contact resistance of $4\times10^{-7}\,\Omega$ • cm² was obtained. Mesa-isolation was completed by wetetching. Contact-mode lithography technology was used to obtain a 1.0 μ m gate pattern. Citric acid-H2O2 solution was used for the gate recess process. Pt/Ti/Pt/Au and Ti/Pt/Au were evaporated to form the gate metal, respectively. The first and second metal lines were Ti/Au. The picture of the MHEMT device is shown in Fig. 1.

^{*} Project supported by the State Key Development Program for Basic Research of China (No. G2002CB311901), the Equipment Investigation Program in Advance (No. 61501050401C), and the Institute of Microelectronics, Chinese Academy of Sciences, Dean Fund (No. O6SB124004)

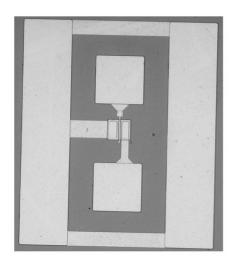


Fig. 1 1. 0μm gate-length MHEMT device

3 Results and analysis

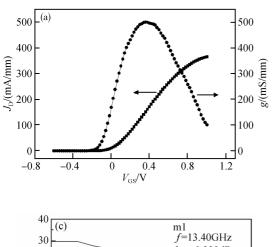
Both MHEMT devices exhibit excellent DC and RF performances. The results of the Pt/Ti/Pt/Au MHEMT (1.0 μ m gate length, 30μ m gate width) are shown in Fig. 2. $V_{\rm T}$, $g_{\rm m}$, $J_{\rm DSS}$, $f_{\rm T}$, and $f_{\rm max}$ are 0.1V, $502\,{\rm mS/mm}$ ($V_{\rm DS}=1{\rm V}$, $V_{\rm GS}=0.35{\rm V}$), $382\,{\rm mA/mm}$, $13.4\,{\rm GHz}$, and 17.0 GHz, respectively. The results of the Ti/Pt/Au MHEMT (1.0 μ m gate length, $20 \,\mu$ m gate width) are shown in Fig. 3. $V_{\rm T}$, $g_{\rm m}$, $J_{\rm DSS}$, $f_{\rm T}$, and $f_{\rm max}$ are $-0.5\,{\rm V}$, $503\,{\rm mS/mm}$ ($V_{\rm DS}=1{\rm V}$, $V_{\rm GS}=-0.2\,{\rm V}$),

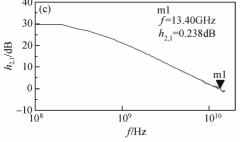
530mA/mm, 14.8GHz, and 17.5GHz, respectively.

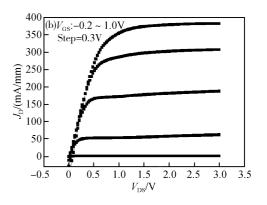
Because Pt-based buried-gate metals were chosen, during the process of annealing, Pt-InAlAs reaction occured and Pt sunk into the InAlAs layer to reduce the distance between gate and channel, and the $V_{\rm T}$ of the Pt/Ti/Pt/Au MHEMT increased positively while the $V_{\rm T}$ of the Ti/Pt/Au MHEMT remained negative. Due to different characteristics of Pt/Ti/Pt/Au and Ti/Pt/Au during annealing, positive and negative threshold voltages have been achieved, respectively.

Nine-stage ring oscillators have been designed and fabricated by 1.0 μ m gate-length Pt/Ti/Pt/Au and Ti/Pt/Au MHEMTs. Oscillators contain nine-stage DCFL inverters and a three-stage DCFL inverter output buffer. When the supply voltage is 1.2V, the oscillation frequency is 777.6MHz, and the gate delay time is 71.4 ps. The testing results of the ring oscillators are shown in Fig. 4.

DC-10GHz SPDT switch MMICs have been designed and fabricated by Ti/Pt/Au MHEMTs. The topology of the SPDT switch was a series-shunt structure, containing 6 MHEMTs (1.0 μ m gate length, 4 × 50 μ m gate width), and the chip size is 1.0mm × 1.0mm. The results of SPDT switches on-wafer testing are shown in Fig. 5. Insertion loss, isolation, input, and output return losses are better than 2.93, 23.34, and 20dB.







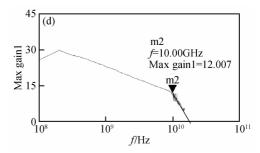


Fig. 2 DC and RF characteristics of Pt/Ti/Pt/Au MHEMT

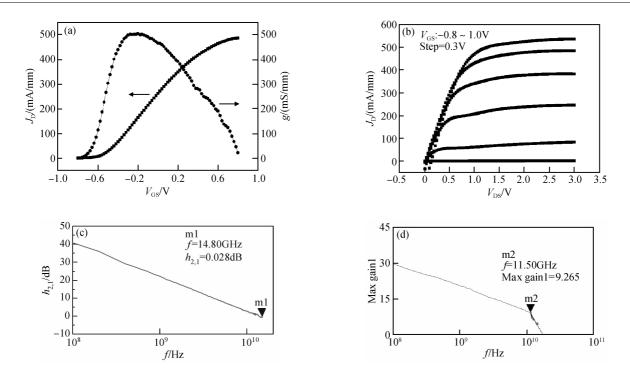


Fig. 3 DC and RF characteristics of Ti/Pt/Au MHEMT

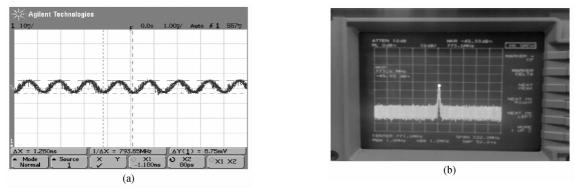


Fig.4 Output wave of nine-stage ring oscillator (a) and result of spectrum analyzer test (b)

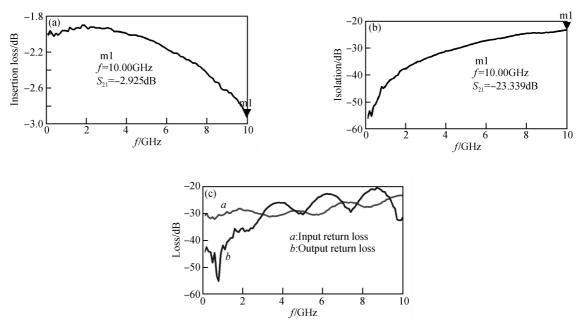


Fig. 5 Insertion loss, isolation, and return loss of SPDT switches

4 Conclusion

1. 0μm gate-length GaAs-based MHEMT devices, nine-stage ring oscillator and DC-10GHz SPDT switch MMICs have been designed and fabricated by MBE epitaxial material and contact-mode photolithography technology. Pt/Ti/Pt/Au and Ti/Pt/Au were evaporated to form gate metal, respectively. $G_{\rm m}$, $J_{\rm DSS}$, $V_{\rm T}$, $f_{\rm T}$, and $f_{\rm max}$ of both MHEMTs are 502(503) mS/mm, $382(530) \,\text{mA/mm}$, 0. $1(-0.5) \,\text{V}$, 13. $4(14.8) \,\text{GHz}$, and 17. 0(17. 5) GHz, respectively. When the supply voltage is 1.2V, the oscillation frequency and gate delay time of the nine-stage ring oscillators are 777.6MHz and 71. 4ps. Insertion loss, isolation, input, and output return losses of the SPDT chips are better than 2.93, 23. 34, and 20dB. Performances of both devices and circuits can be improved further by optimizing the material structure, switch model, the design of devices and circuits, as well as processing conditions.

References

- [1] Yamashita Y, Endoh A, Shinohara K, et al. Pseudomorphic $In_{0.52}$ $Al_{0.48}$ As/ $In_{0.7}$ Ga_{0.3} As HEMTs with an ultrahigh f_T of 562GHz. IEEE Electron Device Lett, 2002, 23(10);573
- ☐ Second Performance improvement in tensile-strained In_{0.5} Al_{0.5} As/In_x Ga_{1-x} As/In_{0.5} Al_{0.5} As metamorphic HEMT. IEEE Trans Electron Devices, 2006, 53(3), 406
- [3] Leuther A. Tessmann A. Dammann M. et al. 50nm MHEMT technology for G- and H-Band MMICs. International Conference on Indium Phosphide and Related Materials. 2007:24
- [4] Hsu W, Chen Y J, Lee C S, et al. Characteristics of In_{0.425} Al_{0.575}-As-In_x Ga_{1-x} As metamorphic HEMTs with pseudomorphic and symmetrically graded channels. IEEE Trans Electron Devices, 2005,52(6):1079
- [5] Shi Huafen, Liu Xunchun, Zhang Haiying, et al. 0. 25μm GaAsbased MHEMT device. Chinese Journal of Semiconductors, 2004, 25(3); 325 (in Chinese) [石华芬, 刘训春, 张海英, 等. 0. 25μm GaAs 基 MHEMT 器件. 半导体学报, 2004, 25(3); 325]

1. 0µm 栅长 GaAs 基 MHEMT 器件及 SPDT 开关 MMIC*

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摘要:利用 MBE 外延材料和接触式光学光刻方式,成功制备出 $1.0\mu m$ 栅长 GaAs 基 MHEMT 器件,分别蒸发 Pt/Ti/Pt/Au 和 Ti/Pt/Au 作为栅电极金属. 获得了优越的 DC 和 RF 性能,Pt/Ti/Pt/Au 和 Ti/Pt/Au MHEMT 器件的 g_m 为 502(503) mS/mm, J_{DSS} 为 382(530) mA/mm, V_T 为 0.1(-0.5) V, f_T 和 f_{max} 分别为 13.4(14.8),17.0(17.5) GHz. 利用单片集成增强/耗尽型 GaAs 基 MHEMT 器件制备出九阶环型振荡器,直流电压为 1.2 V 时,振荡频率达到 777.6 MHz,门延迟时间为 71.4 ps. 利用 Ti/Pt/Au MHEMT 器件设计并制备出了 DC-10 GHz 单刀双掷(SPDT)开关 MMIC,其插入损耗、隔离度、输入输出回波损耗分别优于 2.93,23.34 和 20 dB.

关键词: MHEMT; Pt/Ti/Pt/Au; Ti/Pt/Au; SPDT; MMIC

EEACC: 1350A; 2560S

中图分类号: TN386 文献标识码: A 文章编号: 0253-4177(2008)04-0668-04

^{*} 国家重点基础研究发展规划 (批准号:G2002CB311901),装备预先研究基金(批准号:61501050401C)和中国科学院微电子研究所所长基金(批准号:G6SB124004)资助项目

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