A Novel Technique for Improving Temperature Independence of Ring-ADCs

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Abstract: A new temperature compensation technique for ring-oscillator-based ADCs is proposed. This technique employs a novel, fixed-number-based algorithm and CTAT current biasing technology to compensate the temperature-dependent variations of the output, thus eliminating the need for digital calibrations. Simulation results prove that, with the proposed technique, the resolution in the temperature range of 0 to 100℃ can reach a 2mV quantization bin size with an input voltage span of 120mV at the sampling frequency of $f_s = 100$kHz.

Key words: ring ADC; CTAT; temperature compensation; VLSI
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1 Introduction

Windowed analog-to-digital converters (ADCs) are widely used in digital DC-DC converters due to the fact that the output voltage is regulated in the vicinity of the reference voltage. In recent years, synthesizable windowed ADCs based on delay-line[1~3], or ring-oscillator[4,5] structures have been reported. These structures have the advantages of low-power, low-area, and high-resolution so that they are very suitable for digital DC-DC applications. However, one severe problem is that the digital output data is temperature-dependent since the delay of the delay-cells cannot be precisely controlled against temperature variations. Digital calibrations can be accomplished in a number of ways. A simple strategy is to subtract a reference value from the converted output[1]. Since the variations of the digital output due to temperature variation are not pure DC offset, this type of calibration may be imprecise. A look-up table or a LSI solution[6] can improve the precision. However, it will take a large chip area and will increase the circuit's complexity and power consumption. A detailed comparison will be given in section 6.

In this paper, we propose a novel temperature compensation technique for ring-oscillator-based ADCs. We put forward a fixed-number-based algorithm and a complementary-to-absolute-temperature (CTAT) current biasing scheme. With our technique, a ring-ADC can achieve dramatic temperature independence without complex digital calibrations. We have not found any published ring-ADCs adopting this type of temperature compensation.

The proposed ring-ADC has been simulated with a typical 0.35μm CMOS mixed signal process (Charted). For comparison, a traditional ring-ADC that employs a normal fixed-time-based algorithm[5] and conventional biasing current source is also simulated. Results reveal that, in the temperature range of 0 to 100℃, the input voltage span of 120mV, and the sampling frequency of 100kHz, the proposed ring-ADC can reach a 2mV quantization bin size while an uncompensated ring-ADC reaches only 16mV.

2 System architecture

The principle of the proposed temperature compensation technique is explained with a ring-ADC system, shown in Fig. 1. It consists of a CTAT biasing current source, a ring oscillator pair, and a synthesizable digital block.

The CTAT biasing current source is used to generate a temperature compensated current for the two

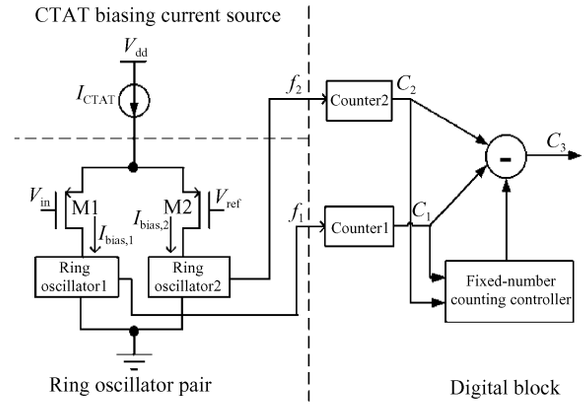

Fig. 1 Schematic of a ring-ADC system using the proposed temperature compensation technique

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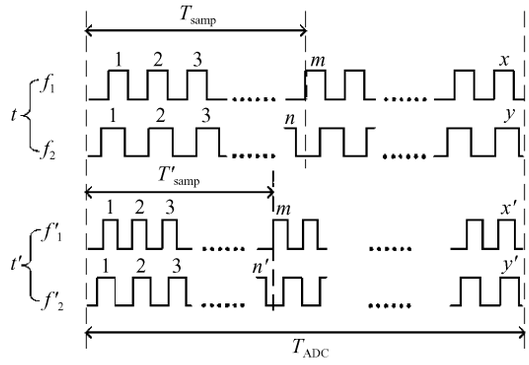

Fig. 2　Derivation of C_e under different temperatures, using fixed-time (top) and fixed-number (bottom) based algorithms

ring-oscillators. The error voltage between V_{in} and V_{ref}, denoted with V_e, brings on error current between two branches, $I_{bias,1} - I_{bias,2}$, thus different frequencies at the two ring-oscillators are generated. The two frequencies are captured by two counters, and then our fixed-number-based algorithm is applied to derive the temperature-independent output.

3　Fixed-number-based algorithm

The right side of Fig. 1 can also be used to explain the fixed-time algorithm[5] if we replace the module fixed-number counting controller with a fixed-time controller. The counters are reset at the beginning of each sampling cycle and stopped after a fixed period of time. Then, one counter's output is subtracted from the other. The result, C_e, is given by[5]:

$$C_e = T_{ADC} K_f (I_{bias,1} - I_{bias,2}) \tag{1}$$

where T_{ADC} is the ADC sampling period, and K_f is the constant characterizing the ring oscillator frequency sensitivity to its biasing current. $I_{bias,1}$ and $I_{bias,2}$ are the biasing currents of the two branches. The digitized error voltage can be calculated by scaling C_e. The error frequency is

$$f_e = f_1 - f_2 = K_f (I_{bias,1} - I_{bias,2}) \propto V_e \tag{2}$$

where V_e is the error input voltage. Then,

$$C_e = T_{ADC}(f_1 - f_2) = T_{ADC} f_e \tag{3}$$

When temperature migrates from t to t', we assume $I_{bias,1}$, $I_{bias,2}$, f_1, f_2 change to $I'_{bias,1}$, $I'_{bias,2}$, f'_1, f'_2, respectively. The following discussion will show that in our solution, the CTAT current biasing will make $I_{bias,1}/I_{bias,2}$ independent of the temperature. That is to say, when temperature migrates from t to t', $I'_{bias,1}/I'_{bias,2} = I_{bias,1}/I_{bias,2}$, and consequently $f'_1/f'_2 = f_1/f_2$.

Then, according to Fig. 2, we have:

$$C_e|_{t,\text{fixed-time}} = x - y = T_{ADC}(f_1 - f_2) = T_{ADC} f_e \tag{4}$$

$$C_e|_{t',\text{fixed-time}} = x' - y' = T_{ADC}(f'_1 - f'_2) = T_{ADC}\left(f'_1 - f'_1 \frac{f_2}{f_1}\right) = T_{ADC} \frac{f'_1}{f_1}(f_1 - f_2) \tag{5}$$

Obviously, C_e changes with the temperature, implying that, with the fixed-time-based algorithm, C_e varies with the temperature and cannot reflect V_e accurately.

In the proposed fixed-number-based algorithm, the counters are also reset at the beginning of each sampling cycle but stopped when the first counter's output reaches a fixed-number m in Fig. 2. Then, Equations (4) and (5) can be rewritten as:

$$C_e|_{t,\text{fixed-number}} = m - n = T_{samp}(f_1 - f_2) = T_{samp} f_e \tag{6}$$

where

$$T_{samp} = \frac{m}{f_1} \tag{7}$$

$$C_e|_{t',\text{fixed-number}} = m - n' = T'_{samp}(f'_1 - f'_2) = T'_{samp} \frac{f'_1}{f_1}(f_1 - f_2) \tag{8}$$

where

$$T'_{samp} = \frac{m}{f'_1} = \frac{T_{samp} f_1}{f'_1} \tag{9}$$

Substituting Eq. (9) into Eq. (8), we get:

$$C_e|_{t',\text{fixed-number}} = T_{samp}(f_1 - f_2) = T_{samp} f_e = C_e|_{t,\text{fixed-number}} \tag{10}$$

Thus, a temperature-independent C_e can be obtained.

Conclusion 1: With the Fixed-Number-Based algorithm, the output of the frequency-ADC will be temperature-independent if the ratio of the currents of the two branches remains constant over the considered temperature range.

Lemma 1: With the Fixed-Number-Based algorithm, the currents ratios may be different for different input voltages. This does not matter as long as the ratio is temperature-independent for a given input voltage. Furthermore, we do not need to know the value of this ratio.

4　Requirements for I_{CTAT}

The above conduction is based on the assumption that when the temperature migrates from t to t', $I_{bias,1}/I_{bias,2}$ remains unchanged, as is not the case without our CTAT current biasing technique. For example, given the circuit of a ring oscillator, the left part of Fig. 1, and an input ($V_{in} - V_{ref}$), we can always derive a relationship between the current of the two branches:

$$I_{bias,2} = A I_{bias,1} \tag{11}$$

Generally A is the function of both the input ($V_{in} - V_{ref}$) and the temperature. We found that we can properly design the biasing current to be a CTAT to guarantee that A is independent of the temperature, but A may still be a function of the input. Starting from the assumption that A is only the function of

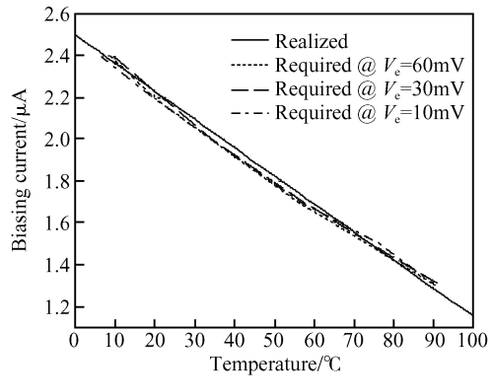

Fig. 3 Required I_{CTAT} under different V_e and the realized I_{CTAT} obtained using the CTAT biasing current source shown in Fig. 4

the input, we inversely conduct the requirements for the biasing current, I_{CTAT}. From Fig. 1, we obtain[7]:

$$(V_{in}-V_{ref})^2=\frac{2}{\mu_p C_{ox}(W/L)_{M1,2}}(I_{CTAT}-2\sqrt{I_{bias,1}I_{bias,2}}) \tag{12}$$

By substituting Eq. (11) into Eq. (12) and using $I_{bias,1}+I_{bias,2}=I_{CTAT}$, I_{CTAT} becomes:

$$I_{CTAT}=\frac{1}{2}\times\frac{(1+A)(V_{in}-V_{ref})^2}{(1-\sqrt{A})^2}\mu_p C_{ox}(W/L)_{M1,2} \tag{13}$$

where μ_p and C_{ox} are the temperature-dependent parameters and their temperature dependencies are given by[8]:

$$\mu_p=\mu_{p0}\left(\frac{T}{T_0}\right)^{-1}$$
$$C_{ox}=C_{ox_0}[l+\alpha_{C_{ox}}(T-T_0)] \tag{14}$$

where l is a positive constant ($l\approx 2$), and $\alpha_{C_{ox}}$ is negative. Thus, Equation (13) can be simplified as:

$$I_{CTAT}\approx I_{CTAT0}[1-B(T-T_0)] \tag{15}$$

where

$$I_{CTAT0}=\frac{1}{2}\times\frac{(1+A)(V_{in}-V_{ref})^2}{(1-\sqrt{A})^2}\mu_{p_0}C_{ox_0}(W/L)_{M1,2}$$
$$B=l/T_0-\alpha_{C_{ox}}>0 \tag{16}$$

The above conductions can be inversely applied. If we set the biasing current as Eq. (15), then A has to be temperature-independent. Notice that here we do not need to know exactly what value A has (refer to Conclusion 1 and Lemma 1). Thus, equation (15) is expected. In reality, the best I_{CTATs} for different input voltages are not exactly the same, however, they almost coincide, as shown in Fig. 3.

Obviously, the slope of I_{CTAT} with respect to temperature should be negative, and can be supplied by V_{BE} of a BJT.

5 Generation of I_{CTAT}

A CTAT biasing current source shown in Fig. 4 realizes the I_{CTAT}. We obtain:

$$I_{M6}=\frac{S_6}{S_1}\times\frac{V_b}{R_3}$$
$$I_{M7}=\frac{S_7}{S_5}\times\frac{2}{\mu_n C_{ox}R_4^2}\times\left(\frac{1}{\sqrt{S_5}}-\frac{1}{\sqrt{S_4}}\right)^2 \tag{17}$$

where

$$S_i=(W/L)_i,\quad i=1,2,3\cdots \tag{18}$$

As we know,

$$V_b=V_{BE}=V_{BE0}[1+\alpha_{V_{BE}}(T-T_0)]$$
$$R_i=R_{i_0}[1+\alpha_R(T-T_0)],\quad i=1\sim 4 \tag{19}$$

where the expression of V_{BE} is obtained through the first-order approximation of a Taylor series expansion. Then, Equation (17) can be rewritten as:

$$I_{Mi}=I_{Mi_0}[1+tc_{I_{Mi}}(T-T_0)],\quad i=6,7 \tag{20}$$

where

$$I_{M6_0}=\frac{S_6}{S_1}\times\frac{V_{BE0}}{R_{3_0}}$$
$$I_{M7_0}=\frac{S_7}{S_5}\times\frac{2}{\mu_{n0}C_{ox0}R_{4_0}^2}\times\left(\frac{1}{\sqrt{S_5}}-\frac{1}{\sqrt{S_4}}\right)^2$$
$$tc_{I_{M6}}=\alpha_{V_{BE}}-\alpha_R$$
$$tc_{I_{M7}}=l/T_0-\alpha_{C_{ox}}-2\alpha_R \tag{21}$$

Thus:

$$I_{M8}=I_{M6}-I_{M7}$$
$$=(I_{M6_0}-I_{M7_0})\left[1+\frac{I_{M6_0}tc_{I_{M6}}-I_{M7_0}tc_{I_{M7}}}{I_{M6_0}-I_{M7_0}}(T-T_0)\right] \tag{22}$$

Since $\alpha_{V_{BE}}<0$, $\alpha_{C_{ox}}<0$ and $\alpha_R>0$ ($\alpha_R=5.79\times 10^{-4}/℃$, using n^+ poly resistor under charted 0.35μm CMOS mixed signal technology), $tc_{I_{M6}}$ is negative and $tc_{I_{M7}}$ positive. Thus, I_{M8} has a negative temperature

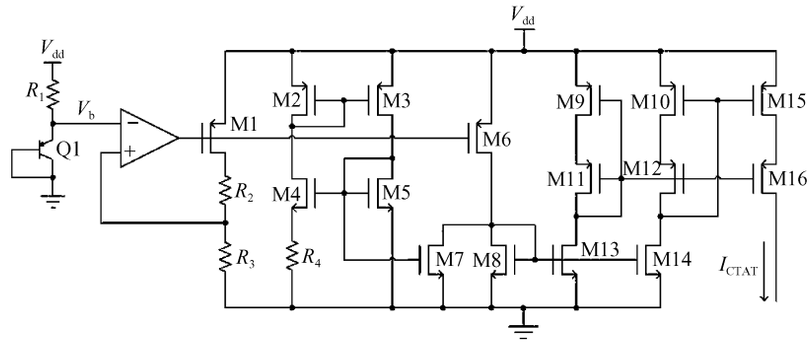

Fig. 4 Schematic of the CTAT biasing current source

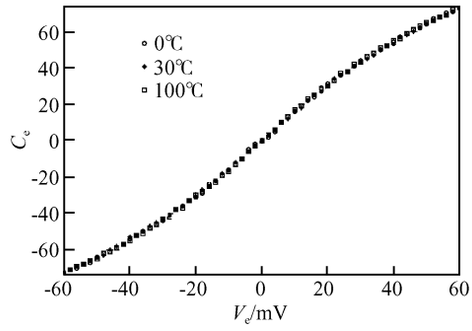

Fig. 5　C_e versus V_e under different temperatures using fixed-number-based algorithm and CTAT biasing current source

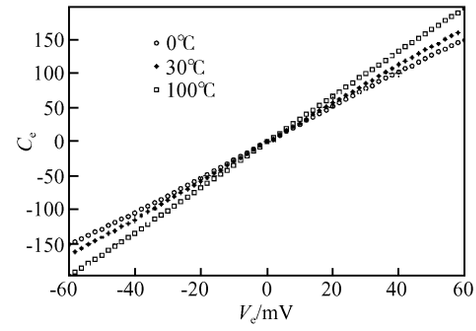

Fig. 6　C_e versus V_e at different temperatures using fixed-time-based algorithm and conventional biasing current source

coefficient ($I_{M7_0} < I_{M6_0}$), which can be tuned by the size of M4, M5, M7, and R4. Finally, the required I_{CTAT} can be achieved by a current mirror:

$$I_{CTAT} = \frac{S_{15}}{S_{10}} \times \frac{S_{14}}{S_8} I_{M8} \tag{23}$$

The realized I_{CTAT} curve, obtained using the structure shown in Fig. 4, is also plotted in Fig. 3. The curve reveals that the CTAT biasing current source provides an excellent fit to the required I_{CTAT} for the entire temperature range.

6　Simulation results

A ring-ADC using the proposed fixed-number-based algorithm together with the CTAT current biasing technique is simulated with a mentor ADMS simulator, under charted 0.35μm CMOS mixed signal technology. The fixed-number is assigned to 128 and the sampling rate is set to 10μs. Meanwhile, a ring-ADC[5] that employs a fixed-time-based algorithm and a conventional biasing current source is also simulated for comparison, with its fixed time set to 10μs. Both ring-ADCs are simulated at three temperatures, 0, 30 and 100℃. Results are plotted in Figs. 5 and 6, with their y-axis representing C_e. The former reveals great stability for the digital output C_e under different temperatures, while the latter shows severe variations, especially at large input voltage error. The proposed technique provides an excellent temperature-independence for ring-ADCs.

At a certain temperature, our temperature compensation technique leads to decreased output linearity, as shown in Fig. 5. However, in the temperature range of 0 to 100℃, our technique achieves much better output linearity than the traditional one, resulting in a much higher converted resolution. Simulation results reveal that our ring-ADC can reach a 2mV quantization bin size while the traditional ring-ADC reaches only 16mV[5]. A typical high-performance digital DC-DC chip, ISL6592[9] requires the quantization bin size of 3.125mV.

Table 1 provides a summary of the comparisons. To further compare our temperature compensation technique with conventional calibration technique, we add information on a delay-line-ADC employing the calibration mechanism that implements a subtract operation[1]. This delay-line-ADC can reach a high speed of f_S = 1MHz. However, limited by the technique, its resolution is only 50mV/LSB, far beyond the requirement of high-performance digital DC-DC chips (3.125mV/LSB[9]). The LSI solution[6] can meet this requirement, but it needs 15,000 transistors and an off-chip quartz. In addition, it was tested under a 5V power supply. By applying our compensating technique, no digital calibrations are needed.

7　Conclusion

This paper presents a novel temperature compensation technique for ring-ADCs. Simulation results prove that, with the proposed fixed-number-based algorithm and a CTAT biasing current source, ring-ADCs can achieve great temperature independence, effectively eliminating the resolution density drift without any additional digital calibration mechanisms.

Table 1　Summary of ring-ADC with/without temperature compensation and delay-line-ADC with calibration

Parameter	Ring-ADC with temperature compensation	Ring-ADC without temperature compensation	Delay-line-ADC using calibration technique in Ref.[1]
Technology	Charted 0.35μm CMOS mixed signal technology		Standard 0.5μm digital CMOS technology
Sampling frequency	f_S = 100kHz		f_S = 1MHz
Input voltage span	120mV		360mV
Resolution	2mV/LSB	16mV/LSB	50mV/LSB
Number of bits	6 bits	3 bits	3 bits

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一种用于降低环振型 ADC 的温度影响的新型技术

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摘要：提出了一种对环振型 ADC 进行温度补偿的新型技术. 该技术采用一种基于固定数的计数算法以及 CTAT 电流偏置技术来补偿温度对输出的影响，不需要任何额外的校准机制. 模拟结果证明，通过采用这种技术，在考虑了 0 到 100℃ 的温度变化的条件下，环振型 ADC 的分辨率可以达到 2mV/LSB（输入电压的范围为 120mV，采样频率为 100kHz）.

关键词：环振型 ADC；CTAT；温度补偿；超大规模集成电路

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