A Programmable 2.4GHz CMOS Multi-Modulus Frequency Divider*

Li Zhiqiang†, Chen Liqiang, Zhang Jian, and Zhang Haiying

(*Institute of Microelectronics, Chinese Academy of Sciences, Beijing* 100029, *China*)

Abstract: A programmable multi-modulus frequency divider is designed and implemented in a 0.35μm CMOS process. The multi-modulus frequency divider is a single chip with two dividers in series, which are divided by 4 or 5 prescaler and by 128～255 multi-modulus frequency divider. In the circuit design, power and speed trade-offs are analyzed for the prescaler, and power optimization techniques are used according to the input frequency of each divider cell for the 128～255 multi-modulus frequency divider. The chip is designed with ESD protected I/O PAD. The dividers chain can work as high as 2.4GHz with a single ended input signal and beyond 2.6GHz with differential input signals. The dual-modulus prescaler consumes 11mA of current while the 128～255 multi-modulus frequency divider consumes 17mA of current with a 3.3V power supply. The core area of the die without PAD is 0.65mm×0.3mm. This programmable multi-modulus frequency divider can be used for 2.4GHz ISM band PLL-based frequency synthesizers. To our knowledge, this is the first reported multi-modulus frequency divider with this structure in China.

Key words: prescaler; frequency divider; programmable; multi-modulus; frequency synthesizer
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1 Introduction

PLL-based frequency synthesizers[1] are widely used in modern wireless communication systems. The main feature of these frequency synthesizers is their capability to frequency hop between different channels, which is realized by changing the division ratio of the frequency divider. The application of the frequency divider requires programmability, high speed, lower power, and high sensitivity operation[2].

In China, several high frequency prescalers with CMOS process were reported recently[3,4,5], but the division ratio is limited to 2^n. Dual-modulus prescalers[6,7] were also reported. A traditional pulse swallow multi-modulus frequency divider[8] was reported, but the division ratio was limited to a small range. In this paper, we present a divided by 4 or 5 dual-modulus prescaler connected with a 128～255 multi-modulus frequency divider, which have been successfully used in a 2.6GHz PLL. To our knowledge, this is the first domestic multi-modulus frequency divider with this structure.

In PLL systems, the frequency divider works in the highest frequency, which makes it the most power hungry circuit in the system. In order to save power, a small division ratio frequency divider, which is called a prescaler[9], is always first connected to the voltage controlled oscillator. In this paper, we present a divided by 4 or 5 prescaler that can work as high as 2.4GHz with a single ended input signal. The dual-modulus prescaler consumes 11mA of current with a 3.3V power supply. The trade-off between power and speed is analyzed.

A conventional pulse swallow multi-modulus frequency divider[10] is realized with a dual-modulus prescaler and two counters. This structure does not have high reusability or high flexibility, so more design time and layout work are needed. In this paper we choose the structure first presented by Vaucher[11,12], and add retiming circuits[13] to lower the jitter accumulation. The multi-modulus frequency divider is formed with seven series divided by 2 or 3 cell, which shares the same circuit implementation. The power consumption can be scaled down as the input frequency is scaled down along the cell chain. This seven stage multi-modulus divider can realize the division ratio of any integer number between 128 and 255, and consumes 17mA of current with a 3.3V power supply voltage.

The divided by 4 or 5 prescaler and the 128～255 multi-modulus frequency divider are connected with a buffer in a single chip. The core area of the die without PAD is 0.65mm × 0.3mm. The chip is designed with ESD protected I/O PAD.

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† Corresponding author. Email: lizhiqiang@ime.ac.cn
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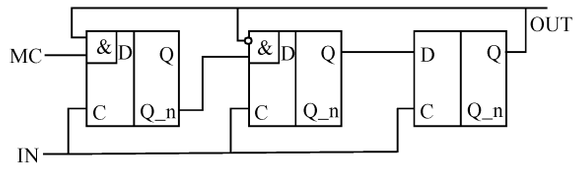

Fig.1　Logic diagram of divided by 4 or 5 prescaler

2　Circuit design

In this section, we will give the circuit architecture and simulation results of the divided by 4 or 5 prescaler and the 128～255 multi-modulus frequency divider. Power and speed trade-offs are analyzed for the prescaler, and power optimization techniques are described for the 128～255 multi-modulus frequency divider. The ESD design for the chip is also given.

2.1　Divided by 4 or 5 prescaler

We used the master-slave D flip-flops and AND gate to form the divided by 4 or 5 prescaler. The logic diagram of the circuit is shown in Fig. 1. MC is the mode control signal. The prescaler is programmed to divide by 4 when the MC is low and divide by 5 when the MC is high.

Current mode logic (CML)[14] was used in the D flip-flop. In the D latch design, two parameters must be considered, i. e., the load resistance and the tail current. The swing voltage of the circuit is decided by the product of the two parameters, so a proper value must be chosen to ensure the reliability of the prescaler. In our design, 1V was chosen as the swing voltage. After the product of the two parameters was chosen, we have to confirm each value of the two parameters. The power of the prescaler is proportional to the tail current, while the speed is inversely proportional to the load resistance, so a trade-off between power and speed is reflected on the tail current and load resistance. For our design goal of a 2.4GHz ISM band application, the 1mA tail current and 1kΩ load resistance were chosen. Post layout simulation shows that with these two parameters' values, the prescaler can work as high as 3GHz.

In order to save area and power, the AND gate was combined with the master latch[15] in the circuit, as shown in Fig. 2. Only three transistors are added compared with the D latch. The simulation result is shown in Fig. 3, where the input is a 300mV 3GHz signal. The waveforms show that the prescaler can work correctly at 3GHz with a differential output.

2.2　Fully programmable 128～255 multi-modulus frequency divider

The block diagram of the fully programmable multi-modulus frequency divider is shown in Fig. 4. The basic cell of the chain is a divided by 2 or 3 circuit, which is connected in series. The division ratio of the 2/3 cell is controlled by P_n and mod_n. If the P_n is logic low, the 2/3 cell will always divide by 2. Only when both P_n and mod_n are logic high, will the 2/3 cell divide by 3. The functional blocks of the divided by 2 or 3 cell are shown in Fig. 5, and the circuit implementation is the same as the divided by 4 or 5 prescaler discussed before.

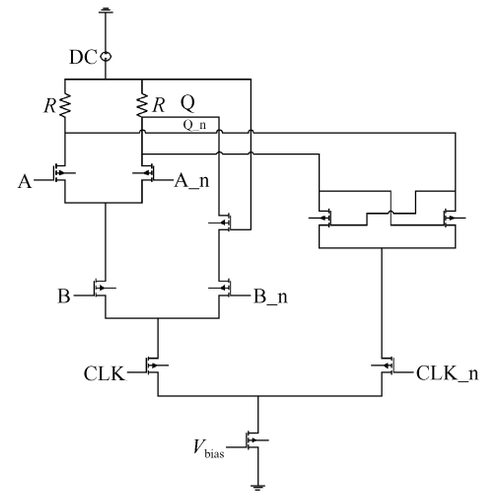

Fig.2　Circuit implementation of D_Latch with AND Gate

The circuit operates as follows. For the last 2/3 cell, the mod_n is set to logic high, and it generates the signal mod_{n-1}. Then the signal propagates up the chain until the first cell. When the mod signal arrives at a cell, it will enable the cell to divide by 3 if the input p is set to logic high. Division by 3 adds an extra period corresponding to its input signal. Hence, a chain of 2/3 cells will provide an output signal with a period:

$$\begin{aligned} T_{\mathrm{out}} &= 2^n T_{\mathrm{in}} + 2^{n-1} T_{\mathrm{in}} p_{n-1} + 2^{n-2} T_{\mathrm{in}} p_{n-2} + \cdots + 2 T_{\mathrm{in}} p_1 + T_{\mathrm{in}} p_0 \\ &= (2^n + 2^{n-1} p_{n-1} + 2^{n-2} p_{n-2} + \cdots + 2 p_1 + p_0) T_{\mathrm{in}} \end{aligned} \tag{1}$$

This equation shows that all division ratios between

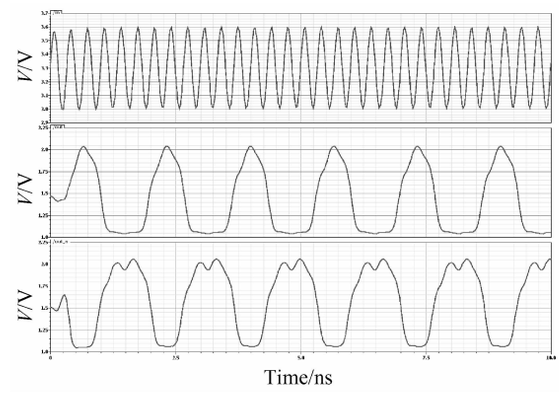

Fig.3　Simulation waveforms with 3GHz input signal

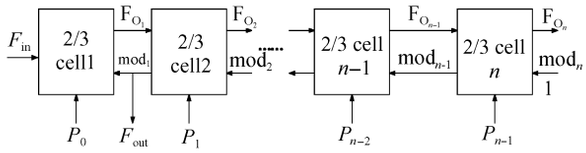

Fig. 4 Block diagram of the fully programmable multi-modulus frequency divider

2^n and $2^{n+1}-1$ can be realized through programmable P_0 to P_{n-1}. In this paper, we chose $n=7$, and realized all division ratios between 128 and 255. The division ratio of our circuit is decided by $2^7 + 2^6P_6 + 2^5P_5 + 2^4P_4 + 2^3P_3 + 2^2P_2 + 2P_1 + P_0$. By controlling P_n, the divider can be fully programmable.

This architecture has many advantages over the traditional pulse swallow architecture. First, power optimization techniques can be used easily by scaling down the tail current of the chain. Second, the reusability is better because its basic cell is the same, so we can easily expand the division ratio. Third, the layout work is much easier because of the repeated cell, which means less time to market. In our design, power optimization techniques are used. The tail current of the 2/3 cell is scaled down according to the input frequency, and the load resistance is scaled up to keep the swing voltage constant.

The asynchronous working of the multi-modulus frequency divider makes the jitter accumulate through the chain, so retiming circuits are very important to eliminate the phase noise. In our design, the simplest way of retiming the divider's output with its input clock was used. We chose the straightforward implementation of a D flip-flop clocked by the divider's input signal structure.

The simulation results are shown in Fig. 6. From top to bottom, the signals are input signal, F_{o_1}, mod_1, F_{o_2}, mod_2. The input frequency is 500MHz with p_0 and p_1 set to logic high. The division ratio is 2 when the mod signal is low and 3 when the mod signal is high, which accords with the theory of the circuit.

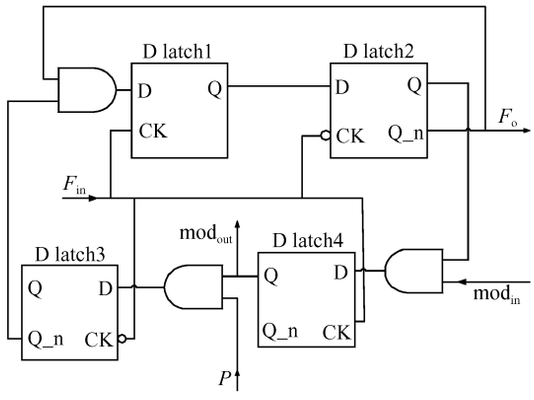

Fig. 5 Functional blocks of divided by 2ro3 cell

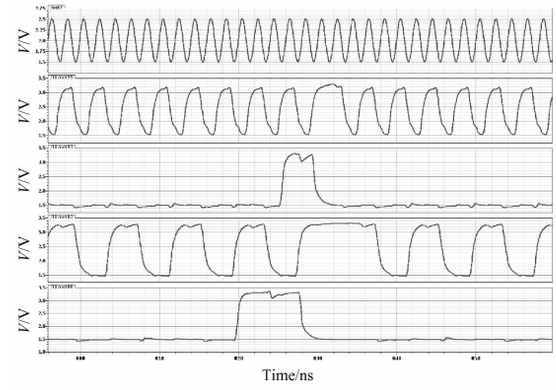

Fig. 6 Simulation waveforms of the multi-modulus frequency divider with 500MHz input signal From top to bottom, the signals are input signal, F_{o_1}, mod_1, F_{o_2}, mod_2.

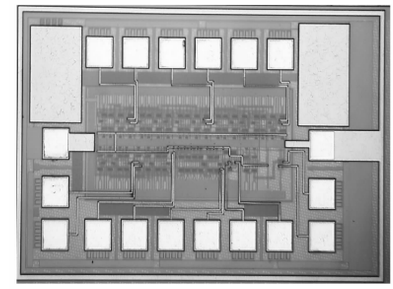

Fig. 7 Die photograph

With 11mA of current, the multi-modulus divider can work as high as 1GHz through post layout simulation.

2.3 ESD design

Electrostatic discharge (ESD) is important for the reliability of the integrated circuits, especially for CMOS technology. In our chip, the I/O ESD protection is realized with inverse biased diode. Simulation shows that the diode can influence the slew rate of the output signal. If the divider is used in PLL, this influence will disappear because no ESD is needed for the divider output.

3 Test results

The prescaler and the multi-modulus divider are connected together with a buffer on a single chip. The

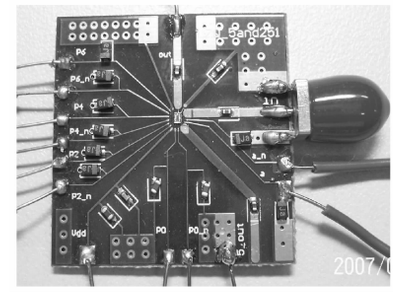

Fig. 8 PCB test board of the chip

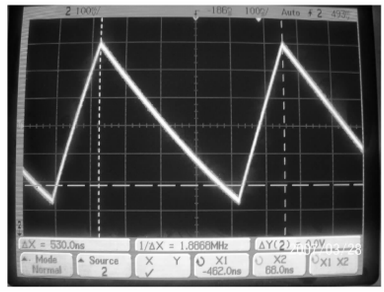

Fig.9　Test waveform of the chip with 2.4GHz single ended input signal and the division ratio of $5\times255=1275$

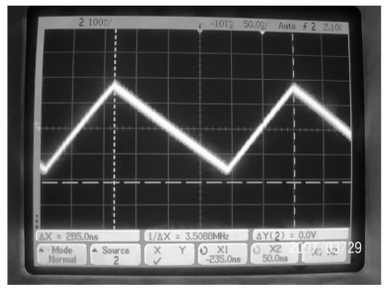

Fig.10　Test waveform of the chip with 2.4GHz single ended input signal and the division ratio of $4\times171=684$

chip photograph is shown in Fig. 7. The chip was tested through PCB, which is shown in Fig. 8. With a single ended 2.4GHz input signal, we can see the output waveform of the final output through Agilent's 54642A oscillograph. In Fig. 9, we make the division ratio $5\times255=1275$ by setting MC = P_6 = P_5 = P_4 = P_3 = P_2 = P_1 = P_0 = 1, and the output frequency is 1.88MHz. In Fig. 10, we make the division ratio $4\times171=684$ by setting MC = P_6 = P_4 = P_2 = 0 and P_5 = P_3 = P_1 = P_0 = 1, and the output frequency is 3.5MHz. Therefore, the prescaler and the multi-modulus both work correctly.

The results are all tested by a single ended input signal. This circuit has been successfully used in a differential 2.6GHz PLL, so the circuit can work beyond 2.6GHz with a differential input signal. The tested output spectrum of the 2.6GHz PLL is shown in Fig. 11, and the details of the PLL will be reported later.

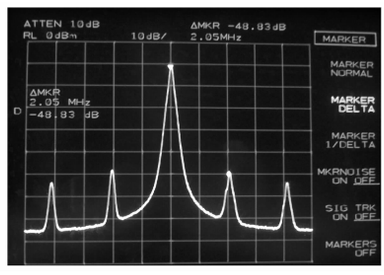

Fig.11　Spectrum of a 2.6GHz PLL using the multi-modulus frequency divider

4　Conclusion

We presented a single chip programmable, ESD-protected 2.4GHz CMOS multi-modulus frequency divider that is composed of a divided by 4 or 5 prescaler and a fully programmable 128～255 multi-modulus frequency divider. This chip can work as high as 2.4GHz with a single ended input signal and beyond 2.6GHz with differential input signals. The dual-modulus prescaler consumes 11mA of current while the 128～255 multi-modulus frequency divider consumes 17mA of current with a 3.3V power supply. The power consumption can be further decreased by using a 0.18μm process. The core area of the die without PAD is 0.65mm×0.3mm. Power and speed tradeoffs are considered in the prescaler design, and power optimization techniques are used in the multi-modulus divider. This frequency divider can be directly used for 2.4GHz ISM band applications.

References

[1] Best R E. Phase-locked loops design, simulation, and application. McGraw-Hill, 1999

[2] Razavi B, Lee K F, Yan R H. Design of high-speed, low-power frequency dividers and phase-locked loops in deep submicron CMOS. IEEE J Solid-State Circuits, 1995, 30(2): 101

[3] Liu Li, Wang Zhigong, Zhu En, et al. 16GHz CMOS 4:1 frequency divider. Research & Progress of SSE, 2006, 26(2): 69 (in Chinese) [刘丽, 王志功, 朱恩, 等. 16GHz CMOS 4:1 分频器. 固体电子学研究与进展, 2006, 26(2): 69]

[4] Lu Jianhua, Wang Zhigong, Tian Lei, et al. An 8.5GHz 1:8 frequency divider in 0.35μm CMOS technology. Chinese Journal of Semiconductors, 2003, 24(4): 366 (in Chinese) [陆建华, 王志功, 田磊, 等. 0.35mm CMOS 8.5GHz 1:8 分频器的设计. 半导体学报, 2003, 24(4): 366]

[5] Zeng Xiaojun, Li Tianwang, Hong Zhiliang. Design of a 1V, 19GHz CMOS frequency divider. Chinese Journal of Semiconductors, 2003, 24(4): 416 (in Chinese) [曾晓军, 李天望, 洪志良. 1V, 19GHz CMOS 分频器设计. 半导体学报, 2003, 24(4): 416]

[6] Xu Yong, Wang Zhigong, Li Zhiqun. Implementation of novel high-speed lower-jitter lower-power-dissipation dual modulus prescaler and the applications in PLL frequency synthesizer. Chinese Journal of Semiconductors, 2005, 26(1): 176 (in Chinese) [徐勇, 王志功, 李智群. 一种新型高速低抖动低功耗双模预分频器及其在 PLL 频率综合器中的应用. 半导体学报, 2005, 26(1): 176]

[7] Chi Baoyong, Shi Bingxue. A novel CMOS dual modulus prescaler based on new optimized structure and dynamic circuit technique. Chinese Journal of Semiconductors, 2002, 23(4): 357 (in Chinese) [池保勇, 石秉学. 一种基于新的优化结构和动态电路技术 CMOS 双模预分频器. 半导体学报, 2002, 23(4): 357]

[8] Xu Yong, Wang Zhigong, Qiu Yinghua, et al. Design of down scalers in mixed-signal GHz frequency synthesizer. Chinese Journal of Semiconductors, 2005, 26(9): 1711 (in Chinese) [徐勇, 王志功, 仇应华, 等. 数模混合 GHz 级频率综合器下变频模块设计. 半导体学报, 2005, 26(9): 1711]

[9] Razavi B. RF microelectronics. Prentice Hall, 1997

[10] Aytur T S, Razavi B. A 2-GHz, 6-mW BICMOS frequency synthesizer. IEEE J Solid-State Circuits, 1995, 30(12): 1457

[11] Vaucher C S, Ferencic I, Locher M. A family of low-power truly

modular programmable dividers in standard 0.35-μm CMOS technology. IEEE J Solid-State Circuits, 2000, 35(7): 1039
[12] Vaucher C S, Apostolidou M, Farrugia A. SiGe building blocks for microwave frequency synthesizers. 12th GaAs Symposium-Amsterdam, 2004: 255
[13] Chien H M, Lin T H, Ibrahim B. A 4GHz fractional-N synthesizer for IEEE 802.11a. Digest of Technical Papers of Symposium on VLSI Circuits, 2004: 4
[14] Alioto M, Palumbo G. Model and design of bipolar and MOS current-mode logic: CML, ECL, SCL digital circuits. Springer, 2005
[15] Rogers J, Plett C, Dai F. Integrated circuit design for high-speed frequency synthesis. Artech House, 2005

一种可编程的 2.4GHz CMOS 多模分频器*

李志强† 陈立强 张 健 张海英

（中国科学院微电子研究所，北京 100029）

摘要：采用 0.35μm CMOS 工艺设计并实现了一种多模分频器. 该多模分频器由一个除 4 或 5 的预分频器和一个除 128～255 多模分频器在同一芯片上连接而成；在电路设计中，分析了预分频器功耗和速度之间的折中关系，根据每级单元电路的输入频率不同对 128～255多模分频器采用了功耗优化技术；对整个芯片的输入输出 PAD 进行了 ESD 保护设计；该分频器在单端信号输入情况下可以工作到 2.4GHz，在差分信号输入下可以工作到 2.6GHz 以上；在 3.3V 电源电压下，双模预分频器的工作电流为 11mA，多模分频器的工作电流为 17mA；不包括 PAD 的芯片核心区域面积为 0.65mm×0.3mm. 该可编程多模分频器可以用于 2.4GHz ISM 频段锁相环式频率综合器.

关键词：预分频器；分频器；可编程；多模；频率综合器
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† 通信作者. Email: lizhiqiang@ime.ac.cn
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