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On-Resistance Degradations Under Different Stress Conditions in High Voltage pLEDMOS Transistors and an Improved Method*

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Abstract: The on-resistance degradations of the p-type lateral extended drain MOS transistor (pLEDMOS) with thick gate oxide under different hot carrier stress conditions are different, which has been experimentally investigated. This difference results from the interface trap generation and the hot electron injection, and trapping into the thick gate oxide and field oxide of the pLEDMOS transistor. An improved method to reduce the on-resistance degradations is also presented, which uses the field oxide as the gate oxide instead of the thick gate oxide. The effects are analyzed with a MEDICI simulator.

Key words: pLEDMOS; on-resistance degradation; hot electron injection and trapping; thick gate oxide
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1 Introduction

In flat display panel (FDP) driver ICs applications, the lateral extended drain MOS transistors (LEDMOS) are the devices of choice for their compatibility with the standard CMOS process. As such, LEDMOS (90～200V) transistors are widely used in plasma display panel (PDP) driver ICs[1～3]. In these driver ICs, the gate oxide of the pLEDMOS must be thick enough to support the high gate voltage, which is the same as the source applied voltage. A severe drawback, however, is that the current flows close to the Si/SiO_2 interface, making hot electron injection and trapping in the thick gate oxide and field oxide possible[4～11]. However, the hot carrier degradation of the pLEDMOS transistors, whose breakdown voltage is above 100V, is less documented.

In this paper, the different on-resistance (R_{on}) degradations of the pLEDMOS with thick gate oxide are examined and correlated with the stress conditions. Under high V_{gs} and low V_{ds} stress, hot electron injection is not found and interface trap generation dominates the R_{on} degradation. However, for low V_{gs} and high V_{ds} stress, hot electron injection and trapping into the thick gate oxide and field oxide dominate the R_{on} degradation at the early stress stage. A detailed discussion on the difference of the R_{on} degradation is given by using a MEDICI simulator, which supports the experimental findings. Finally, an improved method to reduce the on-resistance degradations is also presented, which uses the field oxide as the gate oxide instead of the thick gate oxide and simplifies the fabrication process.

2 Device structure and experiments

Figures 1 (a) and 1 (b) show the schematic cross-section of the high voltage thick gate oxide (TG)-pLEDMOS and field gate oxide (FG)-pLEDMOS structures using bulk silicon (BS) p-substrate, respectively. The p-drift and channel lengths of the pLEDMOS were about 7.5 and 1.5μm, respectively. The thicknesses of the thick gate oxide and the field gate

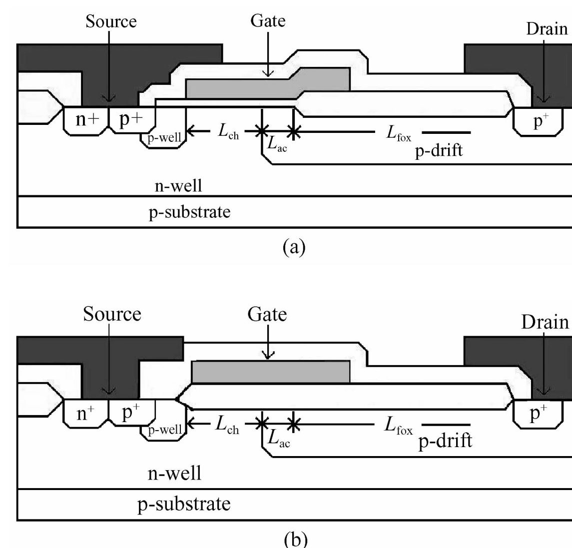

Fig.1　Schematic cross-section of the TG-pLEDMOS (a) and the FG-pLEDMOS (b) with the main geometrical parameters

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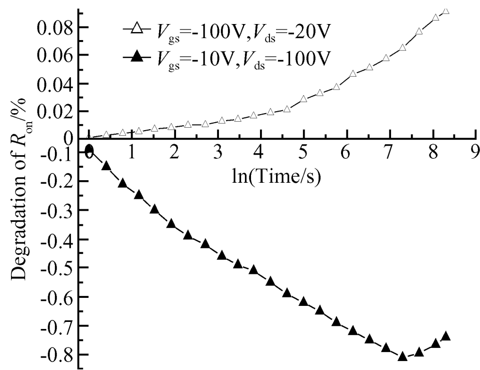

Fig. 2 R_{on} degradations of the high voltage TG-pLEDMOS under the stress conditions of $V_{gs} = -10V$, $V_{ds} = -100V$ and $V_{gs} = -100V$, $V_{ds} = -20V$

oxide are 200 and 400nm, respectively. The threshold voltage and the maximum turn-off breakdown voltage of the TG-pLEDMOS were -6.5 and 110V, respectively. The details of the fabrication process and the characteristics of the TG-pLEDMOS can be found in Ref. [2]. The threshold voltage and the maximal turn-off breakdown voltage of the FG-pLEDMOS were -10.5 and 110V, respectively, which were extracted from the MEDICI simulation results. The most important layout parameters (channel region L_{ch}, accumulation region L_{ac}, and field oxide overlapped drift region L_{fox}) are also indicated in Fig. 1. In practical circuit application, the voltage of V_{gs} is about $-100V$, so the I_{ds} of the FG-pLEDMOS will be large enough for system application.

3 Measurement and discussion

Figure 2 shows the R_{on} degradation of the high voltage TG-pLEDMOS under the stress conditions of $V_{gs} = -10V$, $V_{ds} = -100V$ and $V_{gs} = -100V$, $V_{ds} = -20V$. The R_{on} is measured at $V_{gs} = -15V$ and $V_{ds} = -0.1V$. In practical driver ICs application, these stress conditions always occur. It is interesting to note that R_{on} decreases at the early stress stage when the stress time increases at $V_{gs} = -10V$, $V_{ds} = -100V$. However, the R_{on} is improved when the stress time increases at $V_{gs} = -100V$ and $V_{ds} = -20V$. Under both stress conditions, a small shift in V_{th} is measured and can be neglected, which agrees with the results in Refs. [8,9]. Thus, the R_{on} degradation is independent of the V_{th} shift. Figure 2 shows that the R_{on} degradation of the high voltage TG-pLEDMOS is not serious, which is different from the results of Ref. [8].

Figure 3 (a) shows the electric fields perpendicular to the interface for the TG-pLEDMOS, which are measured along the Si/SiO_2 interface at $V_{gs} = -10V$, $V_{ds} = -100V$ and $V_{gs} = -100V$, $V_{ds} = -20V$, respectively, and the results from the MEDICI simulation.

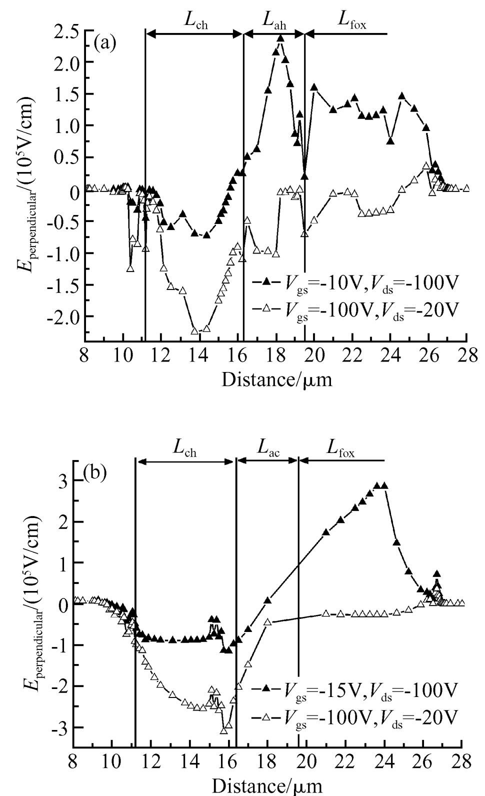

Fig. 3 Electric fields along the Si/SiO_2 interface perpendicular to the interface for the TG-pLEDMOS at $V_{gs} = -10V$, $V_{ds} = -100V$ and $V_{gs} = -100V$, $V_{ds} = -20V$ (a) and FG-pLEDMOS at $V_{gs} = -15V$, $V_{ds} = -100V$ and $V_{gs} = -100V$, $V_{ds} = -20V$ (b)

For $V_{gs} = -10V$ and $V_{ds} = -100V$, the electric field is negative in the channel region and positive in the drift region. Thus, the hot hole can be injected into the thick gate oxide of the channel region and the hot electron can be injected into the thick gate oxide of the accumulation region and field oxide. The electric field is always negative except for the drift region near the drain at $V_{gs} = -100V$ and $V_{ds} = -20V$. Thus, only the hot hole can be injected into the oxide. However, the hot carrier energies are more important to make injection and trapping happen. The carrier temperature along the Si/SiO_2 interface at $V_{gs} = -10V$, $V_{ds} = -100V$ and at $V_{gs} = -100V$, $V_{ds} = -20V$ can be seen in Fig. 4 (a). For $V_{gs} = -100V$ and $V_{ds} = -20V$, there are two peak values of the hot electron energy in the channel region near source and drift boundary, respectively. But the electrical field is negative in the channel region, so the hot electron can not inject into the thick gate oxide.

We also can see the hot hole temperature is less than 1000K to inject into the thick gate oxide and field oxide. Thus, there is no hot carrier injection and no trapping into the oxide of the whole TG-pLEDMOS. Under this stress condition, the interface trap generation in the channel dominates the R_{on} degrada-

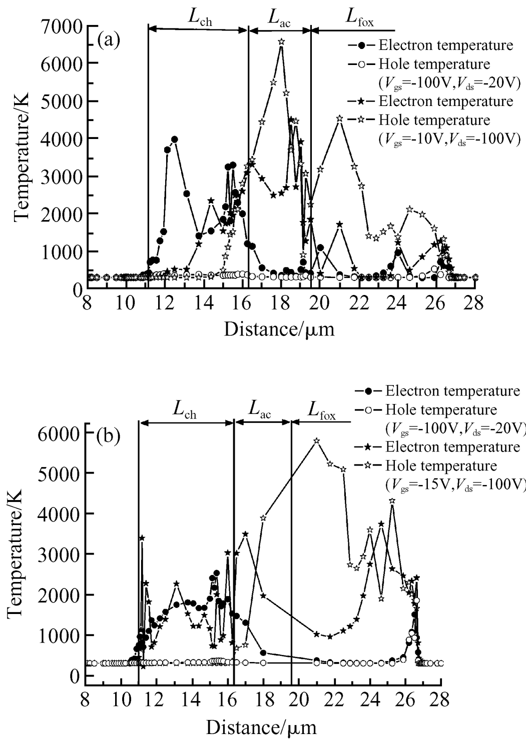

Fig. 4 Carrier temperature along the Si/SiO_2 interface of the TG-pLEDMOS at $V_{gs} = -10V$, $V_{ds} = -100V$ and $V_{gs} = -100V$, $V_{ds} = -20V$ (a) and the FG-pLEDMOS at $V_{gs} = -15V$, $V_{ds} = -100V$ and $V_{gs} = -100V$, $V_{ds} = -20V$ (b)

tion. The interface trap generation can increase the carriers scattering, so as to reduce the hole mobility and increase R_{on} [8]. For $V_{gs} = -10V$ and $V_{ds} = -100V$, the positions of the maximum energy of both the hot electron and hole are near the bird's beak. But the electric field near the bird's beak is positive, so the hot electron will inject and trap into the thick gate oxide of the accumulation region, especially near the bird's beak.

The thick gate oxide is formed by TEOS, so it is less compact and easier for hot electron injecting and trapping. In this way, the hot electron injection probability in the accumulation region L_{ac} becomes large, as shown in Fig. 5 (a). Figure 5 (a) shows the probability per unit length that a hot electron is injected into the oxide along Si/SiO_2 interface at $V_{gs} = -10V$, $V_{ds} = -100V$. The hot electron injection and trapping will also happen in the field oxide, which can also be seen in Fig. 5 (a). Because of the hot electron injection and trapping into the oxide of the drift region, the p-type drift region of the TG-pLEDMOS will have a higher effective doping, resulting in a decrease in R_{on} at the early stress stage.

After 1500s, the hot electron injection and trapping tend to saturation and the influence of the interface trap generation on the R_{on} degradation improves. If the stress time increases futher, the interface trap generation will dominate more, so the R_{on} will slowly increase, which can be seen in Fig. 2. From the above discussion, both at $V_{gs} = -100V$, $V_{ds} = -20V$ and $V_{gs} = -10V$, $V_{ds} = -100V$, there are no hot carriers injected into the thick gate oxide of the channel region. In this way, there is a small V_{th} shift, which also supports the experiment result.

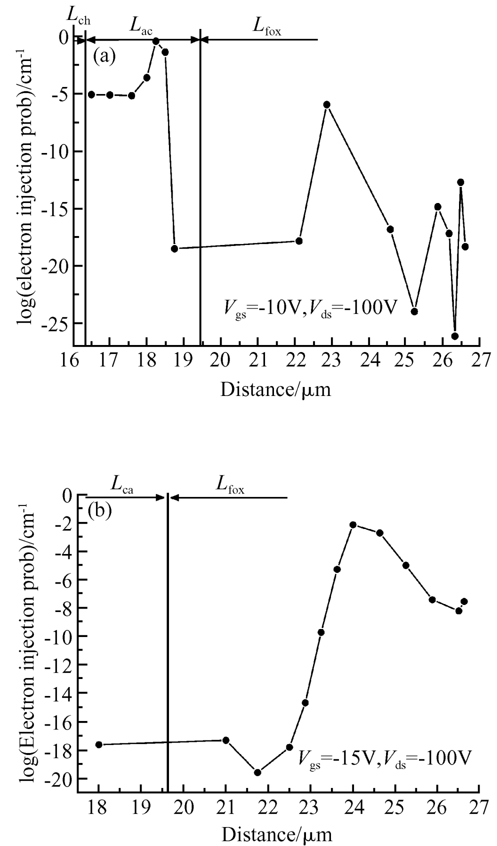

Fig. 5 Probability per unit length that a hot electron is injected into the oxide along Si/SiO_2 interface of the TG-pLEDMOS at $V_{gs} = -10V$, $V_{ds} = -100V$ (a) and the FG-pLEDMOS at $V_{gs} = -15V$, $V_{ds} = -100V$ (b)

4 Improved method and discussion

From the above measurement and discussion results, we can see the hot electron injection and trapping mainly occurs in the accumulation region. Therefore, we can use field oxide as the gate oxide in order to eliminate the bird's beak and reduce the electric field of the accumulation region. The cross-section of the FG-pLEDMOS can be seen in Fig. 1 (b). In this way, the thick gate oxide process can be reduced and the other processes are the same as the TG-pLEDMOS. Because the thickness of the field oxide is 400nm, the threshold voltage of the FG-pLEDMOS is 10.5V. In order to attain a similar stress conduction, $V_{gs} = -15V$, $V_{ds} = -100V$ and $V_{gs} = -100V$, $V_{ds} = -20V$ are used in the MEDICI simulation.

Figure 3 (b) shows the electric fields perpendicular to the interface for the FG-pLEDMOS, which are measured along the Si/SiO_2 interface at $V_{gs} = -15V$, $V_{ds} = -100V$ and $V_{gs} = -100V$, $V_{ds} = -20V$, respectively. The electric fields' distributions are similar to the TG-pLEDMOS, except for the accumulation region. For $V_{gs} = -15V$, $V_{ds} = -100V$, the value of the electric field of the FG-pLEDMOS is much smaller than that of the TG-pLEDMOS.

Figure 4 (b) shows the carrier temperature along the Si/SiO_2 interface at $V_{gs} = -15V$, $V_{ds} = -100V$ and at $V_{gs} = -100V$, $V_{ds} = -20V$. For $V_{gs} = -100V$, $V_{ds} = -20V$, the carrier temperatures of the FG-pLEDMOS is smaller than that of the TG-pLEDMOS, especially at the channel region. For $V_{gs} = -15V$, $V_{ds} = -100V$, the electron and hole temperatures of the FG-pLEDMOS at the accumulation region are smaller than those of the TG-pLEDMOS.

According to the results of the electric field and electron temperature in the accumulation region, the hot electron injection and trapping into the field gate oxide can be greatly reduced, which also can be seen in Fig. 5 (b). The hot electron injection probability per unit length is about 10^{-18}, which is much smaller than that of the TG-pLEDMOS. Figure 5 (b) shows the probability per unit length that a hot electron is injected into the oxide along the Si/SiO_2 interface of the FG-pLEDMOS at $V_{gs} = -15V$, $V_{ds} = -100V$. The hot electron injection probability per unit length increases in the field oxide region, which can also be seen in Fig. 5 (b).

From the above discussion, we can see, for low V_{gs} and high V_{ds}, hot electron injection into the oxide of the accumulation region is reduced, so the equivalent increased doping resulting from the hot electron injection is also reduced. Therefore, the reduction of the R_{on} at the early stress stage will lessen, which is good for the on-resistance degradation. In the FG-pLEDMOS, both at $V_{gs} = -100V$, $V_{ds} = -20V$ and $V_{gs} = -15V$, $V_{ds} = -100V$, there is no hot carrier injection into the field gate oxide of the channel region, so there will also be a small V_{th} shift after the stress.

5 Conclusion

The R_{on} degradations of the high voltage TG-pLEDMOS under different stress conditions have been experimentally investigated. Different mechanisms dominate the R_{on} degradation at different stress conditions. The hot electron may inject and trap into the thick gate oxide and field oxide of the p-drift region for the low V_{gs} and high V_{ds}, which can decrease the R_{on}. For high V_{gs} and low V_{ds}, hot carrier injection and trapping rarely occur, and the interface trap generation makes the R_{on} increase. A novel FG-pLEDMOS is also presented to reduce the on-resistance degradation for low V_{gs} and high V_{ds}, so as to improve the lifetime. No hot carrier injection and trapping into the oxide of the channel region have been found whether in TG- or FG-pLEDMOS, which support the experimental result showing a small shift in the V_{th}.

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高压 pLEDMOS 器件在不同应力条件下导通电阻的衰退及改进方法*

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摘要：实验测试结果揭示高压 pLEDMOS 器件在不同的应力条件下，导通电阻的衰退结果不同，半导体器件专业软件 MEDICI 模拟结果表明 Si/SiO_2 表面的陷阱产生以及热电子的注入和俘获导致了高压 pLEDMOS 器件在不同的应力条件下产生不同的导通电阻衰退.文中同时提出了一种改进方法：用场氧代替厚栅氧作为高压 pLEDMOS 器件的栅氧，MEDICI 模拟结果显示该方法可以明显降低/减缓高压 pLEDMOS 导通电阻的衰退.

关键词：p 型横向延伸漏金属氧化物半导体管；导通电阻衰退；热电子注入和俘获；厚栅氧

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