A Novel Hybrid DPWM for Digital DC-DC Converters

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Abstract: We present a new hybrid digital pulse-width modulator (DPWM) for digital DC-DC converters that employs a ring-oscillator/counter structure. Based on a temperature/process compensation technique and a novel digital controller, the proposed DPWM can not only offer temperature/process-independent pulse widths, but also operate at a much higher clock frequency than the existing delay-line/counter DPWM structure. Post-simulation results show that with our DPWM, the system clock frequency reaches 156.9MHz while the worst variation, in a temperature range of 0 to 100℃ under all process corners, is only ±9.4%.

Key words: DPWM; ring oscillator; DC-DC converter
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1 Introduction

Digital pulse-width modulators (DPWM) serve as the digital-to-analog (D/A) converter in a digital DC-DC converter. The resolution of the DPWM determines the achievable output voltage. If the DPWM resolution is not high enough, an undesirable limit-cycle oscillation may occur[1]. For digital DC-DC converters, the design of high resolution, high frequency DPWMs is of great importance.

The basic principle of a DPWM is to count a clock (generally the system clock) and compare the accumulated sum with the required duty ratio[1~3]. This solution is the easiest to think of. However, it requires a system clock of high frequency (to achieve an n-bit resolution at the switching frequency f_s, the required clock frequency will be $2^n f_s$.) and can easily result in difficult timing constraints and high power consumption for the circuits. A DPWM of the tapped delay-line structure[4~5] involves a long line of delay-units, with the delay of every unit equal to the LSB of the pulse width. By selecting the output of a delay-unit according to the required duty ratio, a proper pulse width is generated. This solution reduces the clock frequency to the switching frequency f_s at the cost of a large digital multiplexer and a large delay-line (a 2^n ∶ 1 multiplexer and at least 2^n delay units for an n-bit resolution). In recent years, DPWMs of the hybrid delay-line/counter structure[6~7] have been reported that make trade-offs between the system clock frequency and the scale of the multiplexers (as well as the delay-line). In the hybrid structures, the system clock frequency is still higher than the switching frequency but much lower than $2^n f_s$. The pulse width corresponding to the least n_d bits of the duty ratio is achieved with the DPWM, whereas that corresponding to the remaining $(n - n_d)$ bits is constructed by counting the system clock.

There are some severe problems for delay-line-based DPWMs. First, the pulse width's LSB generated by the delay-unit is susceptible to the temperature/process variations, resulting in uncertainty about the DC-DC converter's performance. Meanwhile, the smallest pulse width used in the digital circuits is $T_{sys}/2^{n_d}$ (for generating the non-overlapped sequent pulses[6]), making this type of DPWM not suitable for high-frequency applications, such as an f_{sys} of 156.9MHz in this paper.

In this paper, we present a new hybrid DPWM implementation called the ring-oscillator/counter structure. In our DPWM, a ring-oscillator is used to generate the system clock, and the delay of the inner differential stages acts as the LSB of the pulse width. A sensing circuit is designed to get information about the temperature/process variations and accordingly a controlling voltage is generated and imposed on the ring-oscillator. When the frequency of the ring-oscillator begins to deviate from the designed value due to the temperature/process variation, the controlling voltage will act in the opposite direction and pull the frequency back. Thus, the pulse width generated by our DPWM is also temperature/process-independent, ensuring the stability of the DC-DC's performance. Meanwhile, the smallest pulse width used in our digital circuits is only $T_{sys}/2$, thus our DPWM can work at

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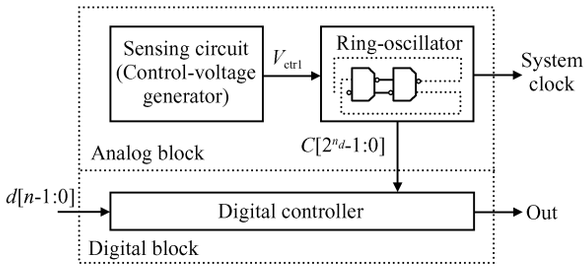

Fig. 1 Block diagram of the proposed DPWM structure

a higher system clock frequency.

2 System architecture

Figure 1 shows the block diagram of the proposed DPWM. It consists of a sensing circuit, a ring-oscillator and a digital synthesizer. The system frequency is f_{sys} and the switching frequency is $f_s = f_{sys}/2^{n_c}$ ($n_c = n - n_d$). In addition to the system clock, the ring-oscillator offers 2^{n_d} outputs for generating the pulse widths between $(1/2^{n_d})T_{sys}$ and $(2^{n_d} - 1/2^{n_d})T_{sys}$. $d[n-1:0]$ is the digitalized required duty ratio, in which $d[n_d-1:0]$ controls a 2^{n_d}:1 multiplexer to select an output from the ring-oscillator and $d[n-1:n_d]$ set the stopping condition for the system-clock counter. The sensing circuit senses the variations of the temperature and the process, and generates a controlling voltage, V_{ctrl}. Compensated with V_{ctrl}, f_{sys} and the LSB of the pulse width are nearly temperature/process independent.

3 Multi-phase ring-oscillator with sensing circuit (analog block)

3.1 Multi-phase ring oscillator

Figure 2 shows a 16-phase ring-oscillator, which is based on an 8-stage differential ring-oscillator. Buffers are added to drive the digital circuits. The structure of the individual delay unit is shown in Fig. 3[8]. The frequency of the oscillator is given by[9]:

$$f = \frac{1}{2Nt_d} \tag{1}$$

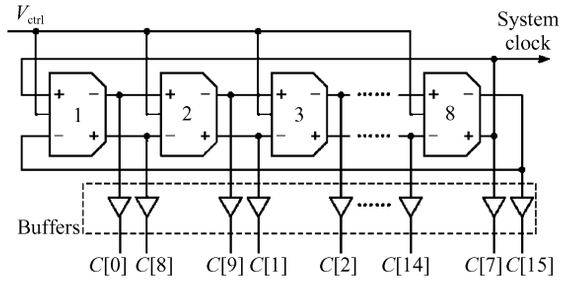

Fig. 2 Schematic of an 8-stage ring-oscillator

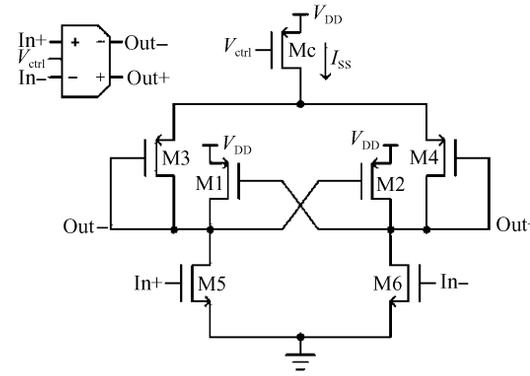

Fig. 3 Schematic of the delay cell in Fig. 2

where N is the number of delay stages, and t_d is the delay time of a delay cell. We have[10]:

$$t_d = \frac{C_L V_{SW}}{I_{SS}} \tag{2}$$

where C_L is the output capacitor, I_{SS} is the biasing current of the delay cell, and V_{SW} is the output swing. Here, V_{SW} approximately equals the supply voltage V_{DD}. I_{SS} can be calculated by:

$$I_{SS} = \frac{1}{2}\mu_p C_{OX}\left(\frac{W}{L}\right)_c (V_{DD} - V_{CTRL} - V_{TP})^2 \tag{3}$$

Substituting Eqs. (2) and (3) into Eq. (1), we obtain:

$$f = \frac{\mu_p C_{OX}\left(\frac{W}{L}\right)_c (V_{DD} - V_{CTRL} - V_{TP})^2}{4NC_L V_{DD}} \tag{4}$$

Because the parameters such as the threshold voltage and the mobility of charge carriers are temperature/process dependent, the frequency of the ring-oscillator is unstable for a fixed V_{CTRL}. We change the V_{CTRL} according to the temperature/process to keep the frequency constant.

Expression (4) can be rewritten as:

$$V_{CTRL} = V_{DD} - V_{TP} - \sqrt{\frac{4NV_{DD}C_L f}{\mu_p C_{OX}\left(\frac{W}{L}\right)_c}} \tag{5}$$

where μ_p, C_{OX}, and V_{TP} are the temperature-dependent parameters[11]:

$$\mu_p = \mu_{p0}\left(\frac{T}{T_0}\right)^{-m} \tag{6}$$

$$V_{TP} = V_{TP0}[1 + \alpha_{V_T}(T - T_0)] \tag{7}$$

$$C_i = C_{i0}[1 + \alpha_C(T - T_0)] \tag{8}$$

By substituting Eqs. (6)~(8) into Eq. (5), and using the first-order approximation of the Taylor series expansion: $[1 + \alpha_{C_{OX}}(T - T_0)]^{-1} \approx 1 - \alpha_{C_{OX}}(T - T_0)$, the temperature characteristic of V_{CTRL} can be obtained:

$$V_{CTRL} \approx V_{DD} - V_{TP0}[1 + \alpha_{V_T}(T - T_0)] - \sqrt{\frac{4NV_{DD}C_{L0}f[1 + (\alpha_{C_L} - \alpha_{C_{OX}})(T - T_0)]}{\mu_{p0}C_{OX0}\left(\frac{W}{L}\right)_c T_0^m}}\, T^{\frac{m}{2}} \tag{9}$$

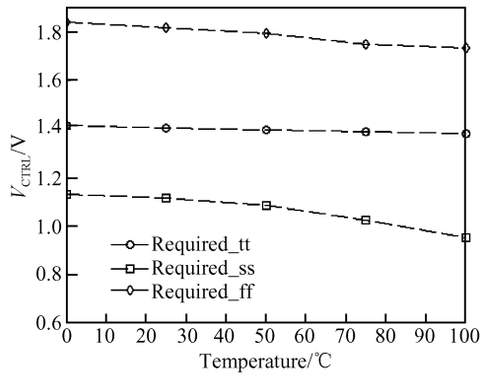

Fig. 4　Required V_{CTRL} under three process corners

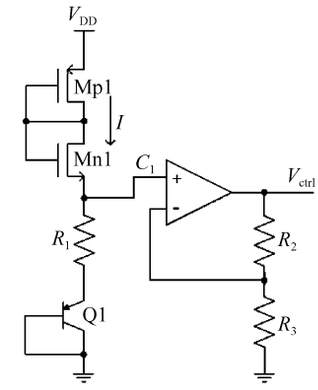

Fig. 5　Basic process-sensing control-voltage generator

Because $m \approx 2$ and $\alpha_{C_L} \approx \alpha_{C_{OX}}$, the above expression can be simplified as:

$$V_{CTRL} = A - BT \tag{10}$$

where

$$A = V_{DD} - V_{TP0} + \alpha_{V_T} T_0 \tag{11}$$

$$B = V_{TP0}\alpha_{V_T} + \sqrt{\frac{4NV_{DD}C_{L0}f}{\mu_{p0}C_{OX0}\left(\frac{W}{L}\right)_c T_0^m}} \tag{12}$$

In Eq. (12), the second term is positive and at least 10^3 times larger than the first one for f = 157MHz, N = 8, and the typical 0.35μm CMOS process (i.e., Charted). Therefore, to keep f a constant, V_{CTRL} should have a negative temperature coefficient, which can be obtained by V_{BE} of a BJT transistor. Meanwhile, since the value of V_{TP} in Eq. (9) depends on a specific process, different process conditions may lead to different V_{TP}, and ultimately different required V_{CTRL} curves. Thus, V_{CTRL} is also designed to compensate process variations.

Figure 4 gives an example of the required compensating curves. Here the V_{CTRL} curves under different process corners are shown. It is required that the compensation should be done well at all three process corners.

3.2　Sensing circuit (control-voltage generator)

A temperature/process-sensing circuit, called a basic control-voltage generator, shown in Fig. 5, can offer the temperature/process compensation curves shown in Fig. 4. V_{CTRL} is given by:

$$V_{CTRL} = \frac{R_2 + R_3}{R_3}(V_{DD} - V_{TP1} - V_{TN1} + D) - \frac{R_2 + R_3}{R_3}\sqrt{2D(V_{DD} - V_{TP1} - V_{TN1} - V_{BE}) + D^2} \tag{13}$$

where

$$D = \frac{1}{R_1}\left(\frac{1}{\sqrt{\mu_p C_{OX}\left(\frac{W}{L}\right)_{P1}}} + \frac{1}{\sqrt{\mu_n C_{OX}\left(\frac{W}{L}\right)_{N1}}}\right)^2 \tag{14}$$

The negative temperature coefficient of V_{CTRL} is achieved through V_{BE} and can be tuned by R_1, $(W/L)_{P1}$, and $(W/L)_{N1}$. Meanwhile, due to V_{TP1} and V_{TN1}, V_{CTRL} also accounts for information from the process variation.

The larger the variation of V_{CTRL} under different process corners is, the better the compensation that can be obtained[12]. Based on this relationship, we propose an enhanced control-voltage generator, shown in Fig. 6. It is a cascade of the basic control-voltage generators. The output of the former stage is the supply voltage of the latter. The expression of V_{CTRL} is similar to Eq. (13) except that V_{DD} in Eq. (13) is replaced with V_{su}. Then, we have:

$$\left.\frac{\partial V_{CTRL}}{\partial(V_{TP} + V_{TN})}\right|_{basic} = \frac{R_2 + R_3}{R_3}\left(\sqrt{\frac{D}{2(V_{DD} - V_{TP1} - V_{TN1} - V_{BE}) + D}} - 1\right) < 0 \tag{15}$$

$$\left.\frac{\partial V_{CTRL}}{\partial(V_{TP} + V_{TN})}\right|_{enhanced} \approx \left.\frac{\partial V_{CTRL}}{\partial(V_{TP} + V_{TN})}\right|_{basic} + \frac{\partial V_{CTRL}}{\partial V_{su}} \times \frac{\partial V_{su}}{\partial V(V_{TP} + V_{TN})} \tag{16}$$

where

$$\frac{\partial V_{CTRL}}{\partial V_{su}} \times \frac{\partial V_{su}}{\partial V(V_{TP} + V_{TN})} = \frac{R_2 + R_3}{R_3} \times \frac{R_5 + R_6}{R_6}\left(1 - \sqrt{\frac{D}{2(V_{su} - V_{TP1} - V_{TN1} - V_{BE}) + D}}\right) \times \left(\sqrt{\frac{E}{2(V_{DD} - V_{TP2} - V_{TN2} - V_{BE}) + E}} - 1\right) < 0$$

$$E = \frac{1}{R_4}\left(\frac{1}{\sqrt{\mu_p C_{OX}\left(\frac{W}{L}\right)_{P2}}} + \frac{1}{\sqrt{\mu_n C_{OX}\left(\frac{W}{L}\right)_{N2}}}\right)^2 \tag{17}$$

We can derive:

$$\left|\left.\frac{\partial V_{CTRL}}{\partial V(V_{TP} + V_{TN})}\right|_{basic}\right| < \left|\left.\frac{\partial V_{CTRL}}{\partial V(V_{TP} + V_{TN})}\right|_{enhanced}\right| \tag{18}$$

Thus, with the proposed enhanced control-voltage generator, V_{CTRL} varies more greatly with respect to the process corners. Figure 7 shows the required V_{CTRL} as well as the V_{CTRL} realized with the

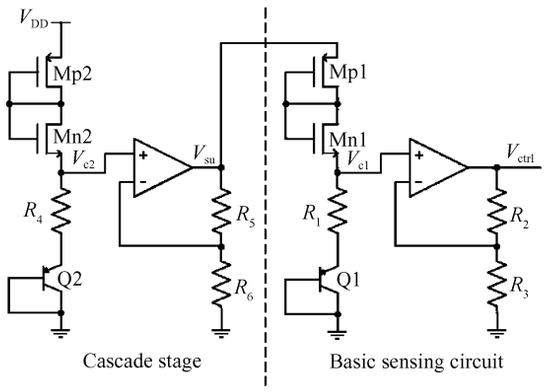

Fig. 6 Enhanced control-voltage generator

basic generator and the enhanced generator, respectively. The proposed enhanced control-voltage generator provides a better fit V_{CTRL} for all process corners than the basic one.

Equation (4) demonstrates that f changes with V_{DD}, making the system susceptible to the power supply. However, a voltage regulator can resolve this by providing the system a temperature and supply independent reference voltage.

4 Digital controller

Figure 8 shows the simplified diagram of the digital controller in Fig. 1 ($n = 11$, $n_d = 4$, $2^{n_d} = 16$) as well as the key waveforms. The upper half is a general counter to form the pulse width corresponding to

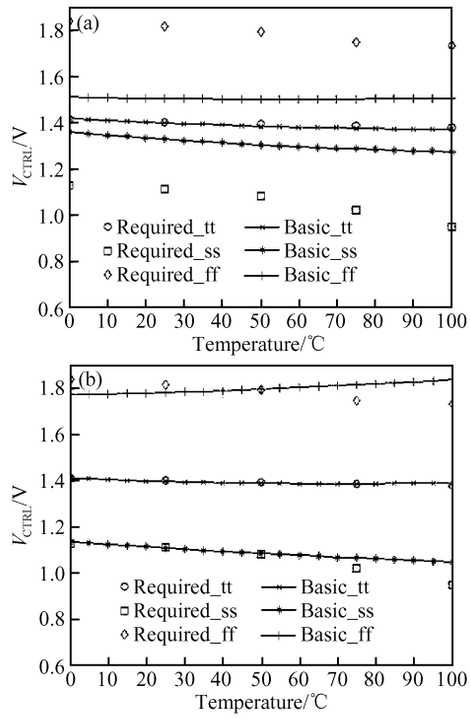

Fig. 7 Required V_{CTRL} under three process corners and the realized curves obtained using the basic (a) and enhanced (b) control-voltage generator

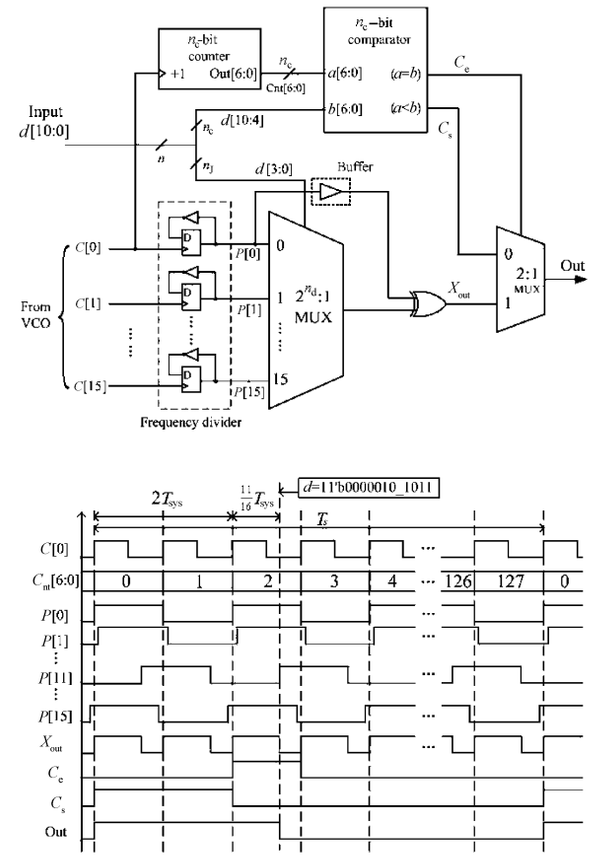

Fig. 8 Digital controller in an 11bit DPWM using hybrid ring-oscillator/counter structure with its operating waveforms

$d[n-1:n_d]$, while the lower half generates the pulse width corresponding to $d[n_d-1:0]$.

The frequencies of the 16 outputs of the ring oscillator, $C[0]\sim C[15]$, are half-divided into $P[0]\sim P[15]$. Then, one of $P[0]\sim P[15]$ is selected by a 2^{n_d}:1 multiplexer to perform an XOR operation with $P[0]$, so that a pulse width between 0 and $(15/16)\times T_{sys}$, with the resolution of $(1/16)T_{sys}$, is generated on the node X_{out}. Meanwhile, pulse $C[0]$ serves as the clock for an n_c-bit counter. When the output of the counter matches $d[n-1:n_d]$, the most significant n_c bits of the n-bit digital input d ($n = n_c + n_d$), the output of the 2:1 multiplexer changes from C_s to X_{out}. Therefore, the n_c-bit counter realizes the high n_c-bit of the n-bit resolution, and X_{out} gives the low n_d-bit of the n-bit resolution.

The delay of the 2^{n_d}:1 multiplexer may influence the low n_d-bit of the resolution due to the fact that $P[0]$ and the signal selected from $P[0]\sim P[15]$ may have different delay times at the XOR gate. To minimize the skew, a buffer can be added on the path from $P[0]$ to the XOR gate, as marked in Fig. 8. In addition, the jitters on the 16-phase clocks may affect the precision of frequency and phase, and ultimately deteriorate the resolution of X_{out}. Thus, a fast-transition on the delay-cells should be ensured to reduce jit-

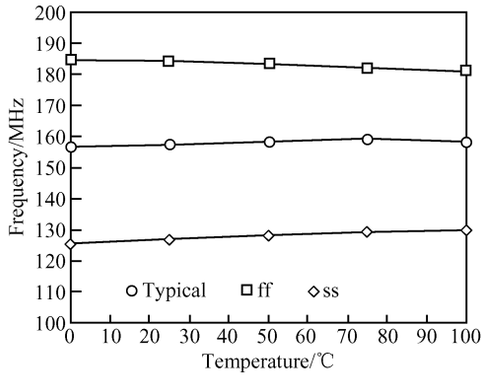

Fig. 9　Simulation results obtained using the basic control-voltage generator

ters[13], as fulfilled in our scheme.

The waveforms in Fig. 8 give an example with d = 43 (11'b00000101011 = 0000010_0000 + 0000000_1011), the pulse width on the node out is constructed with $2T_{sys}$ (realized by the counter) and a $(11/16) \times T_{sys}$.

The smallest required pulse width in the delay-line-based DPWM[6] is $(1/2^{n_d})\ T_{sys}$, while ours is $(1/2)T_{sys}$ (appearing at $C[0]$ to $C[15]$). Thus, the set-up-time constraint of the D-flip-flops is greatly reduced in our DPWM and the working frequency greatly enhanced. Simulations show that the delay-line-based DPWM[6] fails to generate the necessary small pulse width at the system frequency of 156.9MHz, which is used in this paper. A typical high-performance digital DC-DC chip, ISL6592[14] requires the system clock frequency of 156.25MHz ± 10%.

5　Simulation results

5.1　Ring oscillator

Simulations were done under different temperature and process corners with charted 0.35μm CMOS mixed signal technology. Figure 9 shows the results

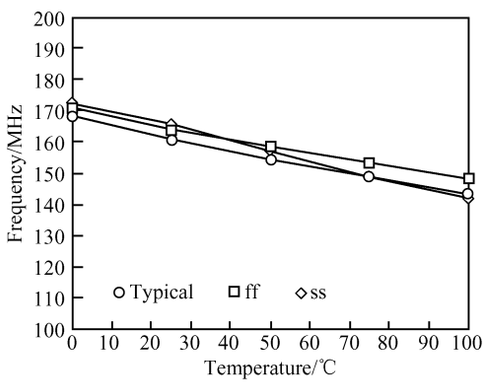

Fig. 10　Post-simulation results of our DPWM, using the enhanced control-voltage generator

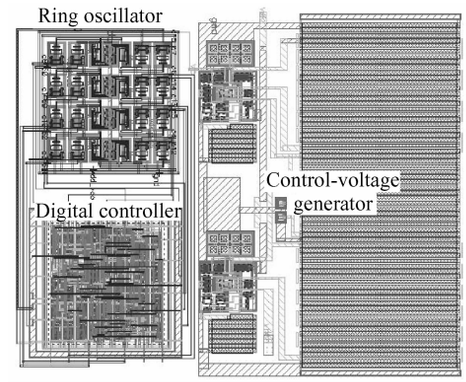

Fig. 11　Layout of the designed 11bit DPWM

when V_{CTR} is generated with the basic control-voltage generator and Figure 10 is the post-simulation results of our DPWM, which employs the enhanced control-voltage generator. The largest variation of f_{sys} in Fig. 9 is ± 19% at the clock frequency of 156.9MHz while it is ± 9.4% in Fig. 10 (compared to ISL6592's 156.25MHz ± 10%), in a temperature range of 0 to 100℃.

5.2　11bit DPWM

An 11bit DPWM is designed and post-simulated. Figure 11 shows the layout, which consists of a full-custom design of the ring-oscillator (analog part) and a semi-custom design of the digital controller (digital part). The area of the whole DPWM is approximately 0.24mm^2.

Figure 12 shows the pulse widths corresponding to $d[n-1:0]$ constructed with a fixed $d[n-1:n_d]$ and a changed $d[n_d-1:0]$. Here, n = 11, n_d = 4, $d[n-1:n_d]$ = 7'b0000010 ($2T_{sys}$), and $d[n_d-1:0]$ are assigned to 4'b0000 ～ 4'b1111, corresponding to $(0/16)T_{sys}$～ $(15/16)T_{sys}$ respectively. The LSB of the pulse width reveals that the resolution of our DPWM achieves 1/(16 × 156.9MHz) = 1/(2.51GHz), at a high system frequency of $f_{sys} \approx$156.9MHz. The rising time and the falling time of the clock are only 88 and 106ps, respectiely.

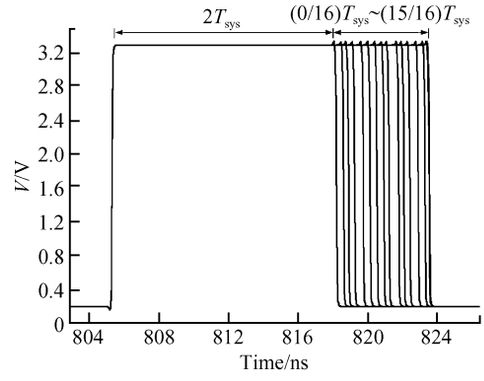

Fig. 12　Pulse widths corresponding a fixed $d[n-1:n_d] = 2T_{sys}$ and a changed $d[n_d-1:0] = (0/16)T_{sys}$～ $(15/16)T_{sys}$

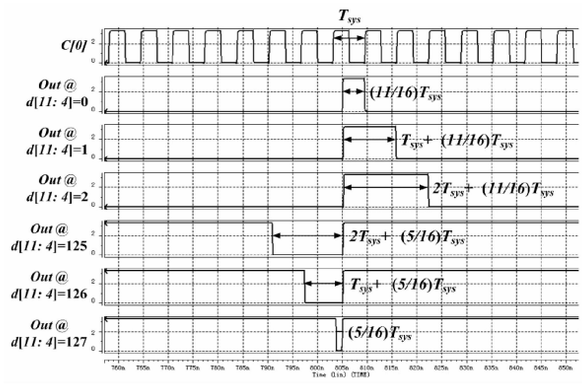

Fig. 13 Pulse widths corresponding a changed $d[n-1:n_d]=AT_{sys}$, $A=0,1,2,125,126,127$, and a fixed $d[n_d-1:0]=(11/16)T_{sys}$.

Figure 13 verifies that our pulse width is seamlessly constructed with $d[n-1:n_d]$ (realized with the counter) and $d[n_d-1:0]$ (realized with X_{out}). Here, $d[n_d-1:0]=4'b1011$ ($(11/16)T_{sys}$) and $d[n-1:n_d]$ are assigned to 0,1,2,125,126, and 127, respectively.

6 Conclusion

This paper presents a new hybrid DPWM structure: the ring-oscillator/counter structure. Based on an enhanced control-voltage generator, the ring-oscillator can provide a stable clock against the temperature/process variations. This ensures the stability of the DPWM output. Also, due to the employment of a novel digital controller, the proposed structure can operate at a higher clock frequency (156.9MHz in this paper) than the delay-line/counter structure, an existing hybrid DPWM structure.

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一种适用于 DC-DC 变换器的新型混合式数字脉宽调制器

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摘要：提出了一种新型的适用于 DC-DC 变换器的混合式数字脉宽调制器. 该脉宽调制器基于混合环路振荡器/计数器的结构. 与已有的延迟线/计数器结构相比，由于该数字脉宽调制器采用了温度/工艺补偿技术和一种新型的数字控制器，使其不仅可为 DC-DC 变换器提供一个不随温度/工艺角变化的时钟，而且可以工作在更高的时钟频率，适用于高频应用场合. 后仿结果表明该混合式数字脉宽调制器工作的时钟频率可达到 156.9MHz，并且在 0～100℃的温度范围内及所有工艺角下的最大偏移只有 ±9.4%.

关键词：数字脉宽调制器；环路振荡器；DC-DC 变换器
EEACC：1250
中图分类号：TN432 **文献标识码**：A **文章编号**：0253-4177(2008)02-0275-06

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