A Low Voltage, Low Power RF/Analog Front-End Circuit for Passive UHF RFID Tags*

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Abstract: This paper presents a low voltage, low power RF/analog front-end circuit for passive ultra high frequency (UHF) radio frequency identification (RFID) tags. Temperature compensation is achieved by a reference generator using sub-threshold techniques. The chip maintains a steady system clock in a temperature range from −40 to 100℃. Some novel building blocks are developed to save system power consumption, including a zero static current power-on reset circuit and a voltage regulator. The RF/analog front-end circuit is implemented with digital base-band and EEPROM to construct a whole tag chip in 0.18μm CMOS EEPROM technology without Schottcky diodes. Measured results show that the chip has a minimum supply voltage requirement of 0.75V. At this voltage, the total current consumption of the RF/analog front-end circuit is 4.6μA.

Key words: RFID; tag; low voltage; low power; temperature compensation
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1 Introduction

Cheap and adaptable, passive radio frequency identification (RFID) tags operating in the ultra high frequency (UHF) band show a wide potential for application. The trend for passive UHF tags is to increase the operating distance, reading rate, and reading speed. Therefore, stringent requirements are proposed, including low power, high power conversion efficiency, and stability under different working conditions. In recent years, various optimizations have been introduced to improve the tag's performances[1~4]. However, most of them are implemented in CMOS technology with Schottcky diodes, which is relatively expensive. Moreover, few works mention the realization of temperature compensation, without which the tag cannot work correctly in conditions of extreme weather.

In this paper, we design a whole tag chip (EPC-global Class 1 Gen 2 standard[8] compliant) in 0.18μm CMOS EEPROM technology. The RF/analog front-end circuit is compatible with the standard CMOS technology, and has a low voltage low power characteristic and a temperature insensitive performance.

2 System architecture

Figure 1 depicts the architecture of our tag, where the circuit within the dotted line represents the RF/analog front-end. The circuit derives its power supply by rectifying the interrogating RF energy. A low voltage reference generator provides voltage and current references for the whole system. The system

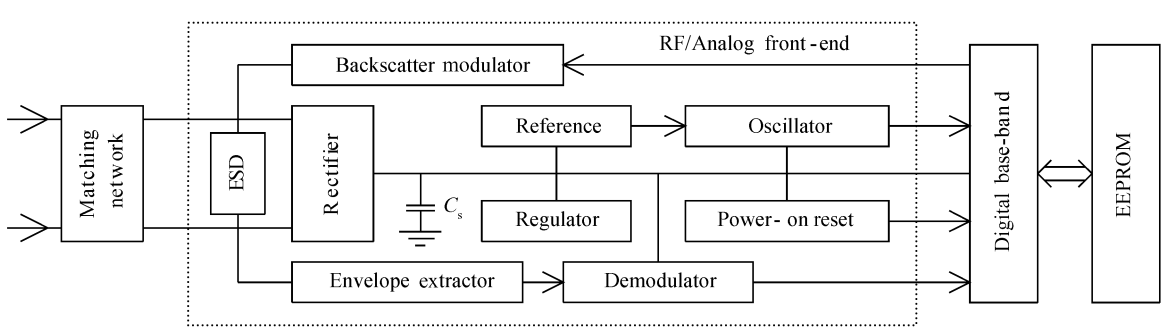

Fig. 1 System architecture

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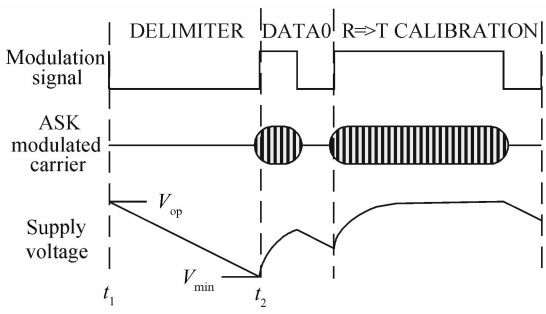

Fig. 2 Supply voltage versus transmission signal

clock is generated by a current controlled ring oscillator[9]. The forward link data are demodulated from the extracted envelope of the carrier[2]. They are sent to the digital base-band for signal process with the clock and power-on reset signals. Backward modulation is achieved using the backscatter mechanism. According to the input FM0 coded signal, the backscatter modulator changes the input impedance of the tag to cause simultaneous phase-shift keying (PSK) and amplitude-shift keying (ASK) modulation of the backscattered electromagnetic wave. An energy storage capacitor C_S is employed to supply the chip in case of an interrogating energy gap.

In RFID tag design, one of the most important global considerations is the low power performance. Current consumption of a Gen 2 tag[8] has been reduced to less than 10μA. However, the supply voltage of a passive tag still remains above 1V[1,4,5,7]. The situation opens the possibility of cutting power consumption by lowering the system supply voltage.

From a systematic view, the merit of low voltage is illustrated with the following example. Figure 2 shows a typical waveform named "frame-sync"[8]. The supply voltage changes with the receiving ASK modulated carrier, which is determined by the modulation signal. Before time t_1, V_{DD} is at a level of V_{OP}, which represents the operating voltage. During the period of DELIMITER, V_{DD} drops to a lower level labeled V_{min}, which should be higher than the tag's minimum supply voltage requirement. The I-V relationship of this period is:

$$C_S(V_{OP} - V_{min}) = \int_{t_1}^{t_2} I(t)\mathrm{d}t \tag{1}$$

where $I(t)$ is the transient current of the whole system. Moreover, V_{OP} is a function of the operating distance:

$$V_{OP} I_{OP} \propto 1/d^2 \tag{2}$$

where I_{OP} is the operating current and d is the operating distance. Equations (1) and (2) indicate that a low V_{min} not only increases the operating distance, but also decreases the chip size by reducing the storage capacitor.

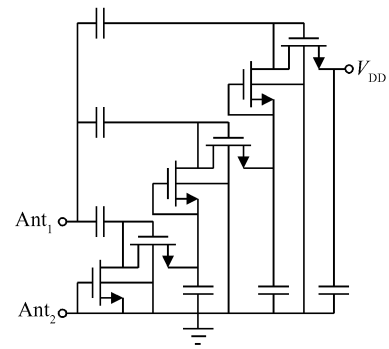

Fig. 3 Schematic of the AC-DC charge pump

3 Building blocks

3.1 Voltage rectifier

The voltage rectifier is constructed by a full wave AC-DC charge pump depicted in Fig. 3[10]. It converts the 900MHz AC energy into a DC voltage:

$$V_{DD} = 2N(V_{RF} - V_D) \tag{3}$$

where N is the stage number, V_{RF} is the amplitude of input RF voltage, and V_D is the voltage drop on a diode connected MOS transistor, which is a specified value for a given technology. Power conversion efficiency η can be defined as:

$$\eta = P_L/(P_L + P_{CP}) \tag{4}$$

where P_L is the power consumed by the load circuit, and P_{CP} is the power dissipated in the charge pump[11].

From Eq. (3), in order to supply the chip with small input amplitude, a large stage number is required. However, for a constant load, a charge pump with more stages dissipates more power on the diode connected MOS transistors. The increase of P_{CP} degrades the power conversion efficiency. Therefore, an optimal stage number exists by balancing the requirement of system supply voltage and the power conversion efficiency. In our design, the stage number N is chosen to be 3. The corresponding maximum power conversion efficiency is 20%.

3.2 Reference generator

The reference generator provides the bias voltage and current for the whole system. For passive RFID tags, three main considerations should be considered when designing the reference generator: temperature characteristics, power signal rejection ratio (PSRR), and the power consumption. A reference generator using sub-threshold techniques makes it a good candidate in tag applications because of its temperature compensation performance and low supply voltage requirement. In our design, the sub-threshold reference generator from Ref. [12] is employed. Figure 4 shows

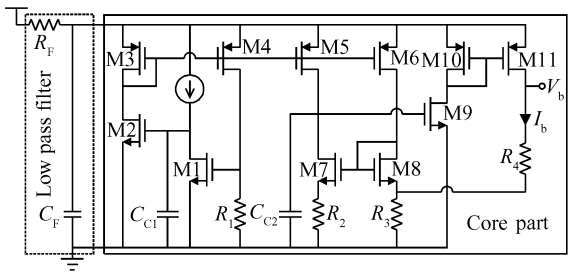

Fig. 4　Schematic of the reference generator

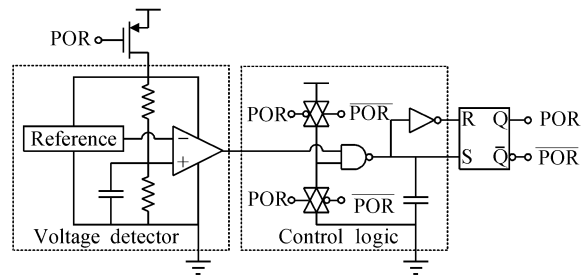

Fig. 6　Schematic of the power-on reset circuit

the circuit structure.

With a constant bias current, the gate-source voltage of a sub-threshold MOS transistor (M1) has a negative temperature coefficient, while the difference of two sub-threshold MOS transistors (M7 and M8) has a positive temperature coefficient. Temperature compensation can be achieved by adjusting the temperature coefficients of these MOS transistors. Since the output of the reference generator provides bias for the clock oscillator, the temperature performance of the reference generator can be represented by the oscillated clock frequency. Figure 5 shows the simulation results of the normalized clock frequency. In the temperature range from −40 to 100℃, the oscillated clock frequency has a deviation of only 1%. In this way, temperature compensation of the reference generator enhances the tag's reliability.

Since the supply voltage of a passive tag is not steady during data communication, power signal rejection performance is vital for the whole system. According to the C1G2 protocol[8], the possible data rates range from 40 to 640kHz. In order to keep the system working correctly, the circuit must reject signals in this frequency band. However, the lag compensation capacitor C_{C2} moves the dominant pole of the circuit core to below 640kHz. Therefore, an RC low pass filter is employed to enhance the circuit's PSRR at high frequency. For the circuit depicted in Fig. 4, the power signal transfer function of the circuit can

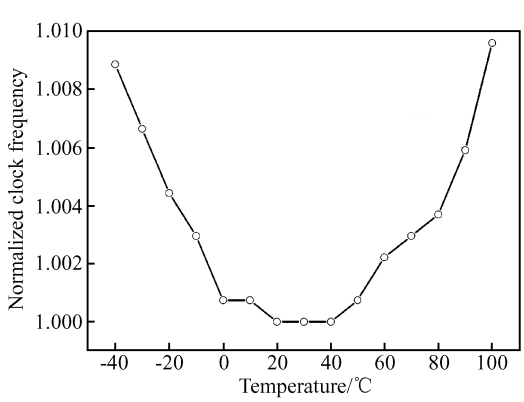

Fig. 5　Normalized clock frequency versus temperature

be regarded as the product of the RC low pass filter and the circuit core as defined by:

$$F_{RG}(f) = F_{LPF}(f)F_C(f) \tag{5}$$

where F_{RG} is the power signal transfer function of the reference generator, and F_{LPF} and F_C are the power signal transfer functions of the low pass filter and the circuit core, respectively. In our design, the corner frequency of the low pass filter is chosen to be 40kHz to cover all data rates. The simulation results of PSRR are 58dB @ dc, 40dB @ 40kHz, 47dB @ 160kHz, and 51dB@640kHz.

The supply voltage requirement of the reference generator can be written as:

$$V_{DD} \geqslant V_F + V_{GS8} + V_{DS6} + V_3 \tag{6}$$

where V_F is the voltage drop on R_F, V_{GS8} is the gate source voltage of a sub-threshold MOS transistor M8, V_{DS6} is the drain source voltage of M6, and V_3 is the voltage drop on R_3. In 0.18μm CMOS technology, the lower bound of V_{DD} predicted by Eq. (6) is approximately 0.75V. This determines the minimum allowable supply voltage of the whole system.

3.3　Power-on reset circuit

The power-on reset circuit performs the function of voltage level detection. When the supply voltage is sufficient for the tag to work, its output POR will be "1" to enable the digital base-band. The prevalent power-on reset method in tag design is to use the threshold voltage of MOS transistors[2,13]. Nevertheless, threshold voltage varies greatly with process and temperature.

Our work exploits the voltage comparison method. Figure 6 depicts the circuit schematic. It contains three parts: a voltage detector, a control logic circuit, and an RS latch. Before the tag is power-on, the voltage detector compares the input voltage with a reference. Since the reference voltage is stable over a large temperature span, the power-on level remains the same. After the output POR becomes "1", the RS latch locks the supply path of the voltage detector and maintains its input with the help of the control logic circuit. In this way, both zero power consumption and temperature insensitivity are achieved.

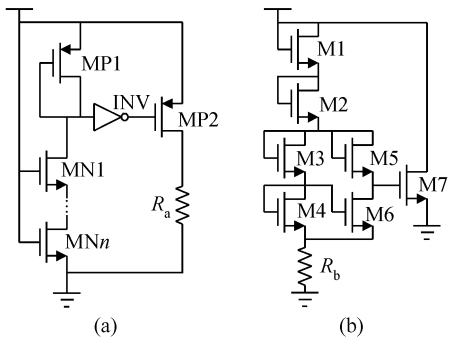

Fig. 7 (a) Regulator of this work; (b) Regulator in Ref. [2]

3.4 Voltage regulator

In a passive RFID tag, supply voltage changes greatly with the operating distance. In order to prevent devices from damaged, the supply voltage should be no higher than the nominal voltage of a specified technology (1.8V in our work). On the other hand, its static current must remain low when the supply voltage is at its lower bound.

Figure 7 (a) is the proposed voltage regulator. For comparison, the regulator in Ref. [2] is drawn in Fig. 7 (b). Figure 8 shows the simulated *I-V* curves of both circuits in logarithmic scale. For the same current piping ability at 1.8V, our work consumes only 28nA static current at the voltage of 0.75V, while that in Ref. [2] consumes 175nA. This is because at 0.75V, current piping transistor MP2 is absolutely cut off while M7 still consumes a little sub-threshold current. The inverter INV only turns on in the period of "0" ~ "1" voltage conversion and provides a large transconductance to make the piping current leap dramatically.

4 Experimental results

A complete tag chip was implemented in 0.18μm

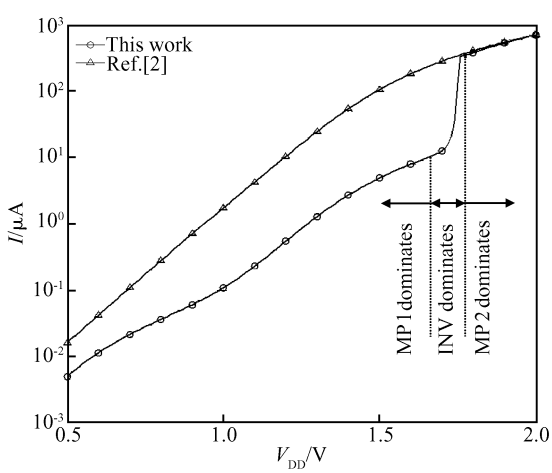

Fig. 8 *I-V* curves of the regulator

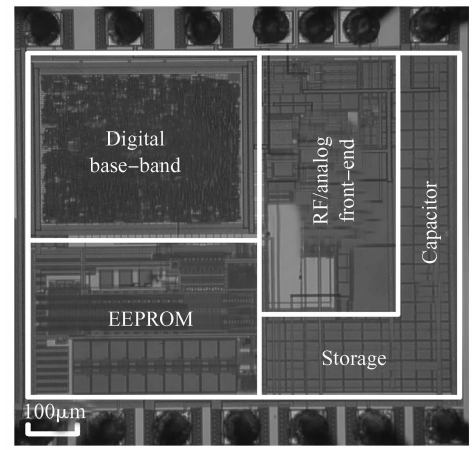

Fig. 9 Die micrograph

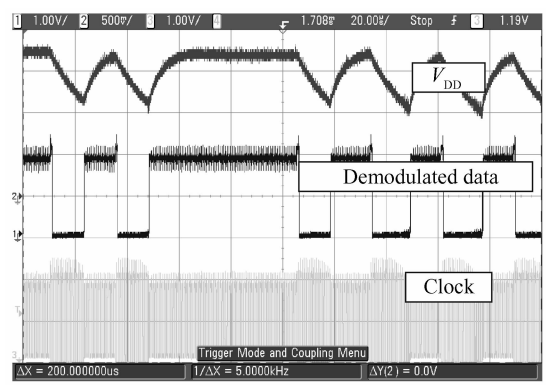

Fig. 10 Rectified voltage, demodulated data and clock

CMOS EEPROM technology without Schottkey diodes. The die size of the chip is 0.8mm^2. Figure 9 is the die micrograph. Measurement results show that the minimum allowable supply voltage is 0.75V, which agrees well with Eq. (6). At this voltage, total current of the RF/analog front-end circuit is 4.6μA. Communication tests were carried out with a 900MHz C1G2 compliant reader[8]. Figure 10 gives the measured signals of the rectified supply voltage V_{DD}, demodulated data, and clock. The chip can process ASK modulated code in pulse-interval encoding (PIE) format, while the modulation depth can be varied from 80% to 100%. The allowable forward link data rate of the system ranges from 40 to 160kb/s. The oscillated clock frequency is 1.28MHz. Comparisons of this circuit's performance with some of the latest work are listed in Table 1. Our work distinguishes itself by its low voltage and temperature insensitive performance.

Table 1 Result comparison

	Ref. [5]	Ref. [6]	Ref. [7]	This work
Process	0.25μm	0.18μm	0.35μm	0.18μm
V_{DD}/V	2	No report	1.5	0.75
I_{DD}/μA	4	10	10.6	4.6
Temperature compensation	Yes	No	No	Yes

5 Conclusion

This paper presents an RF/analog front-end circuit for a passive UHF RFID tag. With a sub-threshold reference generator，a zero static current power-on reset circuit，and a novel voltage regulator，the RF/analog front-end circuit is characterized by low voltage，low power，and temperature insensitivity. The circuit is implemented in 0.18μm CMOS EEPROM technology with digital base-band and EEPROM. It is suitable for tags requiring low cost，long distance operation，and good reliability.

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一种适用于无源超高频射频识别标签的低电压低功耗射频/模拟前端电路*

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摘要：提出了一种适用于无源超高频射频识别标签的低电压低功耗射频/模拟前端电路. 通过引入一个使用亚阈值技术的基准源，电路实现了温度补偿，从而使得系统时钟在－40～100℃的范围内保持稳定. 在模块设计中，提出了一些新的电路结构来降低系统功耗，其中包括一种零静态功耗的上电复位电路和一种新的稳压电路. 该射频/模拟前端电路采用不带肖特基二极管 0.18μm CMOS EEPROM 工艺流片实现，它与数字基带、EEPROM 一起实现了一个完整的标签芯片. 测试结果表明，该芯片的最低电源电压要求为 0.75V. 在该最低电压下，射频/模拟前端电路的总电流为 4.6μA.

关键词：射频识别技术；标签；低电压；低功耗；温度补偿

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