Analysis and Modeling of Broadband CMOS Monolithic Balun up to Millimeter-Wave Frequencies

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Abstract: The implementation of broadband monolithic baluns based on CMOS technology is investigated. The configuration and parameterized layout are analyzed. Then, a wide-band lumped element equivalent circuit model accounting for all necessary physical effects is proposed and model parameters are extracted, with high accuracy in a broadband frequency range, via combination of physical formula and fitting optimization. Two baluns were implemented with TSMC's one-poly eight-metal (1P8M) 0.13μm mixed-signal (MS)/RF CMOS process. The *S*-parameters of these two baluns were measured using a vector network analyzer. The measured results agree well with the modeled parameters up to millimeter-wave frequencies.

Key words: modeling; millimeter-wave; CMOS
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1 Introduction

In modern wireless communication systems, radio frequency (RF) carrier signals are increasing toward tens of GHz where a larger channel capacity and a higher data transmission rate can be obtained. In order to meet the potentially high demand for such wireless communications, wide-band low-cost silicon-based RF integrated circuits (RFICs) are indispensable. The rising demand for low-cost RFICs has stimulated research on the design and implementation of on-chip high-quality passive components in CMOS technology due to its advantages of mass-production, low cost, and compatibility with digital and analogy circuits. The employment of monolithic passive components has been widely demonstrated to enhance the performances of RFICs.

The differential architecture wireless transceiver can have better performance than its single-ended counterpart because all common-mode signal components can be fully repressed by the counteract function of the circuit structure. Common-mode rejection ability is particularly important in state-of-the-art wireless system design, in which efforts are ongoing to integrate the entire transceiver circuitry in one single chip. The receiver should work with circuitry containing a large number of mixed-signal function blocks, where both the power supply and the substrate may introduce a large amount of undesired common-mode signal and noise. However, the signals from or to transceiver antenna are often single-ended. Thus, a balun (balanced-to-unbalanced) is needed to realize an effective connection between a balanced circuit and a single-ended signal source or load.

A variety of baluns have been developed during the past decades[1~5]. Few of them, however, are focused on the frequency range over 10GHz when implemented with standard CMOS technology. It is important to investigate the monolithic baluns which operate on a wide frequency band higher than 10GHz. Moreover, there is still no accurate model for wide-band monolithic baluns so far, which is necessary for time-domain simulation and noise analysis. In this paper, the configuration and the layout design of wide-band CMOS on-chip baluns are discussed. Then, a lumped element wideband model of monolithic baluns is presented. Several baluns are realized in TSMC's 0.13μm RF/MS CMOS process. The *S*-parameters of the realized baluns were measured with an Agilent E8363B VNA. The results show a high agreement with modeling parameters up to millimeter-wave frequencies.

2 Configuration and parameterized layout

Many structures, such as rat-race hybrids, waveguide magic tees, Lange, and so on, can be used to implement baluns at RF and microwave frequen-

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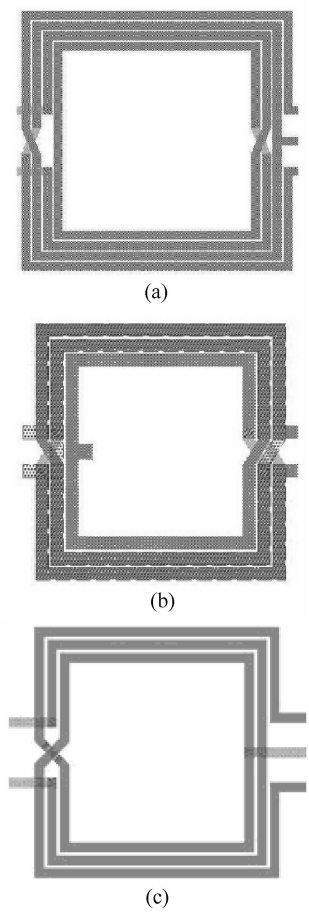

Fig. 1 Structures of the planar spiral transformer balun (a) Tapped structure; (b) Stacked structure; (c) Interleaved structure

cies. Major limitations of these components are their narrow bandwidths and the lack of methods for center-tap grounding. Hence, planar spiral structures should be preferred in the realization of on-chip baluns. The planar spiral transmission line and center-tapped planar spiral transformer are two considerable candidates. Yet, Yeong *et al*. has shown that the performance of the former would severely degrade when fabricated on low resistivity (less than 20Ω · cm) silicon substrates[3]. As a result, a centre-tapped planar spiral transformer structure is chosen in this paper.

There are approximately three types of on-chip planar spiral transformers, that are suitable for balun implementation. They are the tapped structure, the stacked structure, and the interleaved structure. No matter which is selected, a symmetric layout should be employed. The tapped structure, illustrated in Fig. 1 (a), has a maximized self-inductance and a minimized terminal-to-terminal capacitance. Unfortunately, its mutual coupling is too low. The stacked structure is shown in Fig. 1 (b). Although this structure can provide the highest coupling and the best area efficiency, its main drawback is low self-resonance frequency (SRF), resulting in a restricted bandwidth. Moreover, this structure requires multiple metal layers. The other metal layers are much thinner than the top layer in most CMOS processes, which will worsen the insertion loss. The interleaved structure, illustrated in Fig. 1 (c), is employed in our design so as to meet bandwidth and coupling requirements simultaneously.

The layout of the balun in Fig. 1 (c) is parameterized based upon several geometrical attributes: outer diameter/inner diameter, line width, line spacing, and turns-ratio. The performances of the balun, such as the insertion loss, the mutual coupling coefficient, and the bandwidth, are dependent on the geometrical attributes. The mutual coupling coefficient increases when the number of winding turns increases or the space between adjacent turns decreases. However, the parasitic capacitance between adjacent turns will decrease SRF significantly when too many winding turns are employed. The less space there is, the more coupling between primary and secondary there is. The space has a minimum limited by the design rule of the employed process. In this paper, it is 2μm. The inner turns have a higher resistivity than the outer turns at high frequencies due to eddy current and their contribution to inductance is minimal[6]. This is the main reason to leave the spiral center empty. In addition, the balun's operation frequency range is dependent on the outer diameter. The frequency limit lowers as the outer diameter increases. The selection of metal width should balance metal loss and magnetic coupling. A wider metal will reduce the metal loss but also reduce the magnetic coupling. Conversely, a narrower metal will cause a higher metal loss but increase the magnetic coupling.

3 Equivalent circuit

Although the performance of a balun can be characterized by frequency domain network parameters, like *S*-, *Y*-, or *Z*-parameters, the equivalent circuit is still necessary in time domain simulation or noise analysis. The proposed equivalent circuit for a three-port balun is shown in Fig. 2. The low frequency effect of the single-ended primary and differential secondary of the balun, including inductance and resistance, can be modeled using series resistances (R_1, R_2, R_3) and series inductances (L_1, L_2, L_3), with mutual inductances between each two inductances denoted by (M_{12}, M_{13}, M_{23}). The skin and proximity effect[7] of the metal coils at higher frequencies are modeled by three *RL* branches $\{R_{ii}, L_{ii}(i=1,2,3)\}$ and six mutual inductances M_{pij} (here, the subscript p denotes proximity) between L_{ii} and L_j ($i, j = 1,2,3$, $j \neq i$), respectively. The parasitic capacitive coupling

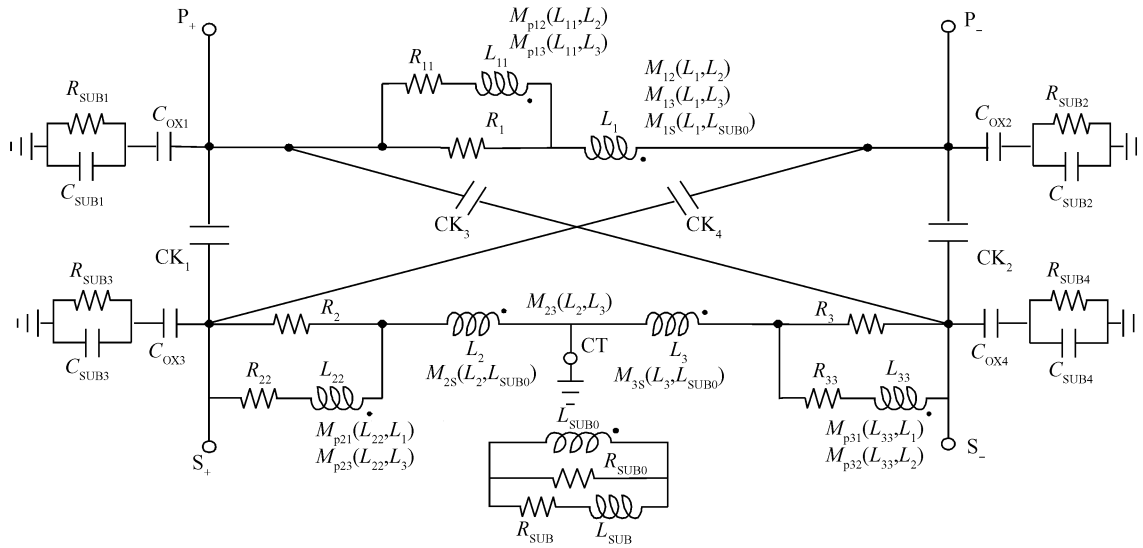

Fig. 2　Proposed equivalent circuit model of planar transformer balun

between primary and secondary windings is modeled by four components CK_1, CK_2, CK_3, and CK_4. The coupling between conductive substrate and the metal windings can be divided into two parts: the capacitive and the inductive. The capacitive coupling is modeled by four substrate RC networks comprised of C_{OXi}, R_{SUBi} and C_{SUBi} ($i = 1,2,3,4$). In balun applications, the port P_+ or P_- is grounded due to the fact that the primary is single-ended. However, only three of the four are effective. The patterned ground shield (PGS)[8] is not adopted because the parasitic capacitance between the metal coils and the PGS makes the SRF become too low. But, eddy current will be induced in the underlying substrate by the penetration of the magnetic field into the conductive silicon substrate without PGS. The network components, including L_{SUB0}, R_{SUB0}, L_{SUB}, and R_{SUB}, can be used to simulate the loss caused by eddy current and the corresponding skin effect of the substrate. The mutual inductances M_{1S}, M_{2S}, and M_{3S} are employed to represent the inductive coupling between the silicon substrate and the metal coils.

The most important aspect for modeling an on-chip balun is the extraction or fitting of model parameters. Most of the purely physics-based modeling can only provide estimates and the error will increase rapidly as the frequency goes up. Another popular approach for parameter extraction is based on the fitting optimization of frequency domain network parameters. The starting point of fitting optimization is a frequency domain matrix that provides the port responses. In a microwave circuit, it is usually an *S*-parameter matrix. Measurements are the preferred origin of the parameters. The process of fitting optimization to minimize the *S*-parameter error between the equivalent circuit model and the measured values can be performed with a commercial software like Agilent ADS. As shown in Fig. 2, there are more than forty unknown parameters in the proposed model. The fitting process may be very time consuming and prone to potential convergence problems with so many parameters. In this paper, the model parameters are extracted with high-precision in a wide frequency band via the combination of physical analytic formulas with fitting optimization.

The parameter extraction steps are as follows: The series inductance L_i, series resistance R_i, and RL branch components L_{ii}, R_{ii} ($i = 1,2,3$) satisfy the following physical constraints[7]:

$$L_i / L_{ii} = 0.315 R_{ii} / R_i \tag{1}$$

$$R_i^{dc} = R_i R_{ii} / (R_i + R_{ii}) \tag{2}$$

$$L_i^{dc} = L_i + (R_i / (R_i + R_{ii}))^2 L_{ii} \tag{3}$$

where R_i^{dc} and L_i^{dc} are the DC resistance and inductance of the ith spiral, respectively. The value of each R_i^{dc} is equal to the product of the metal sheet resistance and the aspect of the metal line (total metal length/metal width). The L_i^{dc} can be calculated by:

$$L_i^{dc} = 9.375 \mu_0 N_i^2 AD_i^2 / (11OD_i - 7AD_i) \tag{4}$$

where μ_0 is the permeability of the free space, N_i is the turn numbers of the ith spiral, AD_i is the average diameter, and OD_i is the outer diameter. Equations (1)～(3) show that only one of the four group variables: ($\{R_i\}$, $\{L_i\}$, $\{R_{ii}\}$, $\{L_{ii}\}$, $i = 1,2,3$) need fitting. The $\{R_{ii}\}$ is selected in this paper. Three mutual inductances M_{ij} ($i, j = 1,2,3, i < j$) can be estimated using the following expressions:

$$M_{ij} \approx \mathrm{Imag}(Z_{ij}) / \omega \tag{5}$$

where Z_{ij} are the elements of the *Z*-parameter matrix, which is converted from measured the *S*-parameter matrix, while ω should be low enough (in this pa-

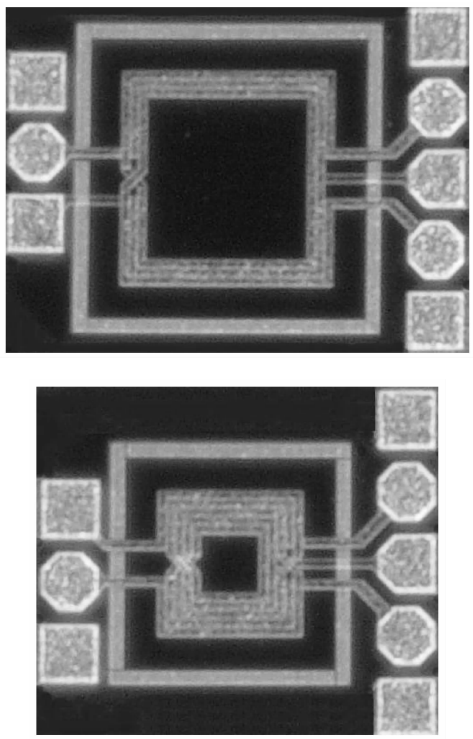

Fig. 3 Micrographs of two implemented baluns

per, $\omega = 2\pi \times 100$MHz). It is difficult to calculate the proximity effect mutual inductances M_{pij} ($i, j = 1, 2, 3, i \neq j$) by an analytical formula, so M_{pij} is also obtained by fitting iteration. However, the following equations can be assumed using symmetry of layout: $M_{p12} = M_{p13}$, $M_{p21} = M_{p31}$, $M_{p23} = M_{p32}$. The coupling capacitances between primary and secondary, $CK_1 \sim CK_4$, consist of two kinds of parasitic effects. The first is the sidewall capacitance of thick conductors existing between adjacent metal wires. The second is the overlap area capacitance between the top metal layer and the underpass. The former can be calculated by an analytical approximation based on conformal mapping[9] and then scaled by the metal length. The latter can be estimated approximately by the commonly used parallel plate capacitor formula. The total coupling capacitance between the primary and secondary coils, namely C_{PS}, is the summation of the two. Then, the $CK_1 \sim CK_4$ can be estimated by: $CK_1 = CK_2 = CK_3 = CK_4 = 1/4\ C_{PS}$. As for the components related to the coupling between substrate and metal coils, including both capacitive and inductive, a series of complex analytical formulas derived by Huo *et al*. with the knowledge of balun layout and process technology[10] can be employed to calculate their values.

4 Measurement results and model verification

Several baluns were fabricated in TSMC's 0.13μm RF/MS CMOS process to verify the performances of on-chip baluns and examine the validity of the proposed lumped element equivalent circuit model. Figure 3 shows the micrographs of two implemented baluns. The outer diameter (OD) of the upper balun is 300μm and its turns-ratio is 1 : 2. The OD of the lower is 200μm and the turns-ratio is 3 : 2. Both line widths are 10μm. The line spacing of both, as mentioned above, is 2μm. The standard GSG pad for single-end and GSGSG for differential are added to perform an on-wafer measurement. The influence of the pad parasitic has been removed with the de-embedding technique.

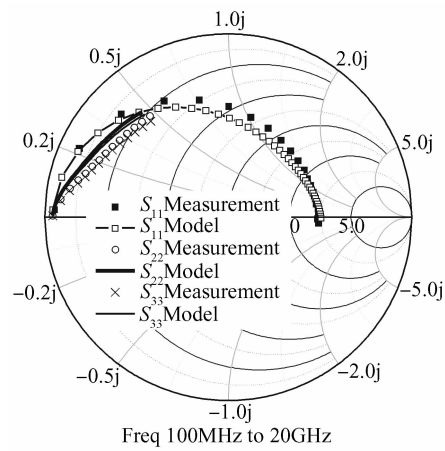

Fig. 4 S_{11}, S_{22} and S_{33} of the 3 : 2 balun

The on-wafer measurement has been performed with an Agilent E8363B VNA, which is a two-port VNA, while balun is a three-port device. When measuring *S*-parameters of multi-port devices using a general two-port VNA, the remaining ports should be terminated by auxiliary loads[11]. The loads may be arbitrary. In our measurement, a 50Ω standard load from Agilent was used such that the *S*-parameter matrix for 50Ω characteristic impedance at all ports can be obtained. The *S*-parameters of the two baluns have been measured up to 20 and 30GHz, respectively. The extracted equivalent circuit parameters of the 3 : 2 balun are as follows: $L_1 = 1.77$nH, $L_2 = L_3 = 0.33$nH, $R_1 = 0.95\Omega$, $R_2 = R_3 = 0.39\Omega$, $L_{11} = 0.28$nH, $L_{22} = L_{33} = 0.11$nH, $R_{11} = 19.2\Omega$, $R_{22} = R_{33} = 3.63\Omega$, $M_1 = M_2 = 0.48$nH, $M_3 = 0.11$nH, $M_{p12} = M_{p13} = 0.07$nH, $M_{p21} = M_{p31} = -0.15$nH, $M_{p23} = M_{p32} = -0.068$nH, $C_{OX1} = C_{OX2} = 31$fF, $C_{OX3} = C_{OX4} = 14$fF, $R_{SUB1} = R_{SUB2} = 592\Omega$, $R_{SUB3} = R_{SUB4} = 173\Omega$, $C_{SUB1} = C_{SUB2} = 5.9$fF, $C_{SUB3} = C_{SUB4} = 2.7$fF, $CK_1 = CK_2 = CK_3 = CK_4 = 53$fF, $L_{SUB0} = 1.2$nH, $L_{SUB} = 4.2$nH, $R_{SUB0} = 540\Omega$, $R_{SUB} = 87\Omega$, $M_{1S} = 1.27$nH, $M_{2S} = M_{3S} = 0.44$nH. Its measured and simulated S_{11}, S_{22} and S_{33} are shown in Fig. 4. From Fig. 4, the SRF of this balun is less than 20GHz. Figure 5 shows the real and imaginary part of S_{21} and

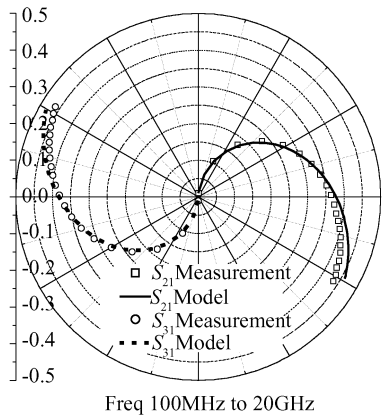

Fig. 5　S_{21} and S_{31} of the 3∶2 balun

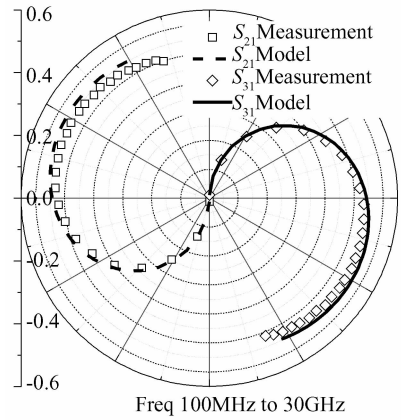

Fig. 7　S_{21} and S_{31} of the 1∶2 balun

S_{31}. The measured results show good agreement with the model.

An important characteristic of the transformer balun is that it can be used as an impedance transformer when the turns-ratio is not equal. Thus, the insertion loss represented by S_{21} and S_{31} is associated with input and output impedance levels. The insertion loss can be reduced by terminating single-ended and differential ports with proper impedances. The extracted equivalent circuit parameters of the 1∶2 balun are as follows: $L_1 = 0.65$nH, $L_2 = L_3 = 0.75$nH, $R_1 = 0.83\Omega$, $R_2 = R_3 = 0.76\Omega$, $L_{11} = 0.89$nH, $L_{22} = L_{33} = 0.44$nH, $R_{11} = 1.93\Omega$, $R_{22} = R_{33} = 4.09\Omega$, $M_1 = M_2 = 0.42$nH, $M_3 = 0.31$nH, $M_{p12} = M_{p13} = -0.02$nH, $M_{p21} = M_{p31} = 0.048$nH, $M_{p23} = M_{p32} = -0.19$nH, $C_{OX1} = C_{OX2} = 24.5$fF, $C_{OX3} = C_{OX4} = 41$fF, $R_{SUB1} = R_{SUB2} = 887\Omega$, $R_{SUB3} = R_{SUB4} = 964\Omega$, $C_{SUB1} = C_{SUB2} = 7.4$fF, $C_{SUB3} = C_{SUB4} = 5.3$fF, $CK_1 = CK_2 = CK_3 = CK_4 = 37$fF, $L_{SUB0} = 0.4$nH, $L_{SUB} = 3.7$nH, $R_{SUB0} = 1189\Omega$, $R_{SUB} = 43\Omega$, $M_{1S} = 0.45$nH, $M_{2S} = M_{3S} = 0.32$nH. Figure 6 shows its measured and simulated S_{11}, S_{22} and S_{33}, demonstrating that this balun can operate at frequencies higher than 30GHz, which belongs to millimeter-wave frequencies. The simulated S_{22} and S_{33} overlap because of perfect symmetry. The transmission S_{21} and S_{31} are shown in Fig. 7. The modeling results agree well with the measurement results up to millimeter-wave frequencies.

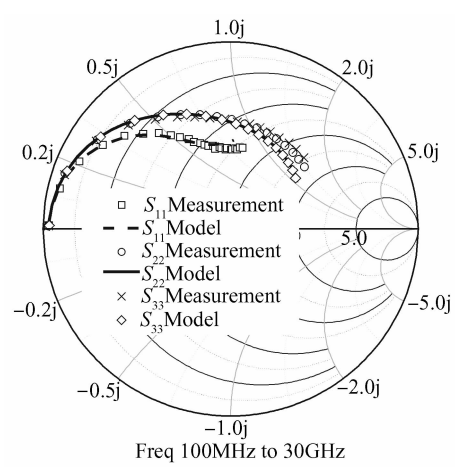

Fig. 6　S_{11}, S_{22} and S_{33} of the 1∶2 balun

Not only the *S*-parameters must be observed, there is another important specification for balun, i.e. imbalance, including magnitude and phase. The imbalance can be calculated by the measured *S*-parameters.[12] The calculation indicates that the two implemented baluns in this paper have good symmetry. Both absolute magnitude imbalances are <0.5dB and the absolute phase imbalances are $<7^\circ$.

5　Conclusion

The implementation of broadband on-chip baluns based on CMOS technology is demonstrated. In order to meet the bandwidth and coupling requirements concurrently, the interleaved layout structure should be employed. A novel broadband lumped element model accounting for all physical effects is proposed. The model parameters are extracted, with high-precision in a wide frequency band, via a combination of physical analytic formulas with fitting optimization. Two baluns with good performance were implemented using TSMC's 0.13μm RF/MS CMOS process and measured with Agilent E8363B two-port VNA. The measured results show good agreement with the model up to millimeter-wave frequencies.

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毫米波频段宽带 CMOS 片上巴伦的分析与建模

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摘要：详细讨论了基于 CMOS 工艺宽带片上巴伦的实现. 首先分析了应当采用的结构及参数化版图. 然后给出了一个宽带集总元件等效电路模型，该模型考虑了各种必须考虑的物理效应. 通过采用物理公式与优化拟合相结合的方法提取了模型参数，以保证模型在很宽频带范围内具有较高精度. 最后，采用台湾半导体制造有限公司(TSMC)提供的 0.13μm 混合信号/射频 CMOS 工艺实际制作了两个具有不同几何参数的巴伦，并使用 Agilent E8363B 矢量网络分析仪测量了 S 参数. 测量结果表明在高达毫米波频段范围内，模型仿真结果与测试结果符合得很好.

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