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Multiple Node Upset in SEU Hardened Storage Cells

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Abstract: We study the problem of multiple node upset (MNU) using three-dimensional device simulation. The results show the transient floating node and charge lateral diffusion are the key reasons for MNU. We compare the MNU with multiple bit upset (MBU), and find that their characteristics are different. Methods to avoid MNU are also discussed.

Key words: multiple node upset; hardened cell; charge collection
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1 Introduction

Hardening by design is an important technique to solve the single event upset (SEU) problem. The basic idea of hardening by design is to provide a memory element with an appropriate feedback devoted to restoring data when corrupted by an ion hit. Hardening by design uses standard CMOS process without any additional mask. Its cost is lower than the SOI process, and its performance does not degrade as much as resistive hardening.

In the past two decades, many SEU hardened storage cells have been proposed. In 1988, the first SEU hardened latch was presented[1]. It consisted of a standard 6-transistor memory cell surrounded with 6 p-channel transistors. Including input buffers, there are 16 transistors in this latch. Experimental results show that no errors were detected for particles having an LET_{th} of $74MeV/mg/cm^2$[2]. A different hardening cell was presented in Ref.[3], and an improved design to decrease the static power was presented in Ref.[4]. Experiments show they have LET_{th} of 120 and $39MeV/mg/cm^2$, respectively[5]. References [2, 6] proposed two heavy ion tolerant (HIT) cells. Their upset cross section is much smaller than the standard SRAM cell. Dual interlocked storage cell (DICE)[7] is another hardened cell. A new approach to harden SRAM cells was presented in Ref.[8]. The LET_{th} is $50MeV/mg/cm^2$[9].

All these hardened cells outperform standard SRAM cells. But, there are still two questions. The first is how these cells upset. In theory, these cells are immune to any amount of charge collection at a single node. However, the experimental results do not confirm this. Experimental results show that the HIT cell upsets under a laser of 12pJ. Reference [8] also reported the hardened cell was upset with low LET ion incidence. The second question is why the LET_{th} of each cell is different. The LET_{th} of the cell in Ref.[3] is $120MeV/mg/cm^2$, while the LET_{th} of the cell in Ref.[4] is only $39MeV/mg/cm^2$.

References [10, 11] reported that a single ion could upset multiple bits in DRAM and SRAM because of lateral charge transport. This phenomenon may also occur in multiple nodes of an SEU hardened cell. Multiple node upset is believed to be the main reason for the upset of the hardened cells[7]. However, the interplay of the charge collection and voltage change is still unclear. Recently, 3D device simulation has been widely used in SEU study, and the results are accurate enough to undertake experiments[12]. In this paper, we use full 3D device/circuit mixed-mode simulation to demonstrate that the mechanism of the multiple node charge collection upsets SEU hardened cells, and to investigate MNU sensitivity.

2 Simulation setup

First, we study the ROCK cell (Rockett presented it in Ref.[1]) in detail. The conclusion will be applied to other cells later. As Figure 1 shows, Pa, Pb, Na, Nb transistors consist of a standard storage latch. P1, P2, P4, P6 consist of a redundant storage place. P2 and P5 provide feedback paths to recover upset of Q and Q'. In ROCK cells, the transistors' size is chosen as: P3>P1, P6>P4, P2>Na, P5>Nb.

The ISE TCAD toolset was used to carry out the simulation. The device model is built by DEVISE tool. Here, we model two pMOS transistors, pMOS1

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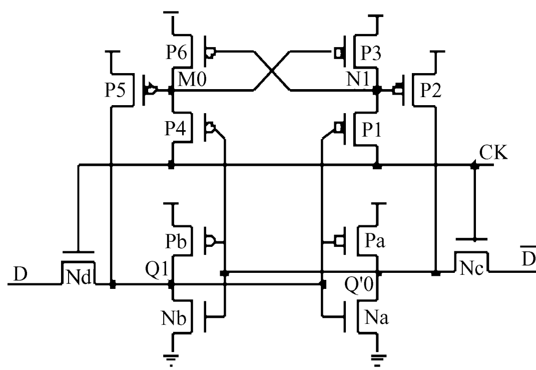


Fig. 1　ROCK cell

and pMOS2, as shown in Fig. 2. The technology is based on a 1μm commercial bulk CMOS process. The width of the two pMOS is 7μm, and the length is 1μm, as seen in Ref. [1]. They were placed 7μm from each other. The MESH tool generated the 3D grid. The grid structure was set up to reflect exactly the layout dimensions of the technology. Mesh refinement is done in the regions of interest: the channels, lightly doped drain, and junction boundaries.

The DESSIS tool performed the simulation. We set the simulation conditions in a DESSIS cmd file. The main physical models activated in the simulations include field- and concentration-dependent mobility models, taking into account the effect of velocity saturation of the carriers, and concentration-dependent Shockley-Read-Hall and Auger recombination models. We also take into account the band-gap narrowing effect. The heavy-ion effect is simulated with an electron-hole pair column with the track as its axis. The ion used in simulation has an LET of 0.5pC/μm. The length and radius of the ion track are 9.5 and 0.48μm, respectively. The ion penetrates the device at 5ps. The simulation time ranges from 0.1ps to 1μs.

Also in DESSIS cmd file, we set up the external circuit for the device model. The external circuits are described in a DESSIS built-in MOSFET Level 6 circuit model. They are coupled with the device model at the contact. Transistors, in which charge collection is not taken into account, are described as external circuits.

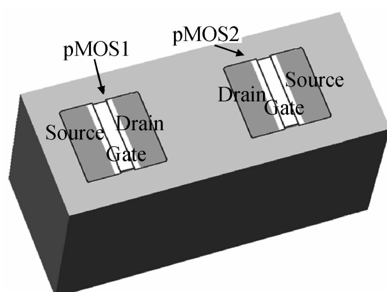


Fig. 2　Device model

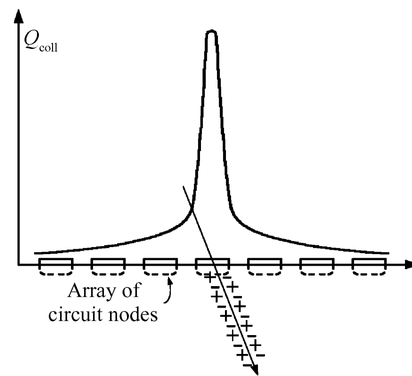


Fig. 3　Multiple node charge collection

3　Multiple node upset simulation

References [12, 13] studied multiple bit upset (MBU) in DRAM and SRAM. They found that heavy ions can affect several adjacent p-n junctions by lateral charge transport. As presented in Fig. 3, when an ion impacts, there will be very high density electron-hole pairs through the ion track. Most charge is collected by the funnel around the track. A little mount of electron-hole pair diffuses widely, although the density decreases. If it reaches another sensitive node, charge will be collected there. If enough charge collects, this node will be upset. It is believed that MBU will be most likely to occur when an ion strikes in the middle of the multiple nodes, because charge will diffuse equally to every node. If an ion strikes directly at one sensitive node, the funnel will decrease the amount of charge diffused to other nodes.

For comparison, we first simulate the single node charge collection in a ROCK cell. The cell is modeled as Fig. 4. Only the Pa transistor is modeled at the

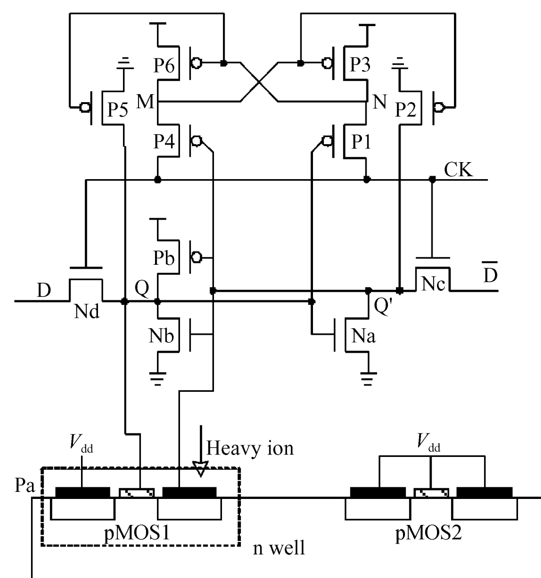


Fig. 4　Single transistor modeled at the device level

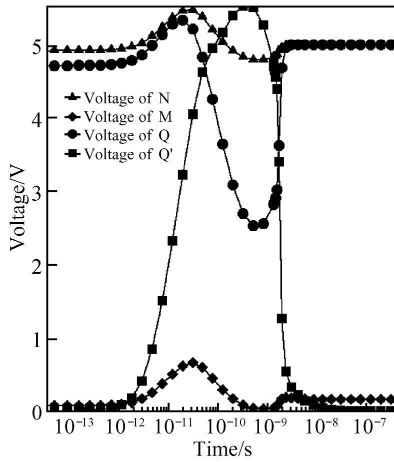


Fig. 5 Single node charge collection

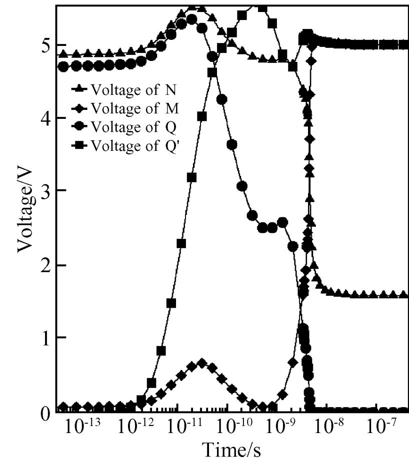


Fig. 7 Multiple node charge collection

device level, corresponding to pMOS1 in Fig. 2. Other all transistors are modeled at the MOSFET Level 6 circuit level. The size of the transistors is from Ref. [1]. The initial voltage of each node is set to be the same as Fig. 1. Pa is in the OFF state. Its reverse bias drain is sensitive to charge collection. pMOS2 is not used here, and all of its contacts are set to $V_{\rm dd}$. A 0.5pC/μm ion strikes at the center of the drain of Pa. Figure 5 shows the voltage change of each node. At 5ps, Q' rises quickly from 0 to 5.5V because of direct charge collection at the drain of Pa, which causes Q to decline. Transistor P1 is turned on. But N will not change because P3 is also conducted and it is bigger than P1 in size. M will remain as low because it is floating, so P2 will remain conducted. After 1.5ns the charge collection is completed, because the $I_{\rm sat}$ of P2 is larger than that of Na, the voltage of Q' will be driven to 0. The cell will recover to the state in Fig. 1. Therefore, the ROCK cell can tolerant single event upset.

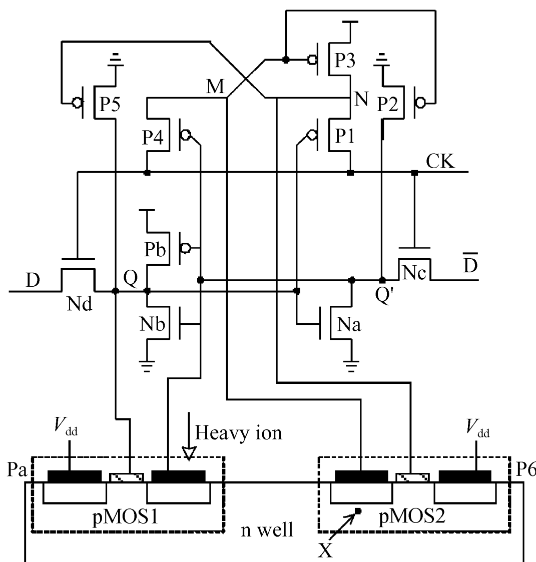


Fig. 6 Two transistors modeled at the device level

Next, we simulated the multiple node charge collection in a ROCK cell. The cell is modeled as Fig. 6. Pa and P6 are both modeled at the device level. Pa corresponds to pMOS1, and P6 corresponds to pMOS2 in Fig. 2. Other transistors are modeled in a MOSFET Level 6 circuit model. The initial voltage of each node is the same as Fig. 1. Pa and P6 are both in the OFF state. Their reverse bias drains are sensitive to charge collection. An ion with the energy of 0.5pC/μm strikes at the drain of Pa. Figure 7 shows the voltage change of each node. At 5ps, Q' rises quickly from 0 to 5.5V because of charge collection. This causes Q to decline. Transistor P1 is turned on, and P4 is turned off. Before 1ns, N node does not change because P3 is bigger in size than P1; and M will remain low because it is floating. But after 1ns, the M node rises to 5V. This turns off transistor P3. Node N is pulled down by P1. P2 is cut off and P5 is conducted, which helps Q upset to 0. Ultimately, the whole cell is upset. Thus, a single ion strike is capable of upsetting ROCK cells when considering MNU.

Compared Fig. 7 with Fig. 5, we find that Figures 5 and 7 are almost the same before 1ns, but they are much different after. Therefore, the voltage change of

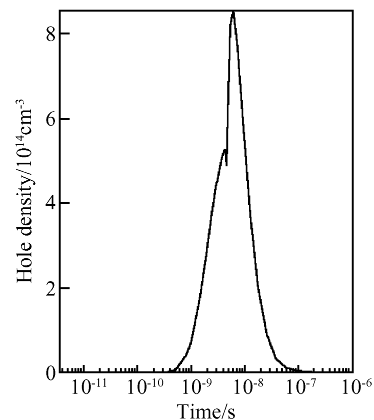


Fig. 8 Hole density at X point

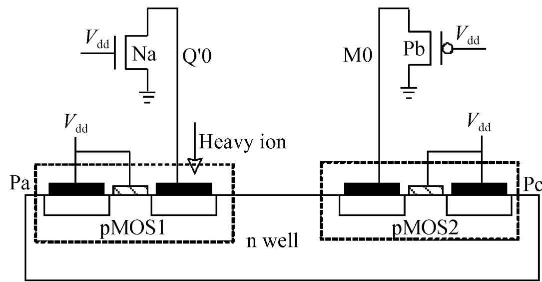


Fig. 9　Charge diffusion to an independent floating node

the M node after 1ns is the key for the total cell upset. Figure 8 presents the hole density of the X point in Fig. 1, which is under the drain junction of pMOS2 and explains why the M node upsets. Before 1ns, the hole density is 0. After 1ns, the hole density rises because the hole generated in the ion track diffuses there. The maximum hole density reaches 8×10^{14} cm^{-3}. However, the hole density is still much lower than that in the ion track, which is more than 1×10^{18} cm^{-3}. How can such a low density charge upset the M node? Because at 1ns, Q' upsetting to 5V results in the M node floating, so the M node retains its voltage only by parasitical capacitance and has no charge supplement. The Q_{cir} of M node is very small. Although the charge collected is small, it is still enough to upset the floating M node.

From this analysis, we conclude that MNU is attributed to two factors. One is that an ion strike upsets the first node, causing the second node to float for a certain period. The other is charge diffusion to the second node when enough charge is collected. It is important to know which is more crucial. We modified the DESSIS command file and built a circuit/device mixed-model, as shown in Fig. 9. Q' node is pulled down by Na and M node is floating with an initial voltage of 0V. An ion with the energy of 30pC/μm strikes at the drain of pMOS1. The result is presented

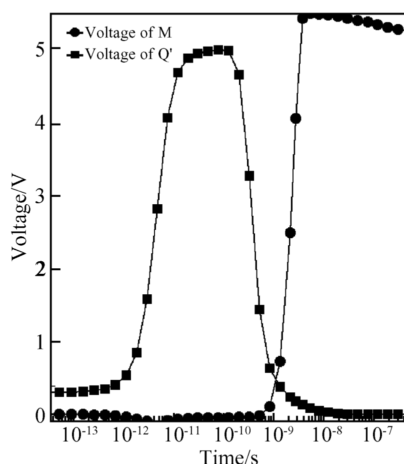


Fig. 10　Time of one node being upset

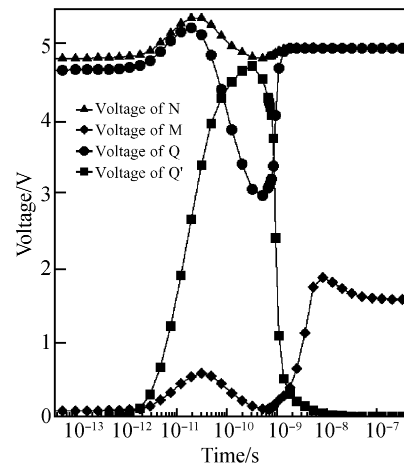


Fig. 11　ROCK no upset at 30

in Fig. 10. The ion strike upsets Q' and M in succession. An ion strike with the energy of 30pC/μm is also simulated for the model in Fig. 7. The result is much different. As Figure 11 shows, the ion strike upsets Q', but M remains low. From Fig. 10, we know that the diffusion charge is capable of upsetting the M node if it is floating. But in Fig. 11, before diffusion charge reaches, Q' has been pulled back to 0V. The M node is no longer floating. The charge supplement through P4 prevents M from upsetting. Thus, the MNU sensitivity is mainly determined by how long the ion strike can hold the first node upset.

4　Comparison of MNU and MBU

From the last section, we know that MNU will occur in an SEU hardened cell because of lateral charge diffusion. This mechanism is similar to the multiple bit upset (MBU). But in MNU, one upset node is a floating node. This makes MNU somewhat different from MBU. MBU in SRAM cells has been studied in Ref. [13] using 3D device simulation. We will now compare the characteristics of MBU and MNU.

We first compare the sensitive region. We wrote several different DESSIS cmd files. In each cmd file, the 0.5pC/μm ion is set to strike a different point between pMOS1 and pMOS2, and the external circuit is the same as Fig. 5. A script was built to call DESSIS to perform all these computations. The simulation results make up an upset map, as shown in Fig. 12. The

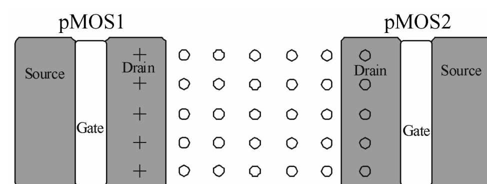


Fig. 12　MNU upset map

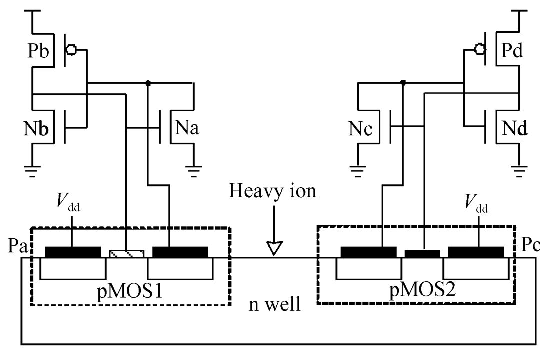


Fig.13 Two SRAM cells

cross indicates an ion strike at this point that caused upset, while the circle shows the ion strikes that did not cause upset. From Fig. 12, we can find the upset points are around the drain of pMOS1. We changed the external circuit, make pMOS1 and pMOS belong to two independent SRAM cells, as shown in Fig. 13, and performed the simulation again. We obtained another upset map of MBU, as shown in Fig. 14. The upset points are in the middle of the two transistors. This map is similar to the result in Ref. [13]. Figure 12 is much different from Fig. 14, which can be explained by the mechanism of floating node upset. In ROCK cells, a direct ion strike at the drain of one transistor will make another node float and make this node much easier to upset. But in MBU, the two nodes are independent. The distance between ion incident point and drain determines whether upset occurs. Thus, an ion strike at the middle point is most likely to upset the two nodes synchronously.

The sensitivity of MNU in the ROCK cell is compared to MBU. First, we use different LET for simulating MNU in ROCK cells. A script is built for DESSIS, in which the LET scan from 0.2 to 0.8pC/μm with a step of 0.02pC/μm. Results show that the first upset occurs at 0.42pC/μm. Then, we modify the circuit description in the DESSIS command file. The circuit and device model form two independent SRAM cells, as shown in Fig. 9. Ion strikes in the middle of pMOS1 and pMOS2. Also, we scan LET from 0.2 to 0.8pC/μm with a step of 0.02pC/μm. In this case, the first upset occurs at 0.68pC/μm. Thus, we can conclude the MNU in a ROCK cell is much more sensitive than the MBU of two independent nodes. This also can be explained by the transient floating node. It is

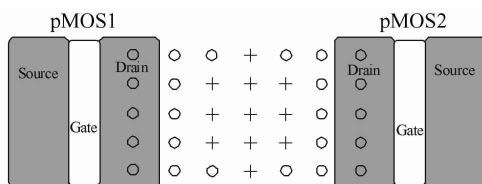
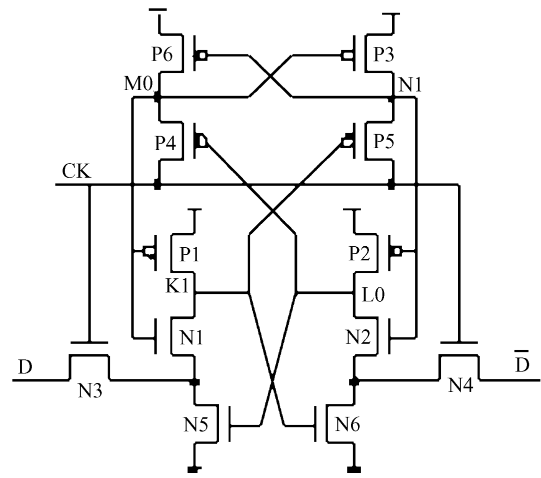


Fig.14 MBU upset map



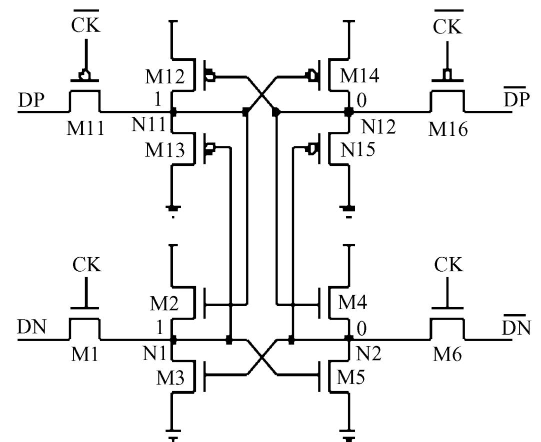


Fig.15 Other SEU hardened storage cells (a) HIT cell; (b) WHIT cell

much harder for an ion to upset a node several μms away than to directly upset a node for a certain time.

5 MNU in other SEU hardened SRAM

In a ROCK cell, Q' and the M node are both sensitive nodes, and the upset of Q will lead to the M node floating. We define these kinds of nodes as coupled sensitive nodes (CSN). Figure 15 shows other SEU hardened storage cells, most of which have CSN. Thus, they are also sensitive to multiple node upset. For example, an HIT cell is in the state of Fig. 15. An ion striking at the drain of P2 will upset the L node. Then, P4 is cut off, and the M node become impeding. Because of charge lateral diffuse, the drain of P6 will collect enough charge to upset. Finally, the whole cell upsets. In a ROCK cell and an HIT cell, the two transistors that collect charge are both pMOS, while in other cells the two transistors may be different. For example, one is pMOS and the other is nMOS in a DICE cell. In a DICE cell the lateral charge diffusion is not an important factor because it is difficult to dif-

fuse across two kinds of dropping Si. Under this condition, the bipolar charge collection becomes more important, which has been described in Ref. [9]. Whether the mechanism is lateral diffusion or bipolar collection, CSN will help upset the whole cell.

To migrate MNU, one must place the coupled sensitive nodes as far as possible from each other in the layout. In an HIT cell, for instance, P2 should be placed far from P4 and P6, and P1 should be placed far from P5 and P3. The other way is to design a cell without CSN. A WHIT cell (Whitaker presented in Ref. [3]) is such a cell. As shown in Fig. 15, sensitive nodes are N1 and N12. Suppose an ion strike at the drain of M3. N1 is upset immediately. The M5 will turn-off and the M13 will turn on. N2 is not a sensitive node. There will be no charge collection even if charge diffuses here. N11 will not upset, because M12 is stronger than M13. Charge diffused to the drain of M14 and M15 will be collected. But, because the charge density is much lower than that in the ion track, the induced transient current cannot overcome the complementary current from M15. So, N12 will not upset unless the ion energy is very large. In experiment, the LET_{th} of the WITH cell is 120MeV/mg/cm^2, much higher than other cells, which proves this explanation is correct. But, the high static current prevents WITH cells from being wildly used.

6 Conclusion

In this work, multiple node upset in SEU hardened cells by single ion strike is studied using a three-dimension device/circuit simulation. A device model containing two pMOSs is built, which is connected to different external circuits to study MNU under different conditions.

First, we compared single node charge collection and multiple node charge collection in a ROCK cell and showed that a ROCK cell will recover from a single node upset. Meanwhile it will upset when MNU occurs even if the two sensitive junctions are 7μm from each other. Thus, MNU may be a limitation on the scaling down of radiation hardened circuits. Charge diffusion and transient floating nodes were found to be the main factor for MNU. How long the node floats is also more important.

Next, we compared MNU in a ROCK cell with MBU of two independent SRAM cells. There was a great difference between them. The LET needed to upset the ROCK cell is much lower than that needed to upset two SRAM cells. The most sensitive area of the ROCK cell is one of the cut-off drains, while the sensitive area of MBU is in the middle of the two cut-off drains. The upset of one node in a ROCK cell causes another node to float. The floating node is sensitive to charge collection.

Other SEU hardened cells are also discussed. Most of them will produce transient floating nodes when one node is upset. Methods to avoid MNU are discussed. One way is to place the coupled sensitive node far from each other during layout. Another way is to avoid floating nodes by design. For example, a WHIT cell will not produce a floating node.

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SEU加固存储单元中的多节点翻转

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摘要：使用3D器件模拟了SEU加固单元的多节点翻转(multiple node upset,MNU)问题.结果表明瞬时悬空节点和电荷横向扩散是MNU的关键原因.对比了MNU和不同存储单元之间的MBU (multiple bit upset),发现它们之间的特点存在较大差异.最后讨论了避免MNU的方法.

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