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Mechanism of Reverse Snapback on *I-V* Characteristics of Power SITHs with Buried Gate Structure

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Abstract: The reverse snapback phenomena (RSP) on *I-V* characteristics of static induction thyristors (SITH) are physically researched. The *I-V* curves of the power SITH exhibit reverse snapback phenomena, and even turn to the conducting-state, when the anode voltage in the forward blocking-state is increased to a critical value. The RSP *I-V* characteristics of the power SITH are analyzed in terms of operating mechanism, double carrier injection effect, space charge effect, electron-hole plasma in the channel, and the variation in carrier lifetime. The reverse snapback mechanism is theoretically proposed and the mathematical expressions to calculate the voltage and current values at the snapback point are presented. The computing results are compared with the experiment values.

Key words: power static induction thyristor; reverse snapback; electron-hole plasma; lifetime; injection level
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1 Introduction

Power static induction thyristors (SITHs) are widely used in switching applications. SITHs frequently switch between the conducting-state and blocking-state. The dynamic state is the transition process from one steady state to another. SITHs have many advantages, including a small gate current required to turn it on, a high switching speed, a high sensitivity of conducting, a large capability for transient current and voltage (di/dt and dv/dt) with small waste, small power consumption, excellent thermal stability, large capacity of withstanding high voltage, and a high operating frequency. A profound understanding of the physical mechanism of the dynamic process is significant for the design and fabrication of satisfactory devices. In recent years, SITHs for high power applications have attracted many scientists' attention because of their excellent properties. Significant developments have been made. But, most researchers have been interested in the analytical model, device structure, numerical simulation, operating mechanism, and electrical characteristics in steady state[1~10]. However, investigation results show that the failure of devices often occurs neither in the conducting-state nor in the blocking-state, but in the dynamic state, i.e., the transition process between the two. Therefore, it is necessary to study the transient process from one steady state to another in physical nature. In this paper, the reverse snapback phenomena (RSP) of *I-V* characteristics of SITH are analyzed and discussed by taking account of the operating mechanism, double carrier injection effect, space charge effect, electron-hole plasma and conductance modulation in the channel, and the variation in carrier lifetime.

2 Fabrication processes

SITH is chiefly used as a switch in power electric systems. In order to satisfy the requirements of high frequency and high power, SITH must be able to block high voltage with a very small leakage current in the forward blocking-state, and to conduct a large current with a very low voltage drop in the conducting-state. To analyze reverse snapback phenomena of *I-V* characteristics, a power SITH has been fabricated with a buried-gate structure using a n-type Si single wafer with 80~100Ω·cm resistivity. Due to the high mobility of electrons, the saturation drift velocity of the electron is larger than that of the hole, thus the transit time of carriers in the channel of the SITH is much shorter, giving good frequency characteristics. The main technological processes for manufacturing SITHs with buried-gate structure have been described in detail in our previous paper[11].

3 Brief descriptions of device structure

Figure 1 shows the cross-section of a portion of

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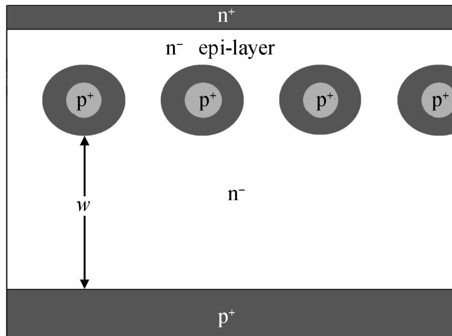
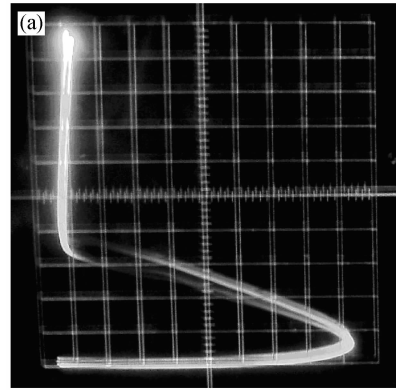


Fig.1 Schematic cross-section of SITH with buried gate

the SITH with a buried gate. In order to demonstrate the intrinsic reverse snapback properties of the SITH with buried-gate structure, the device is designed to be surrounded by a deep groove (not shown in the figure) to cut off the probable various parasitical effects that may degrade the device performance, especially to avoid the parasitical parallel-current effect. The space between the gate and p^+ anode of SITH is referred to as the high resistance drift region whose length is indicated with w in Fig. 1. The structure of the power SITH with buried gate can be considered as a forward biased anode diode controlled by a static induction transistor (SIT). The SIT operates as a switch to control the forward biased anode diode consisting of the anode (p^+) and the drift region (n^-). In the blocking state, although it is forwardly biased, the anode diode cannot inject holes into the drift region. When SIT works in the conducting state, the forward biased anode diode injects a large number of holes into the drift region (n^-). Under the high forward anode voltage, holes and electrons are injected into the drift region and the channel from the anode and the cathode, respectively. The accumulated electrons and holes establish high density plasma in the drift region and the channel, resulting in a rapid increase in channel conductivity. Therefore, the I-V curve displays the reverse snapback phenomenon. With a further increase in the forward anode voltage, the device ultimately turns to the conducting state.

SITH is working in the forward operating state when its anode diode is biased with high positive voltage V_A. When a positive gate voltage is biased ($V_{GK}>0$), SITH enters the forward conducting state and can conduct a large current with a very small voltage drop, as shown in Fig. 2 (a), similar to the characteristics of a thyristor. When a negative gate voltage is applied ($V_{GK}<0$), SITH turns to the forward blocking state and can withstand high voltage with a very small leakage current, as shown in Fig. 2 (b), exhibiting the triode-like characteristics of SIT. With an increase in anode voltage, the channel potential barrier



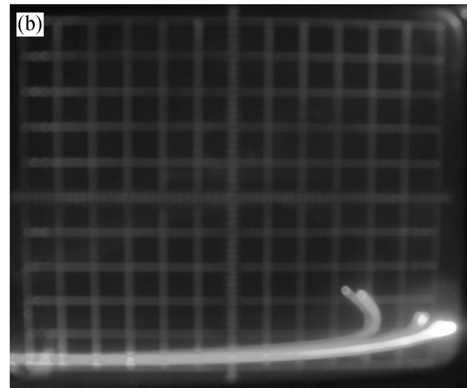


Fig.2 Reverse snapback characteristics of SITH (a) Positive gate voltage; (b) Negative gate voltage

gradually decreases. When the anode voltage V_A is increased to a critical value, the reverse snapback takes place in I-V characteristics, and switches the device permanently to the conducting state.

In SITH, the reverse snapback phenomenon appears in two situations. I-V characteristics of SIT display the reverse snapback under positive gate voltage in the forward conducting state. In the forward blocking state ($V_{GK}<0$), when the anode voltage is increased to a certain value, the reverse snapback takes place in I-V characteristics. The holes are injected from the gate into the channel under positive gate bias. Even if the anode positive voltage is low, the minority carrier holes also contribute to the conducting current, giving rise to reverse snapback analogous to the condition of a thyristor. Because the gate-channel pn junction of SITH is reversely biased by the negative gate voltage, only the electrons take part in the carrying current, exhibiting I-V characteristics of SIT in the small current realm.

4 Theoretical analyses

Suppose a single recombination center energy level is situated in the vicinity of the center of the forbidden band in the long drift region (n^-) of SITH, the recombination centers in the neutral long

drift region are filled with electrons, and the capture cross-section of electrons is much smaller than that of holes. The carrier lifetimes of silicon material are primarily dependent on the mechanisms of the phonon-assistant recombination of deep level, Auger, and radiation recombination. The carrier effective lifetime τ_{eff} can be written as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Aug}} \quad (1)$$

For the indirect gap semiconductor Si, the carrier effective lifetime τ_{eff} is mainly determined by the carrier lifetime τ_{SRH} due to the phonon-assistant recombination of deep level and the carrier lifetime τ_{Aug} dominated by the Auger recombination. The carrier Auger lifetime is expressed as:

$$\tau_{Aug} = \frac{1}{C_3(n_0^2 + 2n_0\Delta p + \Delta p^2)} \quad (2)$$

where n_0 and p_0 are the thermal-equilibrium concentrations, Δn and Δp are the injected excess electron and hole concentrations, and C_3 is the Auger recombination coefficient (about $3.4 \times 10^{-31} cm^6/s$ for silicon). Only Auger recombination must be taken into account for the heavily doped region and high-level injection. Because the drift region in power SITH is lightly doped, Auger recombination comes into effect evidently only when the electron injection level approaches or exceeds $10^{17} cm^{-3}$ if the hole lifetime under low injection is smaller than $10\mu s$.

The carrier lifetime due to the phonon-assistant recombination of deep level (τ_{SRH}) is given by

$$\tau_{SRH} = \frac{\tau_p(n_0 + n_1 + \Delta n) + \tau_n(p_0 + p_1 + \Delta p)}{p_0 + n_0 + \Delta n} \quad (3)$$

where the parameters n_1 and p_1 are defined as:

$$n_1 = n_i e^{(E_t - E_i)/kT} \quad (4)$$

$$p_1 = n_i e^{-(E_t - E_i)/kT} \quad (5)$$

respectively, and τ_n, τ_p are defined as:

$$\tau_p = \frac{1}{\sigma_p v_{th} N_t} \quad (6)$$

$$\tau_n = \frac{1}{\sigma_n v_{th} N_t} \quad (7)$$

where E_t is the energy level of the recombination center, σ_n and σ_p are the capture cross-sections of electron and hole, respectively, N_t is the effective concentration of the recombination centers, and v_{th} is the average thermal velocity of carriers, which is $7 \times 10^7 cm/s$ for silicon at room temperature.

The carrier lifetime (τ_{SRH}) determined by the indirect recombination is a function of the concentration of injected excess carriers, and it varies not only with the position of the recombination center level in the forbidden band, but also with the injection level ($\Delta p/n$), as shown in Table 1. The data in Table 1 are computed using $N_t = 10^{12} cm^{-3}$, $n_0 = 5\times10^{13} cm^{-3}$, $\sigma_n = 5\times10^{-15} cm^{-2}$, $\sigma_p = 5\times10^{-14} cm^{-2}$. With an increase in injection level, the carrier lifetime, determined by the recombination center level near the central line of the band-gap, increases. When the injected excess carrier concentration is comparable with the channel doping density, the minority lifetime is increased approximately by one order.

Table 1 Dependence of τ_{SRH} on $\Delta p/n$ near the central line of band-gap

$\Delta p/n$	0.01	0.1	1.0	10	100
τ_{SRH}/s	2.1×10^{-6}	3.8×10^{-6}	1.1×10^{-5}	2×10^{-5}	2.2×10^{-5}

With respect to the physical structure, a SITH may be considered as being composed of a SIT and a diode. The current in the channel of the SITH consists of an electron current injected from the cathode flowing through the drift region to the anode and hole current injected from the anode flowing into the cathode.

When a high negative voltage is applied to the gate, the high potential barrier in the channel of SIT prevents the holes from being injected from the anode and/or gate, and there are few electrons flowing through the channel. Thus, the current in this situation can be given by:

$$I_n \approx I_0 e^{\phi_{min}/V_T} \quad (8)$$

where I_0 is the saturation current, Φ_{min} is the saddle potential in the channel referred to as the intrinsic gate, and V_T is the thermal potential.

As the anode forward voltage continues to increase, the potential barrier in the channel of SIT is gradually reduced, and the electrons injected from the cathode and the holes injected from the anode continuously increase in number. Therefore, high density plasma of electrons and holes are formed in the channel and drift region, resulting in enhancement in channel conductance. As the lifetime of the minority carrier hole is short in low-level injection conditions, it is impossible for holes injected from the anode to pass the drift region and arrive at the cathode because of recombination with electrons.

With an increase in injection level or an enhancement in the anode electric field, the minority carrier lifetime extends sharply. The holes injected from the anode can transit the drift region and the channel to reach the cathode with enough high velocity. The more the holes are that injected from the anode, the more easily the minority carrier holes pass the drift region and reach the cathode. Due to the high-level injection, the current density in the device is very large and a very low anode voltage is required to easily complete the transition of holes from the anode through the drift region to the cathode. In the cathode region, a large number of electrons are injected

into the channel from the cathode, and the channel potential barrier decreases greatly and even vanishes. The entire drift region and channel become neutral, so a great mass of electrons and holes form high density plasma in this region. The strong conductance modulation effect takes place in the channel and drift region. At this point, the current flow in the SITH is very large, but the anode voltage of hundreds to more than one thousand volts suddenly decreases to the value of conducting-state voltage drop (2～3V), producing the reverse snapback characteristics.

Therefore, the reverse snapback characteristics are caused by the continuous increase in the excess minority carrier hole lifetime as the injection level increases, eventually resulting in the injected minority holes having an adequately high velocity to transit the drift region and reach the cathode. As demonstrated in Table 1, in order to prolong the lifetime of the minority carriers, the injected excess carrier concentration must be comparable with the doping concentration of substrate. For the occurrence of reverse snapback phenomena, it is reasonable to assume the concentration of injected holes to be equal to the doping concentration (N_D) of the drift region. In the drift region near the anode end, this relation can be written as: $p_A = N_D$. To maintain the electrical neutrality, the electron concentration is $n \approx 2N_D$ in this region. Assuming that the electric field is E, then the anode current can be expressed as:

$$I_A = qA(2\mu_n + \mu_p)N_D E \qquad (9)$$

In order for the holes injected from the anode to cross the drift region and reach the vicinity of the cathode, the lifetime of holes τ_p must be larger than the transition time.

$$\tau_p \geqslant t_p = \frac{w}{\overline{v_p}} = \frac{w}{\mu_p \overline{E}} \qquad (10)$$

where $\overline{v_p}$ is the average drift velocity of holes, w is the length of the drift region, t_p is the transit time of holes, and μ_p is the hole mobility. In low electric fields, the drift velocity can be V_p can be approximately given by $V_p = \mu_p E$. At the beginning of the reverse snapback, while the injected holes can reach the anode through the drift region, the channel current is mainly conducted by the electrons. Using Eqs. (8), (9), and (10), the snapback electric field can be expressed as:

$$\phi_{min} \approx -V_T \ln\left(\frac{I_0 L_p^2}{qA(2\mu_n + \mu_p)N_D w}\right) \qquad (11)$$

Suppose that the carriers pass through the channel potential barrier in the diffusion manner, the saturated current I_0 may be written as:

$$I_0 \approx qA_{eff} D_n \frac{N_s}{w_{sad}} = qA_{eff}\mu_n V_T \frac{N_s}{w_{sad}} \qquad (12)$$

where A_{eff} is the effective cross section of the channel, N_S is the doping concentration in the cathode region, and w_{sad} is the distance between the cathode and the intrinsic gate (saddle point).

The intrinsic gate potential is given by:

$$\phi_{min} = \eta\left(V_G + \frac{1}{\mu}V_A\right) \qquad (13)$$

where η is the gate efficiency, and μ is the voltage amplification coefficient.

Substituting Eqs. (12) and (13) into Eq. (11) yields

$$V_{SB} = \mu\,|V_G| - V_T \frac{\mu}{\eta}\ln\left(\frac{\mu_n}{2\mu_n + \mu_p} \times \frac{N_s}{N_D} \times \frac{L_p^2}{w w_{sad}} \times \frac{A_{eff}}{A}\right) \qquad (14)$$

This equation is the mathematical expression for computing the voltage at which the reverse snapback occurs. The corresponding mathematical expression for calculating snapback current can be derived from Eqs. (9) and (10):

$$I_{SB} = qAN_D \times \frac{2\mu_n + \mu_p}{\mu_p} \times \frac{w}{\tau_p} \qquad (15)$$

The coefficients $\mu_n/(2\mu_n + \mu_p)$ and $(2\mu_n + \mu_p)/\mu_p$ in Eqs. (14) and (15) are derived by assuming that the concentration of holes injected from the anode is equal to the doping concentration in the drift region at the point at which the reverse snapback takes place. Letting $\alpha_1 = \mu_n/(2\mu_n + \mu_p)$, $\alpha_2 = (2\mu_n + \mu_p)/\mu_p$, the two equations above can be written as:

$$V_{SB} = \mu\,|V_G| - V_T \frac{\mu}{\eta}\ln\left(\alpha_1 \times \frac{N_s}{N_D} \times \frac{L_p^2}{w w_{sad}} \times \frac{A_{eff}}{A}\right) \qquad (16)$$

$$I_{SB} = qAN_D\alpha_2 \times \frac{w}{\tau_p} \qquad (17)$$

When the gate is biased with a very low negative voltage, the drift region is not completely depleted until the reverse snapback occurs. Before the SBP appears on *I-V* characteristics, the positive bias degree of the pn junction between anode and drift region is enhanced with the increase in anode voltage and some holes are injected into the neutral drift region. When penetrating the neutral drift region in low electric field, the injected holes recombine with large numbers of electrons, and the hole current injected from the anode is converted into electron current through recombination. If only the anode voltage is increased to a critical value, the established electric field in the neutral drift region is high enough to allow holes to penetrate the neutral region and reach the border of depletion region. Then, the holes are driven towards the cathode by the continuously increasing electric field in the depletion region. If the amount of holes that can reach the proximity of the cathode once is sufficiently large, a positive feedback process will oc-

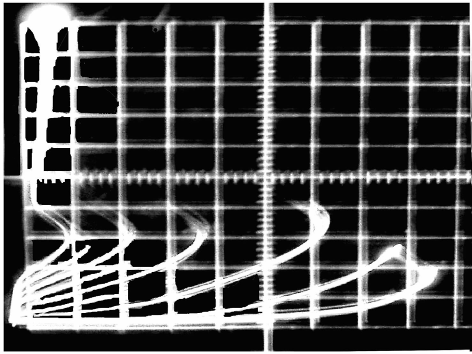


Fig.3 Reverse snapback *I-V* characteristics for different gate voltages

cur, and eventually the reverse snapback phenomena will exhibit *I-V* characteristics. The mathematic analysis procedure and expressions in this situation are similar to the previous case of high negative gate bias.

5 Conclusion and discussion

The reverse snapback phenomena (RSP) of *I-V* characteristics mainly results from two factors. In the physical structure, RSP originates from the positively biased p^+-n junction between the anode and drift region, which makes it possible for the holes to participate in conduction, resulting in the depletion region collecting external current components. In the carrier transmission, with an increase in anode voltage, the injection level of holes from the anode increases and the lifetime of the minority carrier holes continues to extend. Finally, the injected holes having sufficiently long lifetimes can cross the drift region and reach the cathode, realizing complete traverse of holes from the anode to cathode. The accumulation of holes near the cathode increases the positive bias of the n^+-n^- junction and accelerates the injection of more electrons and holes into the depleted drift region. The lightly doped drift region and the channel are filled with high concentration electron-hole plasma established by holes injected from the anode and the high density electrons, resulting in a heavy conductance modulation. The relevant physical process is the double injection limited by the space charge effect under high-injection and the recombination effect. The common effects of many other physical factors such as electrical neutralization, variation in minority carrier lifetime, change in mobility with injection level, and, especially, conductance modulation, result in the shrinkage of the depletion layer and a reduction in the voltage drop across this region. Finally, the reverse snapback process is accomplished in SITH, turning to the conducting-state in the end.

The voltage at which the reverse snapback occurs is dependent on the gate voltage. The higher the gate voltage is, the higher the snapback voltage. But the current value at the snapback point, called the snapback current, does not depend on the gate voltage. The experimental observations, shown in Fig. 3, clearly demonstrate that the snapback voltage is linearly dependent on the gate voltage in the small voltage realm. The experimental results agree well with the value calculated using the mathematical equations represented in this paper. As the voltage amplification coefficient is a function of both the anode and the gate voltages, the dependence of snapback voltage on the gate bias deviates from the linear relationship in the regions of high anode and gate voltages. As the gate voltage is negatively increased, the snapback current is slightly reduced.

The more heavily doped the cathode region is, the more easily the reverse snapback appears. As the doping concentration of the cathode region is increased, the snapback voltage decreases, with a small variation in snapback current. Furthermore, the more heavily doped the drift region is, the more difficult the formation of high-level injection of holes is, and the higher the corresponding snapback voltage is. With an increase in doping concentration in the drift region, the snapback voltage and current are raised. The snapback voltage and current are dependent on the diffusion length or minority carrier lifetime. The longer the diffusion length is, the higher the minority carrier lifetime and the lower the snapback voltage are.

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埋栅型电力静电感应晶闸管的 *I-V* 特性反向转折机理

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摘要： 研究了静电感应晶闸管的反向转折特性. 当工作在正向阻断态的阳极电压增大到某一临界值时，静电感应晶闸管的 *I-V* 曲线呈现出反向转折特性，甚至转向导通态. 在综合考虑了工作机理、双注入效应、空间电荷效应、沟道中的电子-空穴等离子体和载流子寿命变化的基础上分析了静电感应晶闸管的反向转折特性. 首次给出了反向转折机理的理论解释，并给出了估算转折电压和电流的数学表达式，在常用工艺参数范围内，计算结果和实验测量值基本一致.

关键词： 电力静电感应晶闸管；反向转折；电子-空穴等离子体；寿命；注入水平

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