A 0.18μm Transmitter and Receiver with High Speed and Low Power*

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Abstract: This paper describes the design of a low voltage differential signal (LVDS) transmitter and receiver with high speed and low power for CPU, LCD, FPGA, and other fast links. In the proposed transmitter, a stable reference and a common mode feedback circuit are integrated into the LVDS drivers, which enable the transmitter to tolerate variations of process, temperature, and supply voltage. The proposed receiver implements a rail-to-rail amplifier architecture that allows a 1.6Gb/s transmission. The transmitter and receiver are implemented in HJ TC 3.3V, 0.18μm CMOS technology. The experimental results demonstrate that the transmitter and receiver reach 1.6Gb/s. The transmitter and receiver pad cells exhibit a power consumption of 35 and 6mW, respectively.

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1 Introduction

The increasing demand for data bandwidth in networking has driven the development of high-speed links. Optical fibers are costly and area inefficient for these distances. Thus, low-cost, high-speed parallel links and serial links using copper cables are an attractive solution for such applications[1~3].

There are three primary components in a link: the transmitter, the channel, and the receiver. The transmitter converts a digital data sequence into an analog signal in the channel; The channel is the transmission path along which the signal travels; And the receiver converts the received analog signal back to a digital data sequence.

Conventionally, LVDS are designed with GaAs or Si bipolar devices because of their high-speed characteristics. However, GaAs devices are difficult to integrate when solving the problem of high-density logics. BiCMOS solves the problem of technology integration with high-density logics. But performance optimization between bipolar transistors and CMOS transistors is difficult. As the CMOS technology has progressed into deep-submicron regions, CMOS devices have the ability to realize gigahertz operation chips.

LVDS is a transmission technique used in computer systems to transmit data at high speed with low power dissipation. LVDS uses differential data transmission and the transmitter is configured as a switched-polarity current generator. A differential load resistor at the receiver end provides current-to-voltage conversion and optimum line matching at the same time[4,5].

LVDS achieves significant power savings by means of a differential scheme for transmission and termination, in conjunction with a low voltage swing. LVDS standards pose relatively stringent requirements on the tolerance affecting the output levels, raising interesting design issues if low-cost solutions with neither external components nor trimming procedures are required[6].

Previously published transmitters have a power dissipation of about 28~35mW/Gb/s and the receivers have a power dissipation of about 9 ~ 27mW/Gb/s. Boni *et al*.[7] proposed a 1.2Gb/s LVDS IO in 0.35μm CMOS technology. Its transmitter and receiver cells exhibit a power consumption of 43 and 33mW, respectively. Mandal *et al*.[8] proposed a 1.3Gb/s receiver in 0.13μm CMOS technology and its power dissipation is 11mW.

In this paper, the transmitter and receiver reach 1.6Gb/s, and the power dissipation is 22 and 4mW/(Gb/s), respectively. In our transmitter, an accurate bias produces an accurate current for the LVDS differential driver. Therefore, a lower voltage swing compared with other designs helps consume less power. In our receiver, a rail-to-rail amplifier accommodates a wider input range and the self-biased compa-

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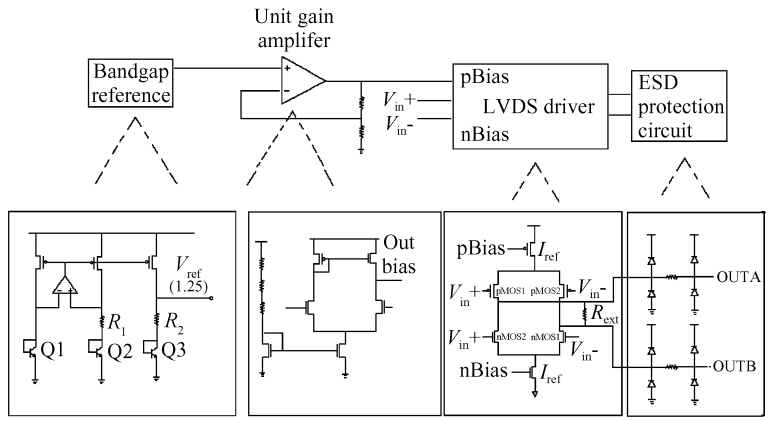

Fig. 1　LVDS transmitter architecture

rator similar to digital comparators has less power than other analog designs.

2　LVDS transmitter

Figure 1 shows the LVDS driver architecture. The core circuit is the LVDS differential output buffer, and the LVDS buffer behaves as a current source with switched polarity. The output current flows through the load resistance, establishing the correct differential output voltage swing.

The operation of the switchable current sources is explained as follows. If $V_{in}+$ is low and $V_{in}-$ is high, then switch pMOS1 and nMOS1 are ON and switch pMOS2 and nMOS2 are OFF. pMOS1 and nMOS1 conduct current I_{ref} and pMOS2 and nMOS2 are OFF. The current I_{ref} flows through the termination resistors and produces the signal swing.

Process, voltage, and temperature (PVT) variations will affect the output swing, the data frequency, and the jitter. In order to maintain the output stability of the LVDS driver, we design three other circuits: a bias circuit without the changes of the PVT as the standard reference, a circuit generating the bias for the LVDS driver current sources, and a common mode feedback circuit to hold the output common mode voltage stable. The three parts of circuits are described below.

First, the bias circuit ensures the LVDS buffers generate controlled current and controlled voltages through and across the load resistance over all PVT conditions. The reference circuit must provide a constant bias voltage, independent of variations in power supply. We designed a bandgap reference circuit without changing the PVT. From Eq. (1), the bandgap reference voltage is 1.25 in Fig. 1. Based on the constant reference voltage, a pMOS bias and nMOS bias reference voltage are generated.

$$V_{ref} = V_{BE} + \frac{R_2}{R_1} V_T \ln n \tag{1}$$

Second, the unity gain amplifier generates a reference voltage to bias the LVDS buffer. The pMOS bias value is decided by the I_{ref}, and the I_{ref} value is calculated on the output swing. Equation (2) describes the I_{ref} value.

$$I_{ref} = \frac{V_{high} - V_{low}}{R_{ext}} \tag{2}$$

where V_{high} is the output high level and V_{low} is the low level voltage of the swing. R_{ext} is the match resistor of the transmission. The transmission line impedance is 50Ω. Therefore, the external differential impedance R_{ext} is 100Ω.

Third, for a high speed transmit system, the output common mode voltage is important to the receiver. In order to achieve higher precision and lower circuit complexity, a simple low-power common-mode feedback (CMFB) control was implemented in the transmitter. Figure 2 shows the CMFB circuit strength and the stability of the common mode output voltage. One input to the amplifier in Fig. 2 is connected to the reference voltage generated by the bandgap and the other input gets the output offset voltage feedback through the middle of the output 100Ω resistors. So, the amplifier will retain an output common mode voltage equal to V_{ref}.

The ESD protection circuits are shown in Fig. 1. The ESD circuits are composed of diode transistors. The diode ESD devices have smaller capacitances than the pad, which is fit to increase the bandwidth of the transmission channel.

Furthermore, for the power of the LVDS transmitter, the circuit has low current. Including all bias stages, the total quiescent current in this circuit is less than 2mA and the output drive current I_{ref} is about 7mA .

In spite of the simplicity of the implemented control circuit, Monte Carlo simulations (process and

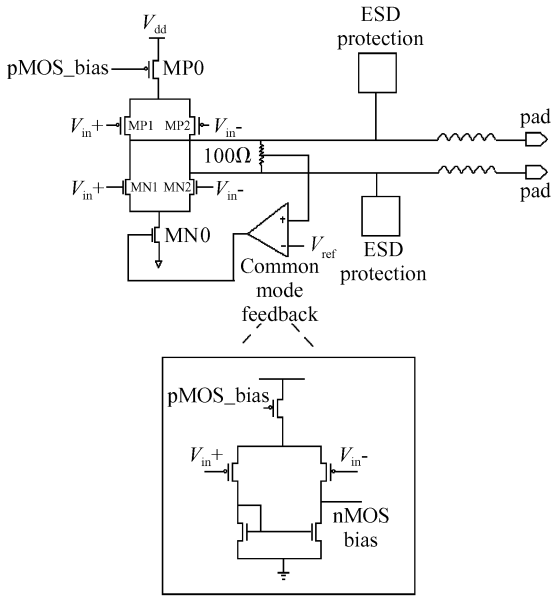

Fig. 2 LVDS driver with common mode feedback circuit

mismatch level) at different supply voltages and temperatures demonstrate that both the output swing and the common-mode voltage are within the allowed LVDS tolerance for more than 90% of the simulation runs.

To calculate the bit error rate, the LVDS driver starts with a 20bit pseudo random bit sequence (PRBS). The eye diagram of output random data signals are simulated by the cadence spectra in Fig. 3. The amplitude of the differential signals reaches 350mV. The common mode voltage is 1.2 and is stable in all periods. The output power of the LVDS buffer is about 28mW, which is sufficient to drive the differential signals to the receiver chip.

3 Rail-to-rail receiver

Practically, the receiver acts as a comparator, taking the voltage difference of the driver and returning "1" if this difference is positive and "0" otherwise[9]. Figure 4 shows the structure of the receiver.

To avoid reflections, the differential impedance

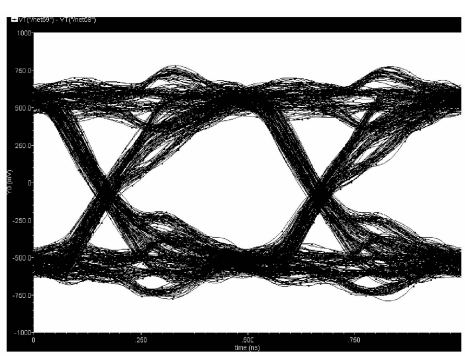

Fig. 3 Eye diagram of the output differential random data

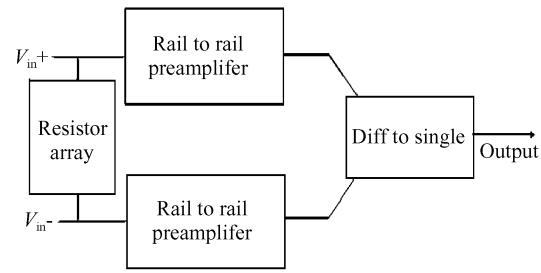

Fig. 4 Architecture of the receiver

of the receiver and its external termination resistor should equal 100Ω. The resistors array generates an accurate value of the 100Ω resistor in Fig. 4.

The common mode voltage level of the differential signals is important to the receiver. Thus, a wide range of input common mode is covered by simultaneously keeping an almost constant receiver dynamic response. So, a fully differential rail-to-rail input preamplifier was used for accommodating the LVDS input range, as shown in Fig. 5.

The proposed couple of pre-amplifiers work properly in a wide common mode voltage range from $V_{SS}+0.3$V to $V_{DD}-0.3$V. The rail-to-rail preamplifiers are important to the transmission system. For proper function, a linear transfer between the p- and n-stages in accordance with the operating region has to be achieved. In fact, the receiver must have more sensitivity to realize long distance and high speed transmission applications. The input amplitude of the receiver is between 250 and 600mV, the gain of the rail-to-rail pre-amplifier is about 40dB, and its bandwidth is more than 4Gb/s. Therefore, the receiver can transform the attenuate differential signal from the long channel to the high swing signals into the chip.

In the proposed receiver shown in Fig. 5, a comparator transfers the analog signals to digital signals. We used a self-biased open loop comparator to reach the function. This comparator can transfer the differential signals to a single signal quickly because of its

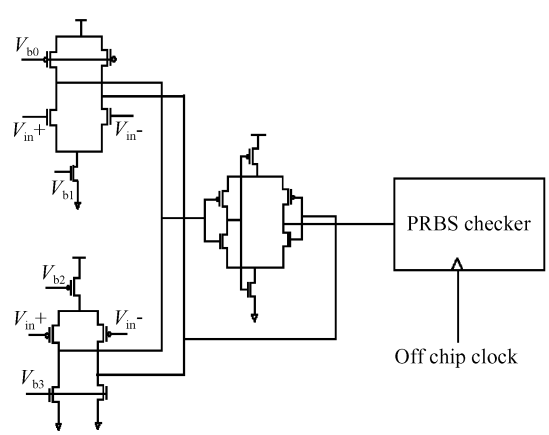

Fig. 5 Rail-to-rail amplifiers in the receiver

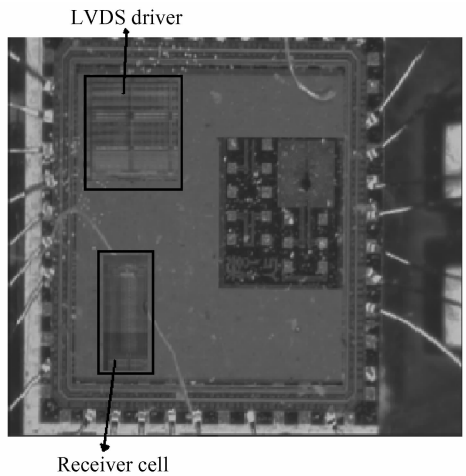

Fig.6　LVDS driver and rail-to-rail receiver chip micro photo

wide bandwidth. Furthermore, the structure of the self biased comparator consumes low power.

The receiver contains the corresponding bit error rate (BER) checking circuits. Because no clock is sent out from the LVDS driver, the data of the receiver are synchronized by the off-chip clock. We can put an off-chip clock into the chip to sample the data and check the BER.

4　Experimental results

A test chip of the LVDS I/O cells with an ESD circuit was designed and fabricated in HJ 0.18μm technology. Figure 6 shows that the LVDS transmitter and receiver cell are on the opposite side of the chip, which transfer the signal from one chip to another chip during the chip measurement. The chip area is 2mm × 2mm.

Figure 7 shows a two layer PCB (printed circuit board) 60cm long and with a 50Ω strip line designed to test the transmission. Two chips are embedded in the board and communicate with each other. The "zigzag" differential lines of about 70cm long are designed in the board to measure whether they can work properly over a long distance.

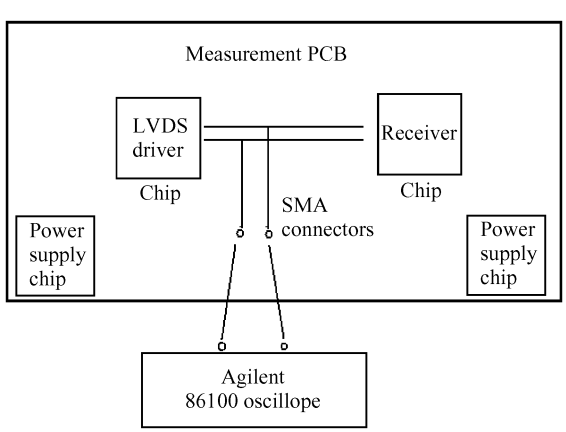

Fig.7　Measurement of chip on the PCB

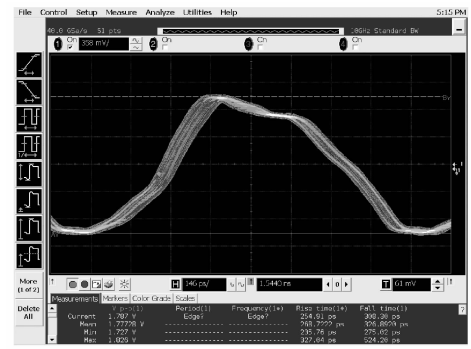

Fig.8　Jitter waveform of the oscilloscope at 1.6Gb/s

Table 1　Typical parameters of the transmitter and receiver

Parameter	Transmitter	Receiver
Area	400μm×600μm	300μm×600μm
Speed	1.6Gb/s	1.6Gb/s
Swing	350mV@CM 1.2V	
Power	35mW @1.6Gb	6mW@1.6Gb
BER		$<10^{-12}$
Sensitivity		Receive minimum differential signals: 250mV Gain:40dB BW:4Gb
Jitter	50ps	
Working distance	>1m	

Table 2　Typical parameters in previous paper

Parameter	Transmitter	Receiver
Ref.[7]	43mW	35mW
Ref.[8]		11mW

To the transmitter, the output data frequency and jitter can be measured by the oscilloscope. The Agilent 86100 oscilloscope can observe the waveform and generate the eye diagram of the random output data. Figure 8 shows that the output differential signals work to 1.6Gb/s and the output jitter is less than 50ps.

Synchronous testing (transmitter and receiver with different clock resources) shows the receiver operates normally and no error is detected for hours when we observe the output error of the PRBS checker.

Table 1 reports a performance summary of the implemented pad cells. Table 2 reports the power dissipation of previous LVDS IO designs.

5　Conclusion

In this paper, we designed a 1.6Gb/s LVDS driver and a rail-to-rail receiver in 0.18μm technology. Measurements of chips on the board are in good

agreement with simulation. The measurement and simulation results show the LVDS transmitter has low jitter, and the transmitter and receiver consume less power than many previous designs. The receiver has good sensitivity to the differential signals. Therefore, the structure of the transmission system can be used to obtain high speed and a long distance channel.

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一个 0.18μm 高速低功耗的发送和接收电路*

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摘要: 提出了一种高速低功耗的低压差分接口电路, 它可以应用于 CPU, LCD, FPGA 等需要高速接口的芯片中. 在发送端, 一个稳定的参考电压和共模反馈电路被应用于低压差分电路中, 它使得发送端能够克服电源、温度以及工艺引起的波形变化. 在接收端采用了轨到轨的放大器结构, 它可以工作到 1.6Gb/s. 芯片设计加工采用的是 0.18μm CMOS 工艺, 芯片测试结果表明, 整个发送接收端数据传输速率可以达到 1.6Gb/s, 同时发送和接收端的功耗分别是 35 和 6mW.

关键词: 低压差分信号; 轨到轨; 低功耗

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