A Novel All-pMOS AC to DC Charge Pump with High Efficiency

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Abstract: A novel AC to DC charge pump with high performance is presented. Due to the pMOS structure and threshold voltage canceling technology, the efficiency and the output voltage are greatly improved. Test results show that the output voltage and power efficiency are improved by 125% and 104% respectively at 13.56MHz for a 1V sinusoidal input compared to the traditional MOS diodes structure.

Key words: rectifier; charge pump; high efficiency
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1 Introduction

A typical AC to DC charge pump (CP) is comprised of a capacitor-diode network. MOSFET diodes are often employed in CMOS technology[1]. There are two drawbacks in this circuit: the output voltage saturates as stages increase due to the body effect and it is difficult to achieve high efficiency.

This paper presents a novel all pMOS charge pump that eliminates the threshold voltage loss of the MOS diode. Furthermore, a threshold voltage canceling technology is employed to further improve the output voltage and power efficiency. The proposed charge pump employs only standard MOS transistors and capacitors is a superior solution when low threshold or zero threshold transistors are not available.

2 Analysis of all pMOS CP circuit

Figure 1 shows the traditional charge pump, which employs nMOS diodes. When a sinusoid signal is applied at V_{in}, DC voltages will be generated on the capacitors and the voltage will rise stage by stage. Thus, compared to the amplitude of the input, a much higher voltage can be acquired at V_{out}.

Figure 2 shows the proposed charge pump and Figure 3 show the structure of a CP cell. M1 is the charge transfer transistor. Two auxiliary MOSFETs, M2 and M3, are introduced to update the body voltage of M1[2]. In this way, the body of M1 is always connected to the higher voltage of V_{in} and V_{out}. In other words, the threshold voltage of M1 is a constant (V_{T0}) since its body is always connected to the source.

An analytical expression for the charge pump output voltage is given below[1],

$$V_{out} = n\Delta V = n(V_{in} - V_{drop}) \quad (1)$$

where n is the number of CP stages, V_{out} is the output voltage, and V_{in} is the amplitude of the input. V_{drop} is the voltage drop on the charge transfer transistors.

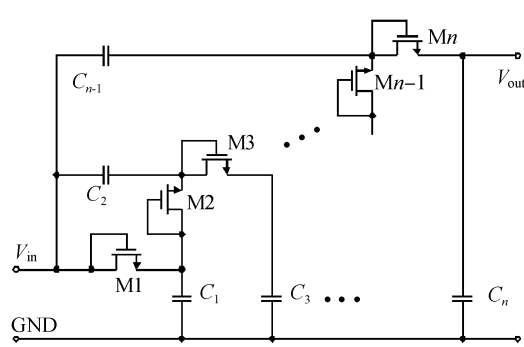

Fig. 1 CP with MOS diodes

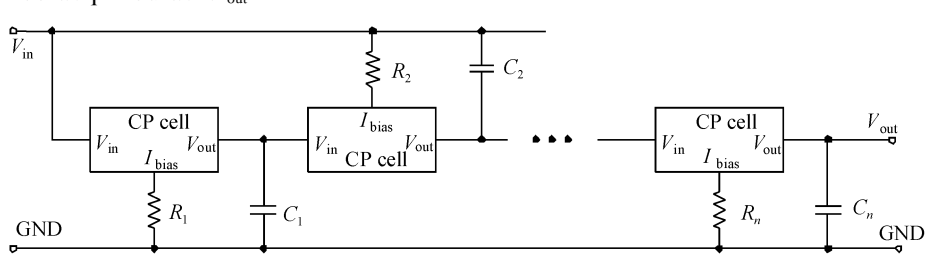

Fig. 2 Structure of proposed CP

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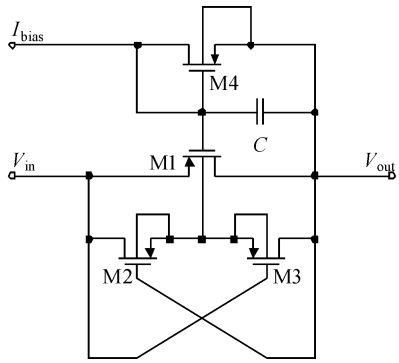

Fig. 3　Charge pump cell

For the charge pump in Fig. 1, we have

$$V_{drop} = \sqrt{2I_{DS}/\beta} + V_T \tag{2}$$

where $V_T = V_{T0} + \gamma(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|})$ is the threshold voltage of the MOS diode. $\beta = \mu_p C_{ox}$ is the technical transmit parameter, and I_{DS} is the current of the MOS diode.

For the proposed charge pump shown in Fig. 3, a voltage of V_{T0} (without body effect) is generated between the source and gate of M4, in other words, on C as M4 is biased with a very small current.

Thus, M1 turns on at the moment when $V_{in} > V_{out}$ since V_{GS1} is more than V_{T0}. For the proposed charge pump, the V_{drop} can be expressed as,

$$V_{drop} \approx \sqrt{2I_{DS}/\beta} \tag{3}$$

If I_{DS} is a very small current or transistors of large size are applied, the voltage drop can be rather small and a much higher voltage without saturation can acquired at the output.

The charge pump conversion efficiency is defined as

$$\eta = P_{out}/P_{in} = 1 - P_{loss}/P_{in} \tag{4}$$

where P_{in}, P_{out}, and P_{loss} are the input power, output power, and circuit power loss, respectively.

The voltage drop and current of every stage of the charge pump is time variable. It is difficult to acquire an accurate mathematical expression for the power loss and it is also unnecessary. The power loss of every stage can be approximated as

$$P_{loss,stage} \approx V_{drop} I_{avg} = V_{drop} I_{out} \tag{5}$$

where I_{avg} and I_{out} are the average current and output current, respectively. For the proposed charge pump, thanks to its much lower voltage drop (close to zero), the efficiency is greatly improved with the same output current.

3　Simulation and test results

3.1　Simulation results

Figures 4 and 5 show the simulation results comparing the MOS charge pump[1] with the proposed all-pMOS charge pump. All the simulations are carried out at 13.56MHz with SMIC 0.18μm RF technology. The load is a resistor of 100kΩ parallels with a capacitor of 60pF to stabilize the voltage.

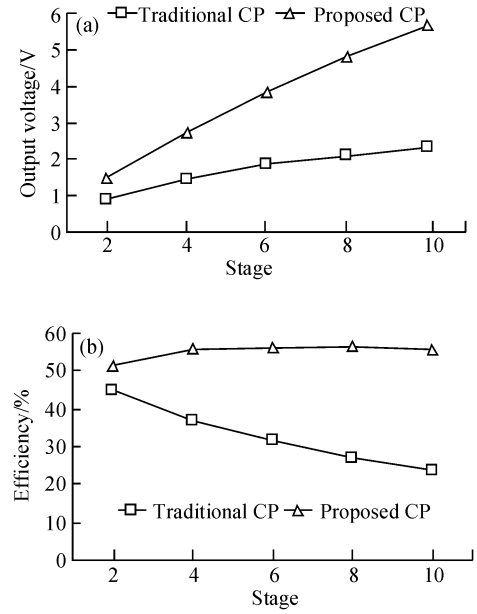

Fig. 4　Output voltage (a) & efficiency (b) versus stages

For a constant input of 1V, the results of output voltage and efficiency versus stages are given in Fig. 4. The output voltage of the proposed charge pump rises almost linearly while the efficiency stays above 50%. The proposed structure is even more attractive for large stage numbers. However, large bias resistors need to be employed as the voltage rises stage by stage, increasing the area occupied dramatically. A few stages will meet the needs of most cases.

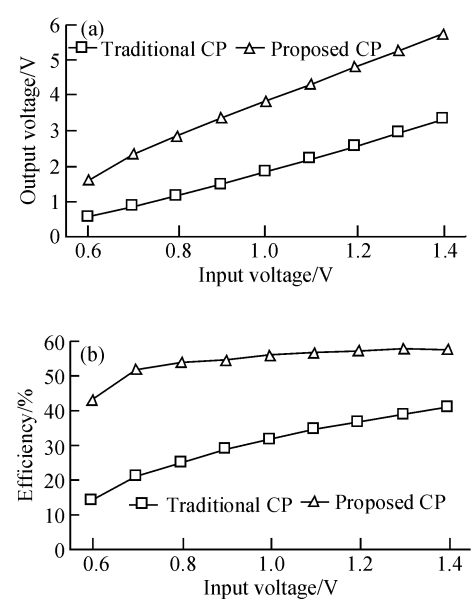

Fig. 5　Output voltage & efficiency versus input voltage

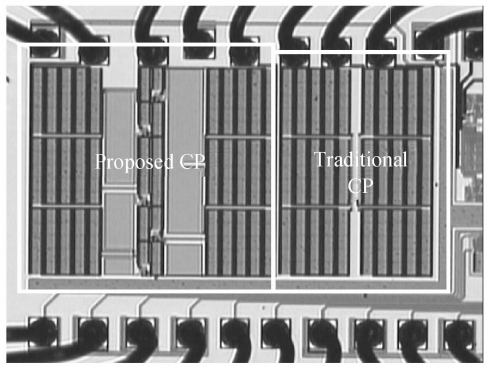

Fig. 6 Layout of traditional CP and proposed CP

For charge pumps with 6 stages, the results for the output voltage and efficiency versus input amplitude are given in Fig. 5. The proposed structure is suitable for low-input applications. It generates higher output voltage and achieves better power efficiency.

3.2 Test results

To verify the simulation, two charge pumps of 6 stages are implemented in SMIC 0.18μm 1P6M mixed-mode CMOS technology, as shown in Fig. 6,

The area of the proposed CP is 600μm by 600μm, which occupies about 30% more than the traditional CP. The test results for output voltage and efficiency versus input amplitude are shown in Table. 1.

The output voltage is very close to the simulation results in Fig. 6. The efficiency of both charge pumps is not as high as the simulation and the results may be not accurate due to the test conditions. However, the proposed CP achieves much better performance than the traditional one.

Table 1 Output voltage & efficiency versus input voltage

Input /V	Output of traditional CP /V	Output of proposed CP /V	Efficiency of traditional CP /%	Efficiency of proposed CP /%
0.7	0.65	2.0	14	34
0.8	1.0	2.6	17	37
0.9	1.3	3.1	17	36
1.0	1.6	3.6	21	43
1.1	1.9	4.2	26	38
1.2	2.2	4.6	27	40
1.3	2.5	5.1	29	39

4 Conclusion

A high efficiency AC to DC charge pump has been designed for RFID applications based on 0.18μm CMOS technology. Simulation and testing results show that this circuit generates higher voltage than the conventional CP structure with the same stage number. Furthermore, the power efficiency is greatly improved, which makes it attractive for low-voltage and low-power applications.

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一种高效率全 pMOS 结构 AC-DC 电荷泵

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摘要：介绍一种全新高性能的 AC-DC 电荷泵. 它采用全 pMOS 的结构和阈值电压消除技术，使得其效率和输出电压都大幅度的改善. 测试结果表明在 13.56MHz 和 1V 的输入条件下，相对于传统的 MOS 二极管结构，这种全 pMOS 电荷泵的效率提高了 104%，而输出电压获得 125%的提升.

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