Fabrication of Silicon Crystal-Facet-Dependent Nanostructures by Electron-Beam Lithography*

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Abstract: Silicon crystal-facet-dependent nanostructures have been successfully fabricated on a (100)-oriented silicon-on-insulator wafer using electron-beam lithography and the silicon anisotropic wet etching technique. This technique takes advantage of the large difference in etching properties for different crystallographic planes in alkaline solution. The minimum size of the trapezoidal top for those Si nanostructures can be reduced to less than 10nm. Scanning electron microscopy (SEM) and atomic force microscopy (AFM) observations indicate that the etched nanostructures have controllable shapes and smooth surfaces.

Key words: silicon nanostructure; anisotropic wet etching; electron-beam lithography
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1 Introduction

The technology for silicon nanofabrication is important for silicon quantum effect devices because clear quantum effects at room temperature can be observed within the sub-10nm scale[1]. In addition, the fluctuation of nanostructure surfaces should be minimized in order to avoid the disturbance to the quantum effect. Electron-beam lithography is an effective technique for pattern transfer in the nanometer scale. As far as silicon etching is concerned, the roughness of the silicon nanostructures surface etched by dry etching cannot be ignored because it has significant influence on the device's characteristics. However, good results can be obtained with anisotropic wet etching in an alkaline solution. The anisotropic wet etching technique takes advantage of the fact that the etching rate of the Si {111} plane is much slower than that of other planes[2]. The roughness of the silicon surface etched by an alkaline solution with a regulator can be as low as 6nm under appropriate etching conditions[3].

In recent years, electron-beam lithography and anisotropic wet etching have been used for fabricating nanostructures on (110) and (100) Si-based substrates. Kurihara *et al*. fabricated sub-10nm Si lines on the Si (110) substrate by the shifted mask pattern method, which used two shifted mask patterns to reduce the width of Si lines[4]. The etched surface was bound by the slow etching rate of the Si (111) planes perpendicular to the (110) substrate. Namatsu *et al*. fabricated 2nm-wide Si lines using the same method[5]. Step-like characteristics in the conductance curve were clearly observed when this structure was applied as an electronic transport channel. Pennelli *et al*. fabricated a device with a similar Si-line structure on the (110) silicon wafer with (111) sidewalls perpendicular to the substrate. The Si-line structure with a width of 15nm separates the source and drain, providing a tunneling barrier between these two contacts[6]. This research group fabricated another type of nanostructure on (100)-oriented silicon-on-insulator (SOI) substrate that was composed of a small silicon island connected to the leads by the channels with triangular cross-section. The I_{DS}-V_{DS} characteristic of that nanostructure exhibits a step-like behavior at room temperature[7].

The structures fabricated by anisotropic wet etching on (100)-oriented substrate generally have a trapezoidal/triangular cross-section[2], which offers more controllability for dimension reduction in the application of quantum effect devices[8]. Hiramoto *et al*. fabricated Si nanostructures including silicon nanowire, a cross-shaped structure, and a T-shaped structure on the (100)-oriented SOI substrate. These nanostructures were fabricated using two anisotropic etching steps and one selective oxidation step. The

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minimum size of the trapezoidal top for those Si nanostructures was about 10nm[9]. Ishikuro and Hiramoto fabricated silicon single-electron transistors in the form of point contact MOSFETs on the (100)-oriented SOI substrate. The point-contact structure is defined by two groups of intersectant (111) crystal facets. This device with an extremely narrow channel showed Coulomb blockade oscillations at room temperature and negative differential conductance at low temperatures[10].

To realize good controllability of the shape of nanostructures, it is necessary to elaborately design the pattern of the mask according to the prosperities of anisotropic wet etching. In our work, silicon crystal-facet-dependent nanostructures, including silicon point-contact structure, half-circle island and elliptical island, have been successfully fabricated on a (100)-oriented silicon-on-insulator wafer using electron-beam lithography and the silicon anisotropic wet etching technique. Those etched nanostructures are constructed by a group of smooth crystal facets on {133}, {313}, and {111} planes during anisotropic etching. The fixed orientation and angle of crystal facets can rectify the distortion of mask film system such as the proximity effect on resist mask and the isotropic lateral etching for oxide mask. Therefore, silicon crystal-facet-dependent nanostructures are reproducible and self-rectified.

2 Experiment

Silicon nanostructures were fabricated on a p-doped {100} separation-by-implanted-oxygen (SIMOX) wafer that consisted of an 80nm-thick top silicon layer insulated from the silicon substrate by a buried 300nm-thick SiO_2 layer. A 30-nm thick SiO_2 layer grown by means of thermal oxidation at 875℃ was used as a mask. A layer of poly-methyl methacrylate (PMMA) resist (AR-P679.04, 950k Mw, 4.0% in ethyl lactate) was spin-coated onto the surface of the SOI chip with a spinning speed of 3000r/min and then baked on a hotplate at 180℃ for 10min. The pattern was defined by Raith150 electron-beam lithography system. After the exposure, the sample was developed in a mixture of methyl isobutyl ketone (MIBK) and isopropyl (IPA) at a ratio of 1∶3 for 20s, then rinsed by IPA and blow-dried with pure nitrogen. The patterns of nanostructure were transferred from PMMA resist to the top SiO_2 layer through the buffered HF etching. Then, the PMMA resist was stripped by soaking the sample in acetone. Consequently, the 30nm-thick SiO_2 layer remained after the buffered HF etching was used as a mask to define nanostructures during silicon anisotropic etching. The patterns of nanostructure were further shrunk because of the lateral etching of the SiO_2 mask. Finally, the (100) silicon top layer was etched in a tetra-methyl-ammonium-hydroxide (TMAH) / isopropyl alcohol (IPA) aqueous solution (TMAH (10%)∶H_2O∶IPA = 5∶15∶2, volume ratio) at 80℃. In such conditions, the etching rate was about 300nm/min with respect to the (100) planes.

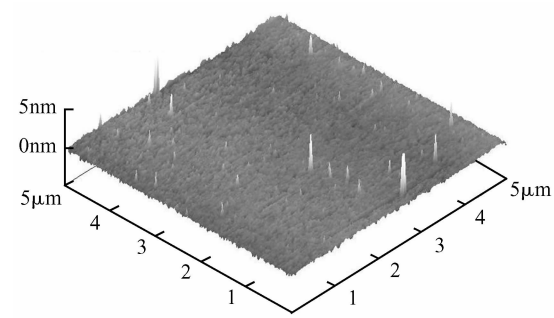


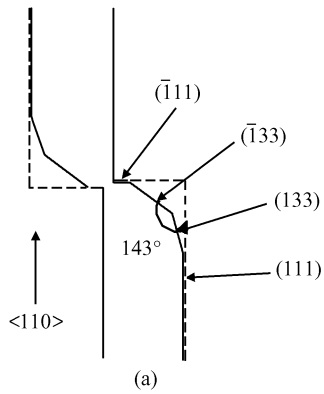
Fig. 1 AFM topography image of etched (111) surface etching by TMAH (10%)∶H_2O∶IPA = 5∶15∶2 solution at 80℃, RMS = 0.22nm

The etchant used was TMAH rather than KOH. TMAH solution does not contain harmful metal ions that might cause problems in the electrical circuits. In addition, it hardly attacks the silicon dioxide film. TMAH aqueous solution has very stable chemical properties for a normal etching process. Its boiling point is 102℃ and it does not decompose below 130℃. The addition of IPA into TMAH solution at high etching temperature can significantly decrease the roughness of the etched Si surface.

An etched (111) silicon surface was measured by AFM. Figure 1 shows the root-mean-square (RMS) roughness of the (111) surface is 0.220nm at a 5μm scan size. The smooth surface is very advantageous to electron transport in quantum devices.

3 Results and discussion

The principal feature of silicon anisotropic etching behavior is the different etching rate for different crystallographic planes. Especially, (111) surfaces are etched at much slower rate than other crystallographic planes. The precise mechanisms underlying the nature of anisotropic etching are not well understood yet. However, it has been confirmed that the variation of the density of atoms from plane to plane is responsible for the behavior of anisotropic etching. Another factor affecting the behavior of anisotropic etching is the active energy needed to remove an atom from the Si surface. For the silicon (100) planes, an atom on the surface has two dangling bonds and two other



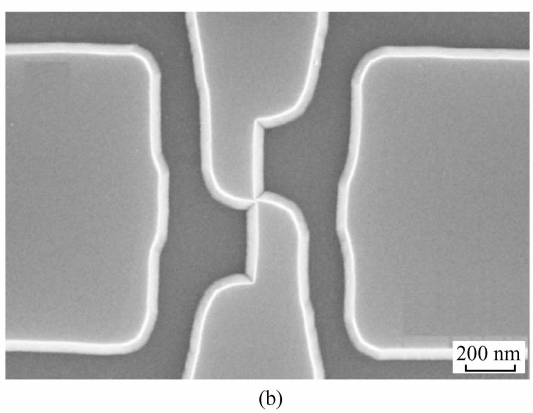
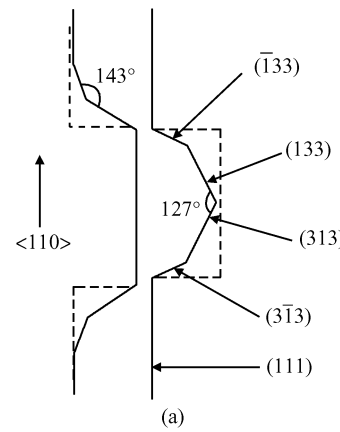


Fig. 2　(a) Schematic diagram of mask pattern and crystal facets for shift-nanowire structure on (100) SOI wafer; (b) SEM image of etched silicon point-contact structure



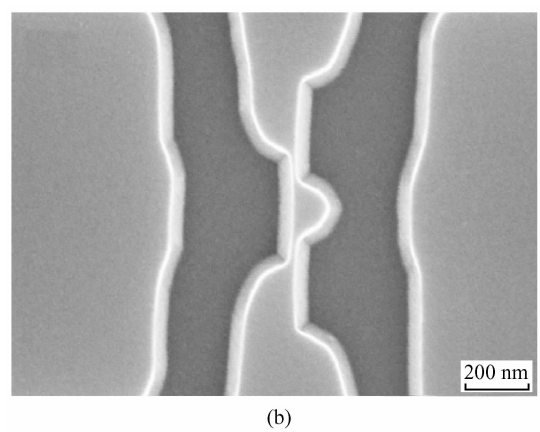
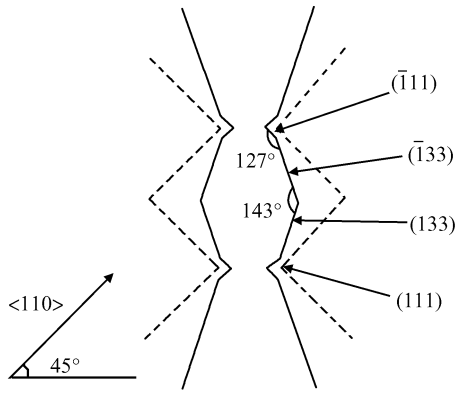


Fig. 3　(a) Schematic diagram of mask pattern and crystal facets for nanowire structure with double shifts on (100) SOI wafer; (b) SEM image of etched half-circle-shaped silicon island structure

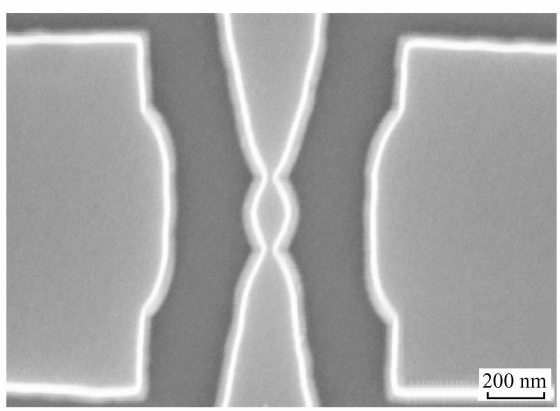
bonds connected to the inner atoms. Thus, there are two bonds that need to be broken to remove each atom. In the case of (111) planes, there is one dangling bond and three bonds connected to inner atoms, so three bonds have to be broken to remove an atom[11]. The etched structures whose edges of the mask oriented in the 〈110〉 directions are bounded by (111) crystallographic planes. Generally, convex corners will be undercut by anisotropic etching. The etching rate of undercutting is determined by the magnitude of the maximum etching rate, the etching rate ratios for different crystallographic planes, and the area of the local surface being actively attacked. Meanwhile, for a concave corner, very little undercutting occurs[12].

Figure 2 shows a silicon point-contact nanostructure with the minimum size sub-10nm of trapezoidal top. In Fig. 2(a), the schematic diagram of the etching mask pattern is shown with a dashed line. The edges of mask were designed in the 〈110〉 direction, in order to obtain nanostructures bounded by (111) planes. After electron-beam exposure, the convex corners of the pattern generally become round due to the proximity effect resulting from secondary electron scattering. The mask pattern of the PMMA resist was transferred to thermal oxidized SiO_2 by buffered HF etching. The oxide mask pattern is shrunk with rounder convex corners because of the lateral isotropic etching for the mask. Figure 2 (b) shows the SEM image of the shape of the silicon nanostructure after etching in TMAH + IPA aqueous solution. Two convex corners were undercut significantly. Figure 2 (a) provides a sketch map of crystal facets appearing on the two convex corners. The round part of the convex corner consists of intersectant {133} planes with a fixed angle of 143°[13]. The round shape is better for electron transport than the sharp angle. The point-contact structure is confined by two concave corners. The concave corner is limited by two adjacent {111} planes with the angle 90°. On one hand, etching concave corner results in very little undercutting; on the other hand, {111} planes has the slowest etching rate. These guarantee the fabrication of the point-contact structure is fixed and fine.

Figure 3 shows a half-circle silicon island, whose mask is designed as a rectangle and is connected to nanowire by two point contact structures. The corner shape of the mask is rounded by the proximity effect on resist film and the isotropic lateral etching for ox-



(a)



(b)

Fig. 4 (a) Schematic diagram of mask pattern and crystal facets for diamond nanostructure with an angle of 45° to 〈110〉 direction on the (100) SOI wafer; (b) SEM image of etched elliptical-shaped silicon island structure

ide film during the fabrication process. However the fixed orientation and angle of crystal facets are useful for the reproducibility of the silicon island shape. The convex and concave corners are rectified by a group of smooth crystal facets on {133}, {313}, and {111} planes during anisotropic etching. As shown in Fig. 3 (a), the angle of adjacent {133} facets is 143° and the angle of adjacent {313} and {133} facets is 127°. As the SEM image shown in Fig. 3 (b), point contact structures are spread out to be a short nanowire by the fast etching rate for {133} planes. We achieved a trapezoidal top for the silicon nanowire of less than 10nm.

Figure 4 shows an elliptical silicon island sandwiched between two point-contact nanostructures. In Fig. 4 (a), the schematic diagram of the mask is shown with a dashed line. The pattern was turned 45° to the primary 〈110〉 direction in order to ensure the surfaces of point-contact structure are bounded by four (111) crystal facets. The convex corners are limited by {133} and {111} crystal facets. As the SEM image in Fig. 4 (b) shows, the angle of adjacent two {133} planes is 143° and the angle adjacent {133} and {111} planes is 127°. The size of the trapezoidal top for the silicon point contact structure is less than 20nm.

4 Conclusion

Three different nanostructures consisting of point-contact structures were fabricated by electron beam lithography and the anisotropic wet etching technique. The surfaces of point-contact structure were limited by the low etching rate of the Si (111) planes, which is important for the good reproducibility of fabricating nanostructures. The facets adjacent to the Si (111) planes in those nanostructures were bounded by the fast etching rate of intersectant Si {133} planes with large angles. The minimum size of the trapezoidal top for those Si nanostructures can be shrunk to less than 10nm. The RMS roughness of the etched silicon (111) surface is 0.220nm at 5μm scan size by AFM observation. The smoothness of the nanostructure facets is important for electron transport in quantum effect devices. This fabrication technique is promising for silicon-based single electron devices, nano-MOSFET, and quantum logic circuits.

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利用电子束光刻制备晶面依赖的硅纳米结构*

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摘要：利用电子束光刻和各向异性湿法腐蚀技术，在(100)SOI 衬底上成功地制备出晶面依赖的硅纳米结构. 这项技术利用了硅的不同晶面在碱性腐蚀溶液中具有不同腐蚀速率的特性. 纳米结构脊部宽度的最小尺寸可以达到 10nm 以下. 扫描电镜和原子力显微镜的观察表明，利用这种方法制备出来的纳米结构具有很好的重复性，而且表面光滑.

关键词：硅纳米结构；各向异性湿法腐蚀；电子束光刻
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